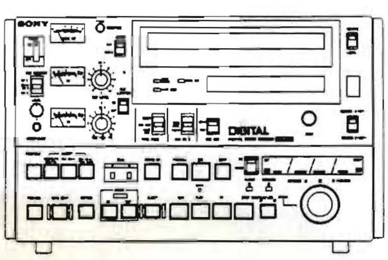
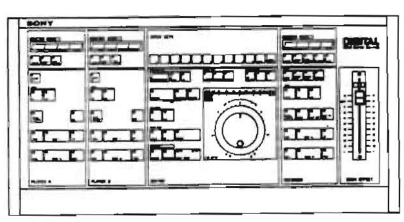
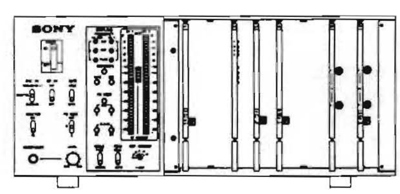
SONY®

Digital Mastering System
Training Manual

(DAE-1100/1100A, DMR-4000/2000, PCM-1610/1630)







DIGITAL MASTERING SYSTEM TRAINING MANUAL

(DAE-1100/1100A, DMR-4000/2000, PCM-1610/1630)

Training Manual

Prepared by the

PROFESSIONAL AUDIO TRAINING GROUP

SONY PROFESSIONAL PRODUCTS COMPANY

1st Edition, Rev. 2

DIGITAL AUDIO EDITOR/PCM PROCESSOR
TECHNICAL TRAINING MANUAL

SECTION 7 DAE-1100 SERIES DIGITAL AUDIO EDITOR

SECTION 1

INTRODUCTION

SECTION 1

INTRODUCTION

1.1 DIGITAL AUDIO MASTERING SYSTEM

In 1977, the SONY **PCM-1600** Digital Audio Processor was introduced to studios the world over. Since then, over 550 units of the **PCM-1600/1610** have been put into operation throughout the world. The second generation of Digital Audio Processor is the **PCM-1630.** Following in the trail blazed by the **PCM-1600/1610,** the **PCM-1630** incorporates new features such as: Read After Read (RAR), Read After Write (RAW), improved metering, and electronically balanced (transformerless) circuitry with oversampling at the output resulting in improved audio quality. It should be noted that the RAR and RAW functions of the **PCM-1630** are active only when the optional **DABK-1630** board is installed and **DMR-4000** Digital Master Recorder is used.

This second generation Digital Audio Mastering System is further enhanced with: The **DAE-1100A** Digital Audio Editor (the successor of the **DAE-1100**) which incorporates a wider variety of time saving functions to accelerate the editing process; The **DTA-2000** Digital Tape Analyzer which will drive any standard printer to create a hard copy of all errors on the Master tape; the **DFX-2400** sampling rate converter which will convert digital audio data at any sampling frequency input to it between 30kHz and 50kHz to digital audio data at any standard selected sampling frequency output desired:

example: 48kHz to 44.1kHz

The **DAQ-1000** PQ subcode editor for PQ subcode preparation of Digital Audio Master Tape; and finally the **DMU-30** Remote Metering Unit which allows remote placement of the **PCM-1630** with metering at the editor keyboard. The **DMU-30** not only provides the metering for the **PCM-1630,** it also provides error status indication.

All of these components are an integral part of the Digital Audio Mastering System, a system that is the unquestioned de facto standard of the industry. Soon to join this system are the new digital audio stationary head recorders, the **PCM-3102** (7-1/2 ips) DASH recorder, the **PCM-3202** (15 ips) Twin DASH recorder, and the **PCM-3402** multi-speed DASH machine. Soon to follow will be implementation of the new series R-DAT system machines for the fullest flexibility and compatibility for all forms of professional digital audio data storage.

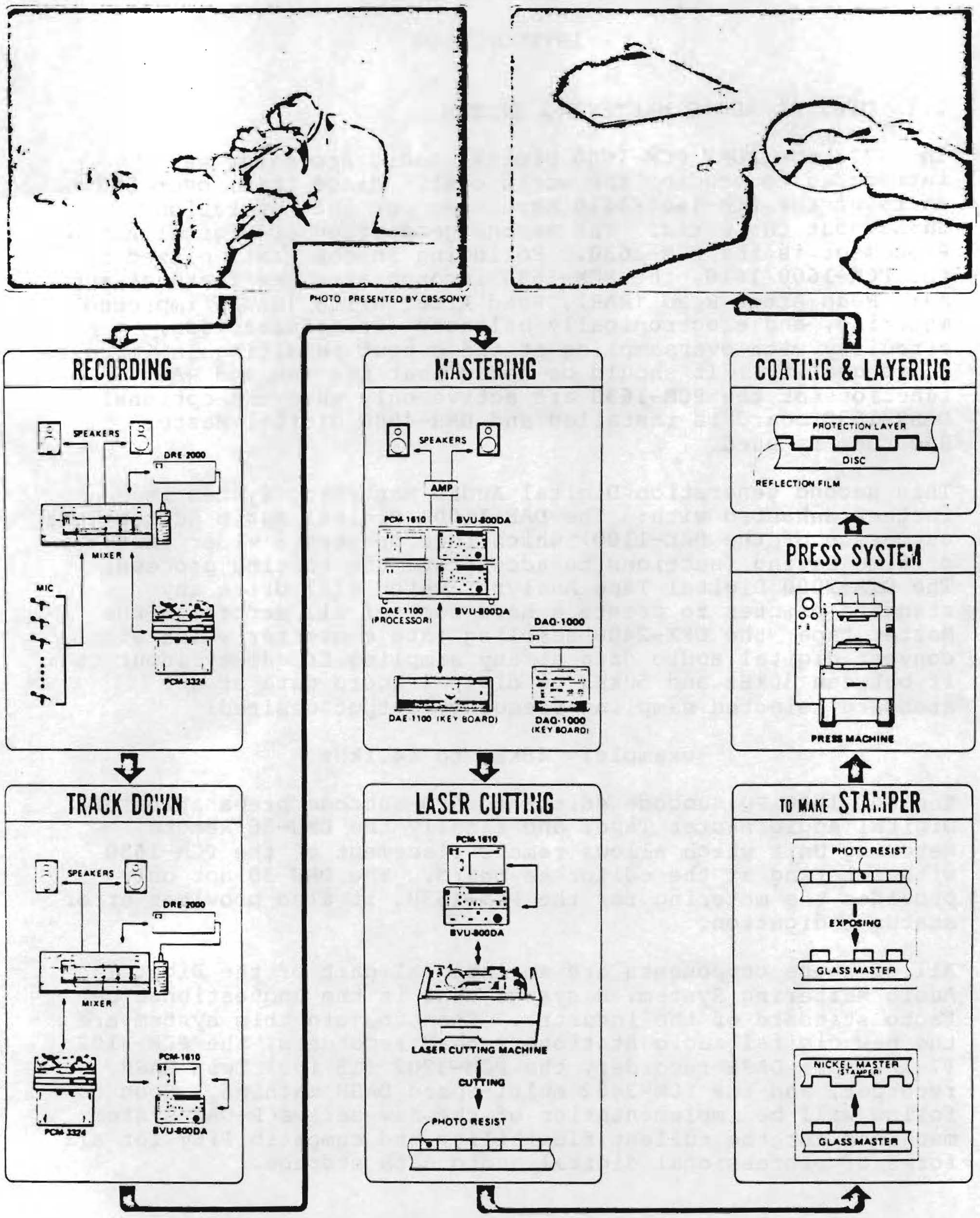


PHOTO PRESENTED BY CBS/SONY
RECORDING
SPEAKERS
DRE 2000
MIXER
MIC
PCM-3324
MASTERING
SPEAKERS
AMP
PCM-1610
BVU-800DA
DAE 1100 (PROCESSOR)
BVU-800DA
DAQ-1000
DAE 1100 (KEY BOARD)
DAQ-1000 (KEY BOARD)
COATING & LAYERING
PROTECTION LAYER
DISC
REFLECTION FILM
PRESS SYSTEM
PRESS MACHINE
TRACK DOWN
SPEAKERS
DRE 2000
MIXER
PCM-1610
PCM-3324
BVU-800DA
LASER CUTTING
PCM-1610
BVU-800DA
LASER CUTTING MACHINE
CUTTING
PHOTO RESIST
TO MAKE STAMPER
PHOTO RESIST
EXPOSING
GLASS MASTER
NICKEL MASTER (STAMPER)
GLASS MASTER

Figure 1

1.2 THE DIGITAL AUDIO MASTERING PATH

As shown in Figure 1-1, the flow chart of the production of Digital Audio Compact Discs begins with the initial recording of the material in PCM format. Currently, in some cases the original recordings are done on analog equipment, this being mostly true for older recordings. In some cases, the analog multi-track tapes are remixed onto a digital 2-track machine such as the **PCM-3000** series DASH recorders or directly to the **DMR-4000** using the **PCM-1630** Digital Audio Processor. State of the art is to use the **PCM-3324** DASH Digital Multi-track recorder and mixing down to one of the digital 2-track recorders.

The next step, after all material for the selection is recorded, is to do the final mix down or track-down to the Helical Scan PCM format. Sometimes, this involves a digital transfer from the **PCM-3000** series DASH recorders or the recording of an analog stereo master tape. The Mastering phase is next. The system shown in Figure 1-1 is a standard fully operational system able to prepare a Digital Audio Master Tape for Compact Disc (CD) production. STEPs 4, 5, 6, and 7 are part of the CD manufacturing process.

1.3 THE IMPORTANCE OF MASTER TAPE QUALITY

Digital Audio Master Tapes, while receiving a high degree of scrutiny prior to manufacture, must have the proper format and cue sheet logging any deviation or artistic aspect of the material. For example, if there are special instructions for the PQ Subcode editing of the tape, this should be noted to the CD manufacturing facility. The following is a list that outlines the most critical specifications of the Master Tape presented to a CD manufacturing facility for the production of Digital Audio Compact Discs.

From the standpoint of the recording engineer, it is important to ensure the quality of the master tape so that the tape presented to the CD manufacturing facility can be used directly in the disc cutter such as the **DMC-1200** Disc Master Cutter. This offers the total freedom of creativity to the producer. If the guidelines are not adhered to, delays in the Compact Disc production schedule are likely to occur and the possibility of errors in the final product are increased.

From the standpoint of the CD manufacturing facility, adherence to guidelines provides a more workable product whose quality need not be evaluated merely upon subjective listening tests. Given a listing of the specifications of the master tape, the ultimate goal of the CD manufacturing facility is to make an exact duplicate of the master tape. In creating an exact duplicate, the responsibility of the CD manufacturing facility is clearly defined and not accounted for by subjective methods, rather by objective results.

1.3.1 Specifications for CD Master Tape

1. Sampling frequency must be 44.1kHz.
2. Tape format must be 3/4-inch U-matic NTSC Standard.
3. Time code must be SMPTE Non-Drop Frame time code.
4. Time code must be synchronized to the NTSC video signal.
5. Time code shall run continuously and uninterrupted. Code shall not cross 23 hours, 59 minutes, 59 seconds, 29 frames.
6. Time code should be recorded on Analog Track #2 of the U-Matic Tape.
7. Record digital mute with time code for a minimum of 1 minute before the first track and 1:30 minutes after the last track.
8. A minimum of 2 seconds must be allowed for emphasis changes between tracks.
9. Prepare a list that is frame accurate to locate beginning and ending points
10. Prepare a noise information guideline that indicates any unusual noises or general notes regarding the quality of the recording.
11. Maximum program duration shall not exceed 73 minutes, 00 seconds.
12. The cue sheet information must be provided including the time code values for the start and end of each song. If there are any index points, these should also be included
13. A print out of a **DTA-2000** error analysis must accompany the master tape to the CD manufacturing facility.
14. The error rate on the tape must not be greater than 10 errors per minute of program material. Optimally, there should be less than 200 errors per hour.

1.4 OBJECTIVE

The objective of this manual is to provide a source of reference for the service and maintaining engineer. This manual will encompass all of the information necessary to properly install, maintain, and repair all of the components of the Digital Audio Mastering system.

SECTION 2

A GUIDE TO SYSTEM CONFIGURATION

SECTION 2

A GUIDE TO SYSTEM CONFIGURATION

2.1 INTRODUCTION

The purpose of this section is to describe the different means of connection of the Digital Audio Mastering system for different applications. In each of the subsections, the switch settings and some of the logistics of the connections are also covered. Below are brief descriptions of each of the subsections contained herein.

2.2 RECORDING AND PLAYBACK (BASIC CONNECTION)

The configurations shown in this section describe the basic connection for 2-track digital recording. It describes the connection between a PCM processor and a rotary head recorder.

2.3 LONG TERM RECORDING

The configurations shown here require the use of two rotary head recorders and one PCM processor. The two recorders are used alternately to produce a long time playback with continuous time code.

2.4 DIGITAL DUBBING

This section shows the configuration for duplicating digital audio tapes in the rotary head format. The equipment required is two rotary head recorders and one PCM processor.

2.5 ELEMENTARY EDITING

For editing to frame accuracy, this section shown the minimum configuration required. The same equipment as used in Digital Dubbing is required providing basic electronic editing features.

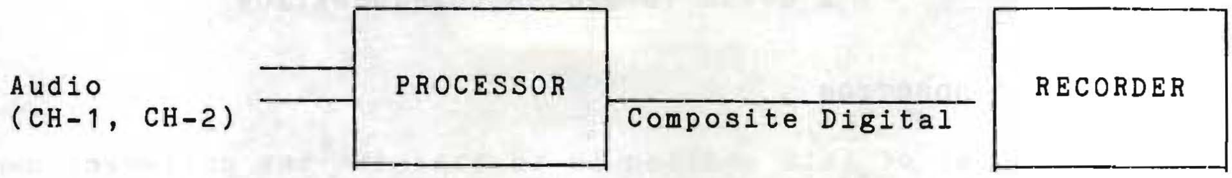
2.6 PRECISE EDITING WITH THE EDITOR

This section describes the configuration of the **DAE-1100** series Digital Audio Editor system.

2.7 PQ EDITING

In this section, PQ subcode editing configurations are described using the **DAQ-1000** Digital Audio Cue Editor.

2.2 RECORDING AND PLAYBACK (BASIC CONNECTION)



The connections shown in this section are the minimum requirements for a 2-track digital recorder in the rotary head format. A configuration like this may be used as the master recorder during a multi-track mixdown session. When this is done, the 2-track rotary head masters can be edited onto one tape (the complete project) using one of the electronic editing configurations described later in this chapter.

This configuration may also be used for transferring analog 2-track masters to digital rotary head format. If a DASH 2-track is used, it is preferable to do a digital data transfer rather than an analog transfer so that the quality of the audio is not degraded.

PROCESSOR	**RECORDER**	**PAGE**	**NOTE**
PCM-1630 (+**DABK-1630**)	**DMR-4000**	2-3	.RAR (with **DABK-1630**) .RAW (with **DABK-1630**) .TC READER/GENERATOR built in the **DMR-4000**
PCM-1630	**DMR-2000**	2-8	.TC READER/GENERATOR built in the **DMR-2000**
	BVU-800DB (+**BK-806**)	2-10	.TC READER/GENERATOR built in the **BVU-800DB**(with **BK-806**)
PCM-1610	**DMR-4000**	2-13	.RAW .TC READER/GENERATOR built in **DMR-4000** .TC GENERATOR built in **PCM-1610**
	DMR-2000	2-16	.TC READER/GENERATOR built in **DMR-2000** .TC GENERATOR built in **PCM-1610**
	BVU-800DB (+**BK-806**)	2-18	.TC READER/GENERATOR built in **BVU-800DB**(with **BK-806**) .TC GENERATOR built in **PCM-1610**

2.2.1 **DMR-4000/PCM-1630 (DABK-1630)**

SETTING OF DMR-4000

-Front Panel

.TRACKING control--------------FIXED
.Meter selector----------------R/P (w/o **DABK-1630**)*
.AUX LIMITER switch------------insignificant
.RAW OUT selector--------------MAIN
.AUX CH-2 selector-------------TIME CODE
.TIME CODE selector------------REC RUN**
.REMOTE/LOCAL selector---------LOCAL***
.REMOTE-1 (9P)/
REMOTE-2(36P)selector------REMOTE-2(36P)
.AUX MONITOR selector----------insignificant
.PB-PB/EE selector-------------PB/EE****

* when **DABK-1630** is installed may use CONFI to monitor RAR
** when using an external TC source use REGEN function
*** if also using a **DTA-2000** analyzer use REMOTE setting
****fixed with a switch protector

-Rear Panel

.75-ohm termination switch----ON (Composite Digital Input)

-SY-37 Board

.TIME CODE AUTO STOP MODE switch(S1)--position according to use

-TC-38 Board

.GENERATOR DF/NDF selector----select the position according to the program material or external TC generator (NDF Time Code must be used in CD Master Tapes)

-DM-49 Board

.Composite Digital Output switch--OFF(NORMAL)

SETTING OF PCM-1630

-Front Panel

.ENC IN selector----------------ANALOG
.DA IN selector-----------------INT
.MUTE indication mode selector--as desired*
.MONITOR selector---------------PB
.PB MODE selector---------------RAR(w/**DABK-1630**)-A(w/o **DABK-1630**)
.SCALE selector-----------------NORMAL
.PEAK indication mode selector--as desired

* HOLD recommended with RAR function to indicate MUTE
**PEAK OVER holding function recommended with RAR function

-Rear Panel

.75-ohm termination switch------insignificant
(Composite Sync Input)

-AD-23 Board

.EMP switch---------select position according to program material remembering that if EMPHASIS changes within the program material that there must be a 2 second space without music on the CD

-ENC-2 Board

.REC MUTE switch--------------OFF

-SIF-1 Board

.Fs selector--------select according to the program material remembering that for CD mastering, the sampling frequency will have to be 44.1kHz

-MT-16 Board

.PEAK HOLD switch---in fact this switch only affects the meters however it is recommended that the PEAK OVER holding function is used especially when the RAR function is being used so that an OVERLEVEL condition will keep the OVER LEDs lit

-DABK-1630 Board

.RAW switch-------------------OFF

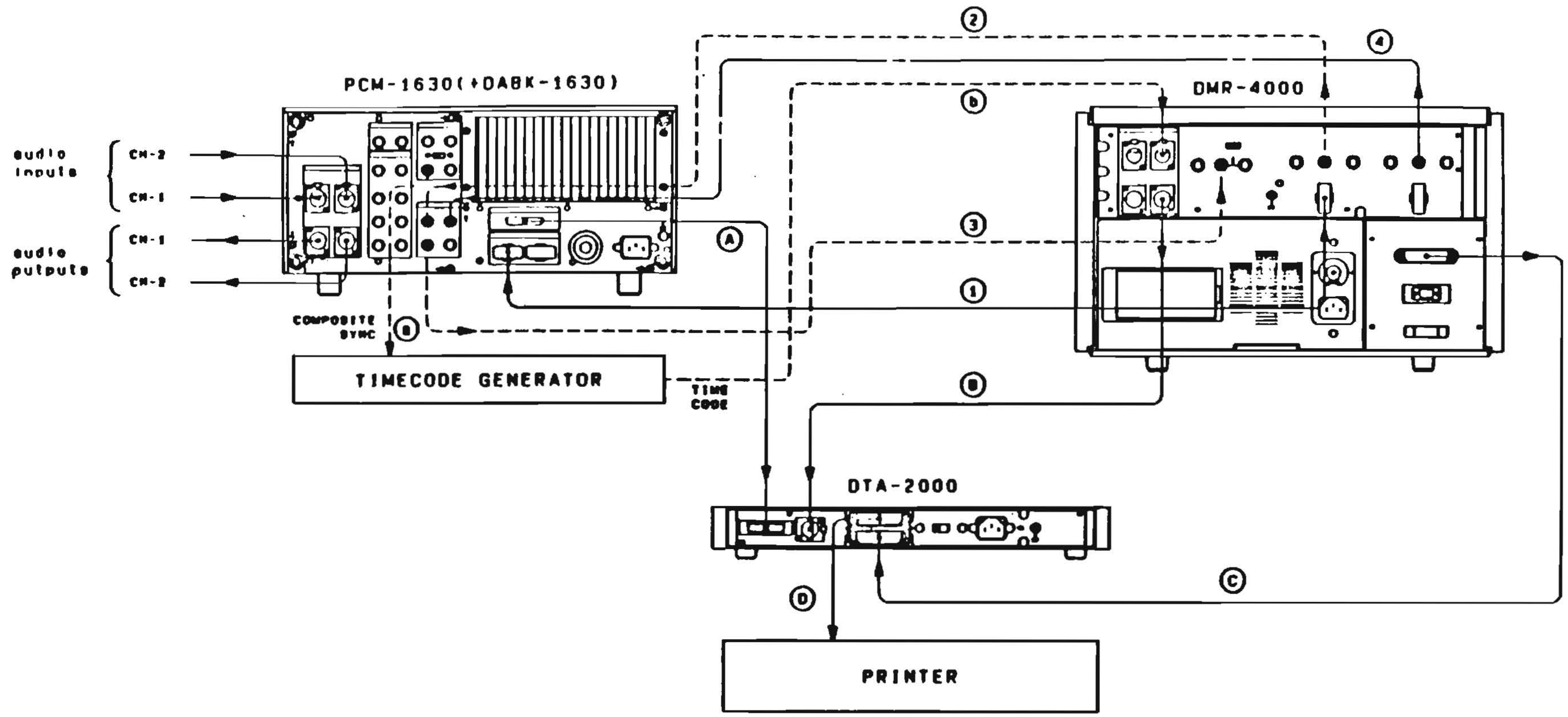
SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch-----------set this to AUTO for automatic function or set to MANUAL in which case the RUN and START switches must be pressed also

RECORDING AND PLAYBACK

PCM-1630(+DABK-1630)
DMR-4000



If the 8-pin connector (connection 1) is used the BNC input connectors (connections 2 and 3) are disabled, therefore unnecessary. Figure 2-2 shows the pin out of the 8-pin connector (female) located on the back of the **DMR-4000**. The BNC output connector may be connected to a monitor in this configuration allowing for a visual representation of the data.

(X) = High
(G) = Shield

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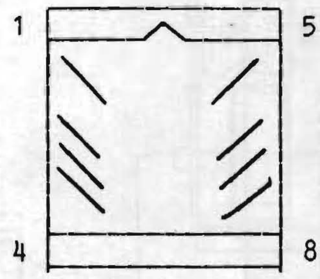
of O & M Manual



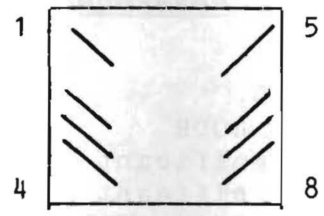
CN203

COMPOSITE
DIGITAL I/O

1	AUX CH-2 OUTPUT	(X)
2	COMPOSITE DIGITAL OUTPUT	(X)
3	COMPOSITE DIGITAL INPUT	(G)
4	COMPOSITE DIGITAL INPUT	(X)
5	AUX CH-2 OUTPUT	(G)
6	COMPOSITE DIGITAL OUTPUT	(G)
* 7	SELECT IN	
8	AUX CH-2 IN	

Figure 2-2 DMR-4000 8-pin Connector

As seen in figure 2-2, the connector allows for all necessary inputs and outputs on the **DMR-4000**. The **PCM-1630** allows for Composite Digital Input and Output only. Using this connector is not recommended when there is a need for external time code because the time code connectors are disabled. This connector can be used, however, when the time code source is the built-in generator of the **DMR-4000**. Usually this will be the case when transferring analog masters or when using the rotary head system as the 2-track Master recorder. It will not be acceptable where established time code values are already created for editing of the music or for conformance to video. Figure 2-3 shows the pin out of the 8-pin connector on the **PCM-1630**.



(X) = High
(G) = Shield

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1	N/C	
2	COMPOSITE DIGITAL INPUT A	(X)
3	GND	(G)
4	V PCM OUT 3	(X)
5	N/C	
6	GND	(G)
*7	GND	
8	N/C	

Figure 2-3 PCM-1630 8-pin Connector

*At the **PCM-1630** side of this connection, the SELECT IN line of the **DMR-4000** is connected to ground, thus presenting a low on the SELECT IN command line (activating the 8-pin connector). When activated, a logic low is routed (in the **DMR-4000**) to the relay RY-1 on the SW-103 board and to the CX20060(IC1) semi-conductor switch located on the MD-32 board.

Figure 2-1 shows all of the possible connections. When using an external TC generator, make connections a, and b. When using a **DTA-2000**, make connections A, B, C, and D. When utilizing the **DABK-1630** board for the RAR function, make connection 4.

NOTE: The RAW function in this configuration can be done by removing connection 4 and moving connection 2 from the MAIN OUTPUT to the SUB OUTPUT.

2.2.2 **DMR-2000/PCM-1630**

SETTING OF DMR-2000

-Front Panel

.TRACKING CONTROL--------FIXED
.CH-2 switch-------------TIME CODE
.AUX LIMITER switch------insignificant
.MONITOR SELECT switch---insignificant
.REMOTE/LOCAL switch-----REMOTE-2/LOCAL
.TIME CODE mode selector-AUTO STOP (internal time code)
REGEN (for external time code)
.MEMORY switch-----------select display mode

-Rear Panel

.NDF/DF selector---------select the position according to the program or the external TC generator

SETTING of PCM-1630

-Front Panel

.ENC IN selector------------------ANALOG
.DA IN selector-------------------INT
.MUTE indication mode selector----select mute indicator mode
.MONITOR selector-----------------PB
.PB MODE selector-----------------A
.SCALE selector-------------------NORMAL
.PEAK indication mode selector----select metering mode

-Rear Panel

.75-ohm termination switch(COMPOSITE SYNC INPUT)--insignificant

-AD-23 Board

.EMP switch-----select the position according to the program

-ENC-2 Board

.REC MUTE switch---OFF

-SIF-1 Board

.Fs selector-------select 44.1kHz for CD Mastering

-MT-16 Board

.PEAK HOLD switch---select desired metering mode

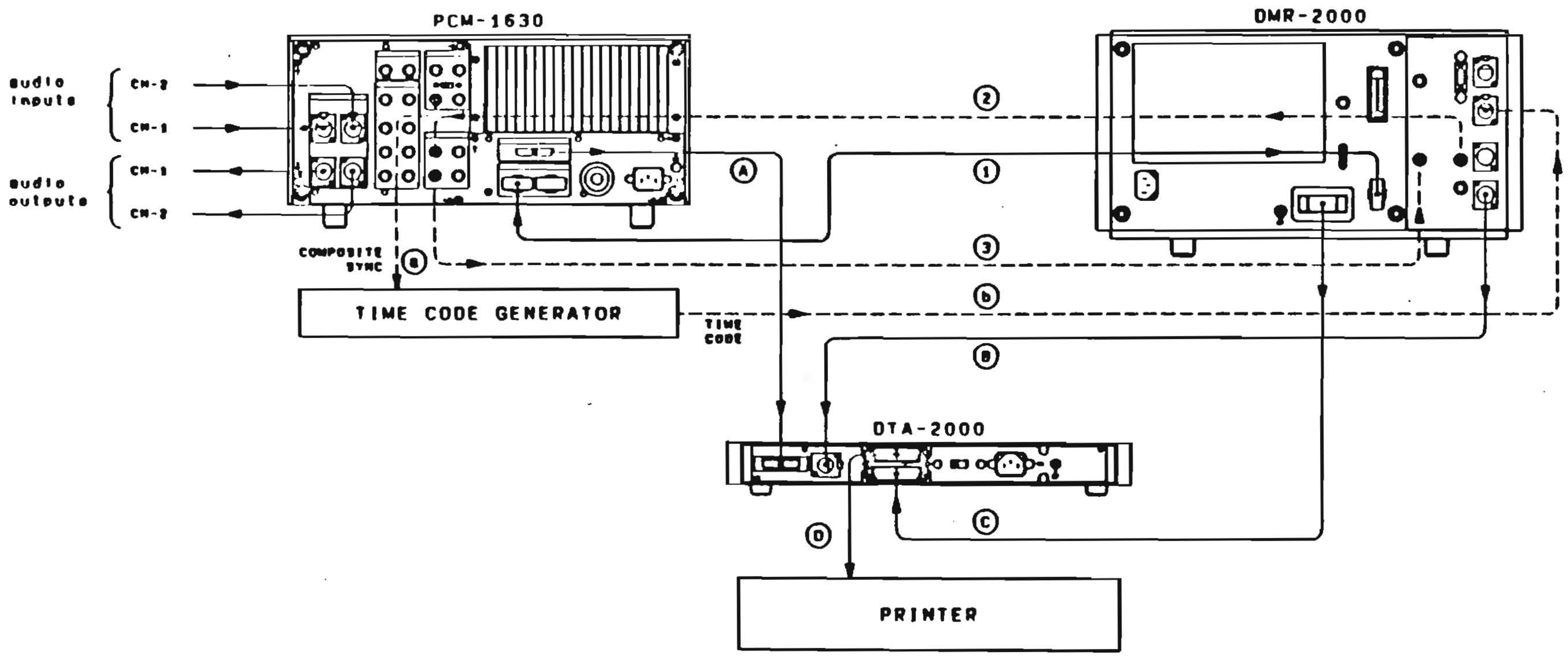
SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to desired mode of operation (use RUN, START, and STOP in MANUAL mode

RECORDING AND PLAYBACK

PCM-1630
DMR-2000



2.2.3 BVU-800DB (BK-806)/PCM-1630

SETTING OF BVU-800DB

-Front Panel

```
.TRACKING control-------------FIXED
.TIME CODE switch-------------TC TRACK (TC GENERATOR in BK-806)
                              AUDIO CH-2 (w/o BK-806)
.AUDIO MONITOR selector-------CH-2
.AUDIO LIMITER switch---------insignificant  ┐
.MIXING SELECT switch---------OFF            │
.MUTE SELECT switch-----------NORMAL         │
.VIDEO INPUT SELECTION switch-LINE           │fixed with switch
.REMOTE-1(9P)/REMOTE-2                       │          protectors
       (36P) selector--------REMOTE-2(36P)   │
.PB/PB/EE selector------------PB/EE          ┘
.REMOTE/LOCAL selector--------REMOTE (when using DTA-2000)
                              LOCAL (w/o DTA-2000)
```

-Rear Panel

```
.COLOR ON/OFF switch----------------OFF
.DOC ON/OFF switch------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)----ON
.AUDIO IN LEVEL selectors-----------HIGH
.600-ohm ON/OFF switches(AUDIO IN)--set for external TC generator
                                    insignificant w/internal TC
```

SETTING OF BK-806

```
.INT TC/EXT TC select switch-----INT TC
.NDF switch----------------------NDF used for CD Mastering
                                 DF may be selected if required
.ERROR BYPASS switch-------------ON
.Editing mode switch-------------AUTO*
                      *(When the TIME CODE switch on the front
                        panel is set to TC TRACK, the time code
                        on AUDIO CHANNEL-2 is displayed on the
                        time counter.)
```

SETTING OF PCM-1630

-Front Panel

```
.ENC IN selector------------------ANALOG
.DA IN selector-------------------INT
.MUTE indication mode selector----sets MUTE indicator HOLD or
                                  normal (indicator LED only)
.MONITOR selector-----------------PB
.PB MODE selector-----------------A
.SCALE selector-------------------NORMAL
.PEAK indication mode selector----selects metering mode, PEAK OVER
                                  holding is recommended for most
                                  critical applications
```

-Rear Panel

.75-ohm termination switch
(COMPOSITE SYNC INPUT)------insignificant

-AD-23 Board

.EMP switch----------------select according to the program. Remember that for CD Mastering that there must be a 2 second silence if the EMPHASIS mode is changed within the CD.

-ENC-2 Board

.REC MUTE switch----------OFF (when this is ON, no recording will take place)

-SIF Board

.Fs selector---------------select the position according to the program material. For CD Mastering, the sampling frequency must be set to 44.1kHz.

-MT-16 Board

.PEAK HOLD switch----------select the position according to the desired metering mode. For the most critical applications, the OVER LED should never illuminate, therefore it is recommended to use the PEAK OVER holding mode so that whenever an overlevel condition is detected, the OVER LED remains illuminated.

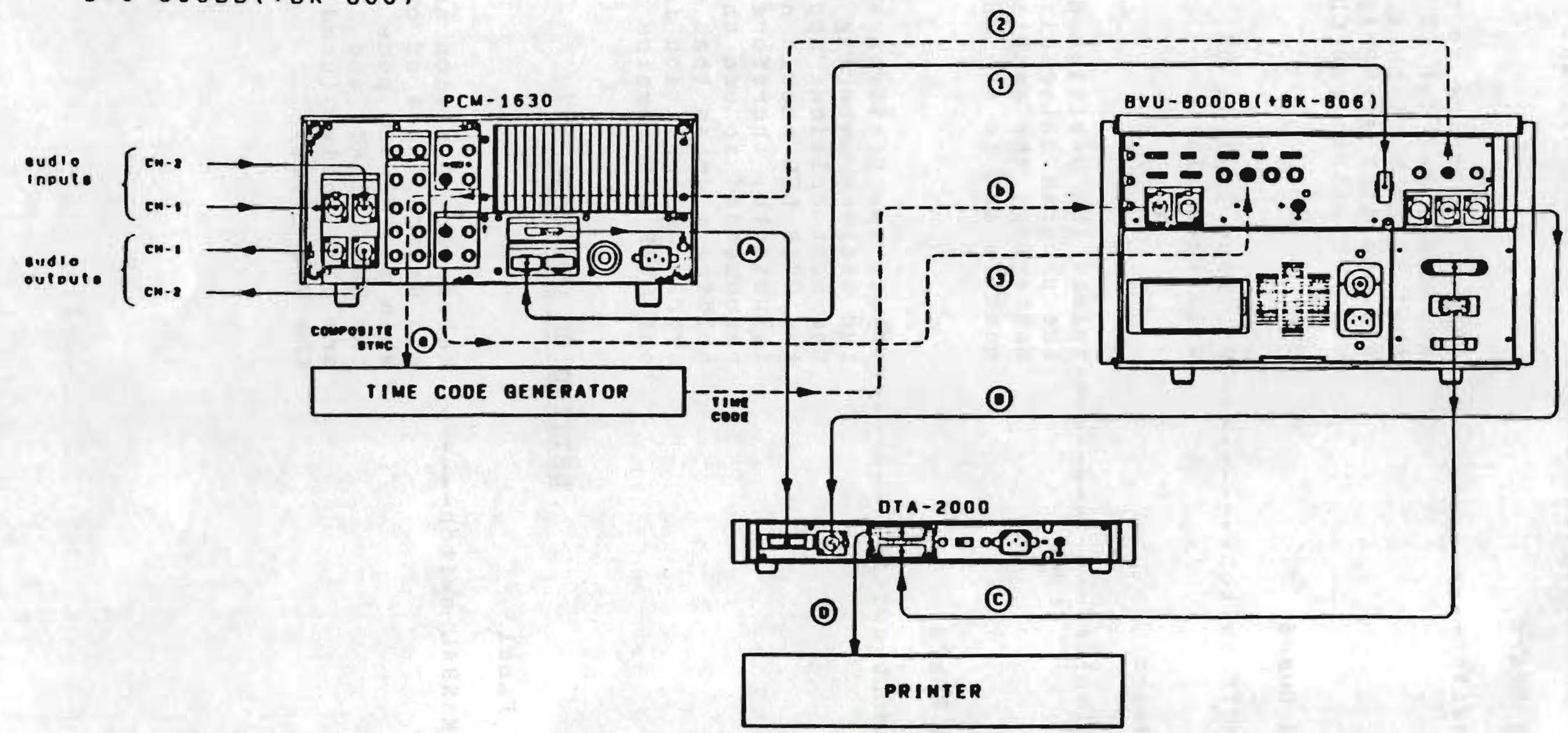
SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch--------select the position according to the desired mode of operation. When the MANUAL mode is selected, the RUN, START, and STOP switches are also active (used to control the **BVU-800DB**)

RECORDING AND PLAYBACK

PCM-1630
BVU-800DB(+BK-806)



2.2.4 DMR-4000/PCM-1610

SETTING OF DMR-4000

-Front Panel

```
.TRACKING control------------FIXED
.METER selector--------------R/P (meter monitors main video
                             heads)
.AUX LIMITER switch----------insignificant
.RAW OUT selector------------MAIN
.AUX CH-2 selector-----------TIME CODE
.TIME CODE selector----------REC RUN
.REMOTE/LOCAL selector-------LOCAL (w/o DTA-2000)
                             REMOTE (with DTA-2000)
.REMOTE-1(9P)/REMOTE-2(36P)
 selector--------------------insignificant (w/o DTA-2000)
                             REMOTE-2 (with DTA-2000)
.AUX MONITOR selector--------insignificant
.PB/PB/EE selector-----------PB/EE (fixed with a switch
                             protector)
```

-Rear Panel

```
.75 ohm termination switch---ON
 (COMPOSITE DIGITAL INPUT)
```

-SY-37 Board

```
.TIME CODE AUTO STOP MODE switch
 (S1)------------------------select TC generator mode of
                             operation
```

-TC-38 Board

```
.GENERATOR DF/NDF selector---for CD Mastering select NDF.  For
                             some applications (such as
                             external TC) the DF mode may be
                             used
```

-DM-49 Board

```
.Composite Digital Output switch--OFF (NORMAL)
```

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch--insignificant
.MONITOR/METER switch---------PB
.MUTING mode selector---------selects the MUTING mode, set to the desired position
.D/A INPUT selector-----------INTERNAL
.A/D INPUT selector-----------ANALOG

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)------insignificant

-Encoder Board

.EMPHASIS switch------------select the position according to the program material. Remeber that for CD Mastering there must be a 2 second pause (silence) in the program if the EMPHASIS mode is changed.

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector-------for CD Mastering, this must be set for 44.1kHz, however, it may be set for 44.056kHz if desired

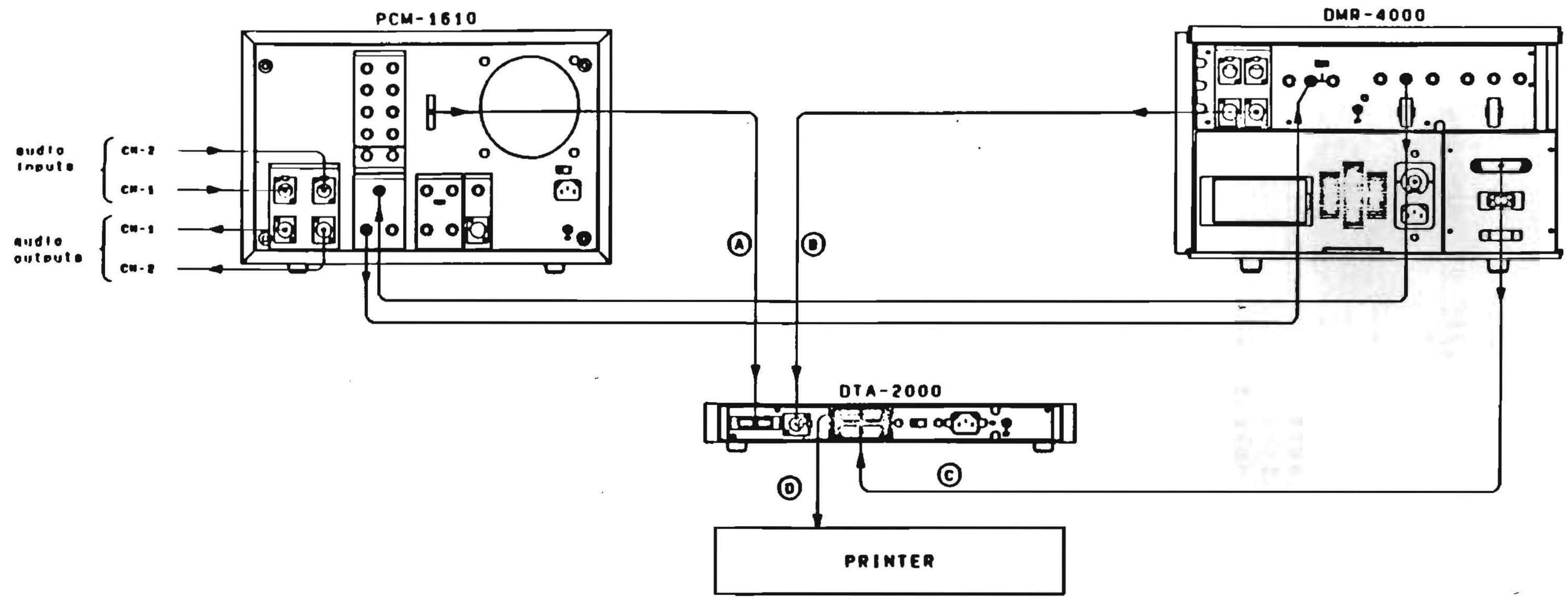
SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---------selects the mode of operation of the **DTA-2000**. If the MANUAL mode is used, the RUN, START, and STOP switches will activate the printer and the rotary head recorder. When using the **DTA-2000** make sure the recorder is set for REMOTE control on the 36-pin port (REMOTE-2).

RECORDING AND PLAYBACK

PCM-1610
DMR-4000



2.2.5 DMR-2000/PCM-1610

SETTING OF DMR-2000

-Front Panel

.TRACKING CONTROL----------FIXED
.CH-2 switch---------------TIME CODE
.AUX LIMITER switch--------insignificant
.MONITOR SELECT switch-----insignificant
.REMOTE/LOCAL switch-------REMOTE-2/LOCAL
.TIME CODE mode selector---AUTO STOP
.MEMORY switch-------------selects the display mode

-Rear Panel

.NDF/DF selector-----------use NDF for CD Mastering, DF may be used where required

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch--insignificant
.MONITOR/METER switch--------PB
.MUTING mode selector--------selects the muting mode
.D/A INPUT selector----------INTERNAL
.A/D INPUT selector----------ANALOG

-Rear Panel

.75 ohm termination switch
(COMPOSITE SYNC INPUT)-----insignificant

-Encoder Board

.EMPHASIS switch--set according to the program material, changes in setting between selections must have 2 second pause (silence) on CD

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL)
selector---------------------for CD Mastering use 44.1kHz

SETTING OF DTA-2000

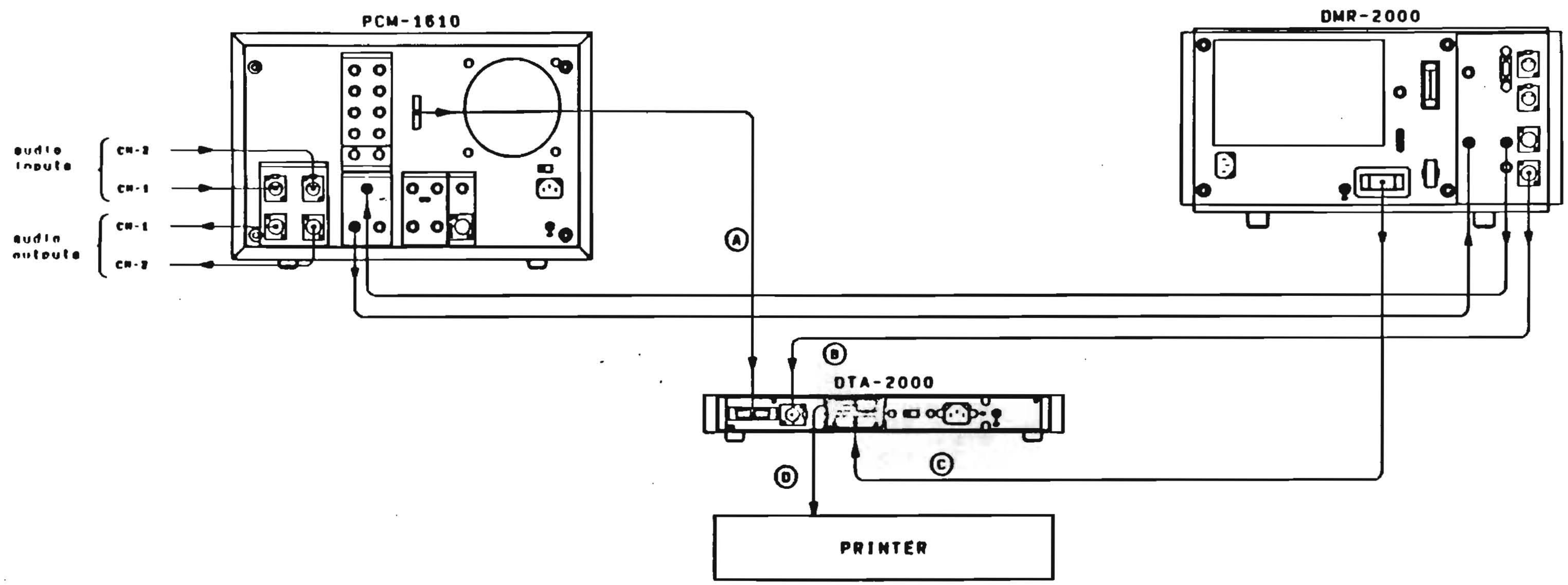
-Front Panel

.AUTO/MANUAL switch----selects the mode of operation. When MANUAL is used, the RUN, START, and STOP switches are active.

NOTE: When using the **DTA-2000**, make connections A through D as shown in Figure 2-7.

RECORDING AND PLAYBACK

PCM-1610
DMR-2000



2.2.6 BVU-800DB (BK-806)/PCM-1610

SETTING OF BVU-800DB

-Front Panel

```
.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK (with BK-806)
                                     AUDIO CH-2 (w/o BK-806)
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL
.VIDEO INPUT SELECT switch-----------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2(36P)
.PB/PB/EE selector-------------------PB/EE
.REMOTE/LOCAL selector---------------LOCAL (w/o DTA-2000)
                                     REMOTE (with DTA-2000)
```

-Rear Panel

```
.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--ON
```

SETTING OF BK-806

```
.INT TC/EXT select switch----INT TC
.NDF switch------------------for CD Mastering use NDF, DF
                             may also be used if required
.ERROR bypass switch---------ON
.Editing mode switch---------AUTO*
```

NOTE: When the TIME CODE switch on the front panel is set to TC TRACK, the time code on AUX CH-2 (audio channel 2) is displayed on the time counter.

SETTING OF PCM-1610

-Front Panel

```
.TIME CODE GENERATOR switch--if TC Generator is used set to NDF
                             (not used with BK-806)
.MONITOR/meter switch--------PB
.MUTING mode selector--------selects the desired muting mode
.D/A INPUT selector----------INTERNAL
.A/D INPUT selector----------ANALOG
```

-Rear Panel

```
.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant
```

-Encoder Board

.EMPHASIS switch----------select the position according to the program material. Any changes in the EMPHASIS mode between selections on a CD must be accompanied by a 2 second pause (silence) in the program material.

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector-------------------------for CD Mastering this must be set to 44.1kHz, however this may be set to 44.056kHz if required.

<u>SETTING OF DTA-2000</u>

-Front Panel

.AUTO/MANUAL switch--------selects the mode of operation of the **DTA-2000**. If the MANUAL mode is used, the RUN, START, and STOP switches will activate the printer and the rotary head recorder. When using the **DTA-2000** make sure the recorder is set for REMOTE control on the 36-pin port (REMOTE-2).

NOTE: When using the **DTA-2000**, make connections A - D as shown in Figure 2-8.

When using the TIME CODE GENERATOR of **PCM-1610**, make a connection a and be sure to set the **BVU-800DB** for external time code.

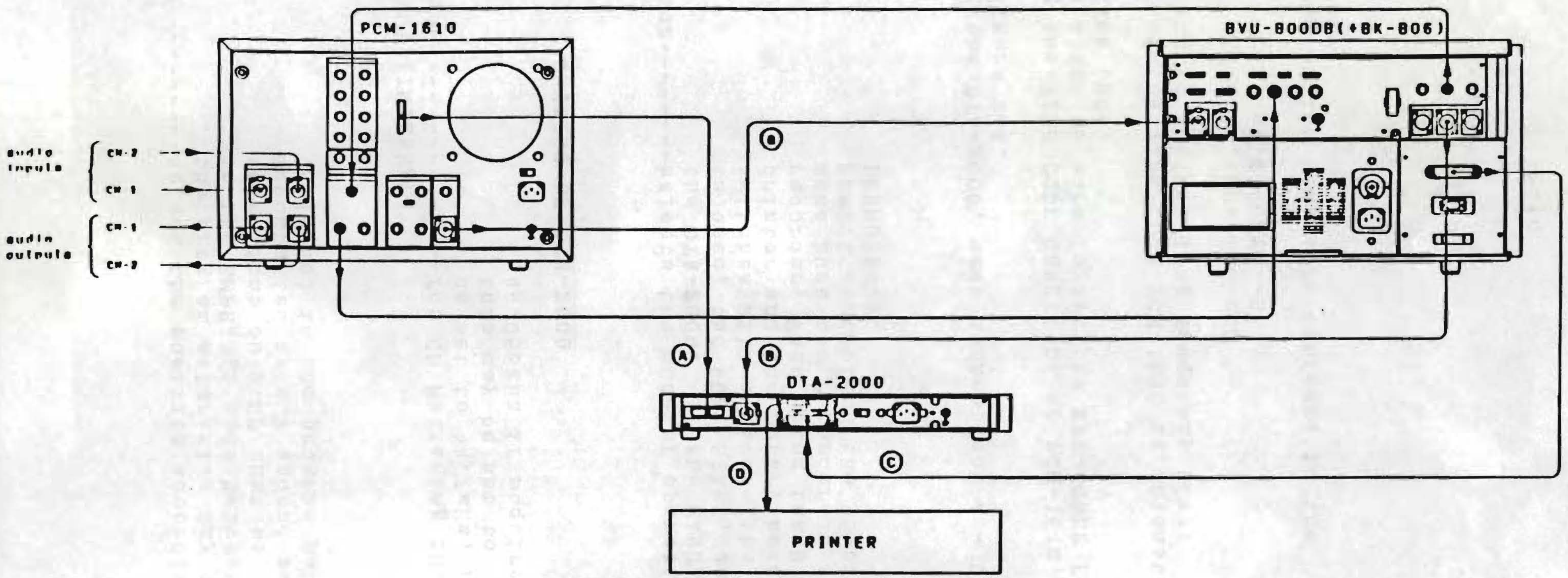
The DF/NDF of the TIME CODE **PCM-1610** is automatically set according to the sampling frequency (Fs):

Fs = 44.1kHz-----NDF
Fs = 44.056kHz---DF

This is done so the time code conforms to the sampling rate.

RECORDING AND PLAYBACK

PCM-1610
BVU-800DB(+BK-806)



2.3 LONG TERM RECORDING

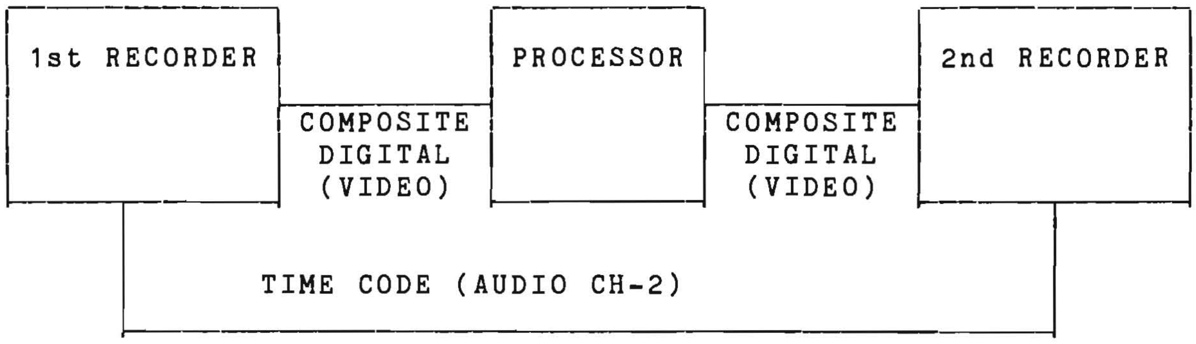


Figure 2-9 Long Time Recording Block Diagram

If playback is performed using a processor and two recorders (one of them must be **DMR-4000** or **DMR-2000**) alternately, a long time recording with a continuous time code can be made. This configuration may be used in the case that the master recording is made over two 30 minute or 60 minute tapes and a continuous playback with a continuous time code track needs to be achieved. At this time, the program material may be duplicated to one of the newly developed long playing tapes which are 75 minutes in duration. The maximum program length for a single Compact Disc (CD) is of course 73 minutes.

PROCESSOR	**RECORDER**	**2nd RECORDER**	**PAGE**	**NOTE**
PCM-1630	**DMR-4000**	**DMR-4000**	2-22	.RAW(both RECORDERs)
		DMR-2000	2-25	.RAW(1st RECORDER)
		BVU-800DB	2-28	
	DMR-2000	**DMR-4000**	2-31	.RAW(2nd RECORDER)
		DMR-2000	2-34	
		BVU-800DB	2-37	
PCM-1610	**DMR-4000**	**DMR-4000**	2-40	.RAW(1st RECORDER or 2nd RECORDER)
		DMR-2000	2-43	.RAW(1st RECORDER)
		BVU-800DB	2-46	
	DMR-2000	**DMR-4000**	2-49	.RAW(2nd RECORDER)
		DMR-2000	2-52	
		BVU-800DB	2-54	

Table 2-2 Long Time Recording Configuration Index

2.3.1 DMR-4000/PCM-1630

SETTING OF DMR-4000 (1st RECORDER)

-Front Panel

.TRACKING control----------------------FIXED
.METER selector------------------------R/P (monitors main video output)
.AUX LIMITER switch--------------------insignificant
.RAW OUT selector----------------------MAIN
.AUX CH-2 selector---------------------TIME CODE
.TIME CODE selector--------------------FREE RUN
.REMOTE/LOCAL selector-----------------LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---insignificant
.AUX MONITOR selector------------------insignificant
.PB/PB/EE selector---------------------PB/EE (fixed/switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT) --------ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---use NDF for CD Mastering, DF may be used if required (conform to 44.056kHz)

-DM-49 Board

.Composite Digital Output switch--OFF(NORMAL)

SETTING OF PCM-1630

-Front Panel

.ENC IN selector----------------ANALOG
.DA IN selector-----------------INT
.MUTE indication mode selector--selects mute indicator mode, for the most critical work use MUTE HOLD mode
.MONITOR selector---------------PB
.PB MODE selector---------------A
.SCALE selector-----------------NORMAL
.PEAK indication mode selector--selects the metering mode, for the most critical work use PEAK OVER holding mode

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)-------------insignificant

-AD-23 Board

.EMP switch---set according to program material. When EMPHASIS mode is changed there must a a 2 second pause on the CD

-ENC-2 Board

.REC MUTE switch---OFF

-SIF-1 Board

.Fs selector---select 44.1kHz for CD Mastering

-MT-16 Board

.PEAK HOLD switch---selects the metering mode. It is recommended to use the PEAK OVER holding mode

SETTING OF DMR-4000 (2nd RECORDER)

-Front Panel

.TRACKING control-----------------------FIXED
.METER selector-------------------------R/P (main video output)
.AUX LIMITER switch---------------------insignificant
.RAW OUT selector-----------------------SUB
.AUX CH-2 selector----------------------TIME CODE
.TIME CODE selector---------------------REGEN
.REMOTE/LOCAL selector------------------LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---insignificant
.AUX MONITOR selector------------------insignificant
.PB/PB/EE selector---------------------PB/EE (fixed/switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT) --------ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)--------insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---should be the same as the 1st RECORDER

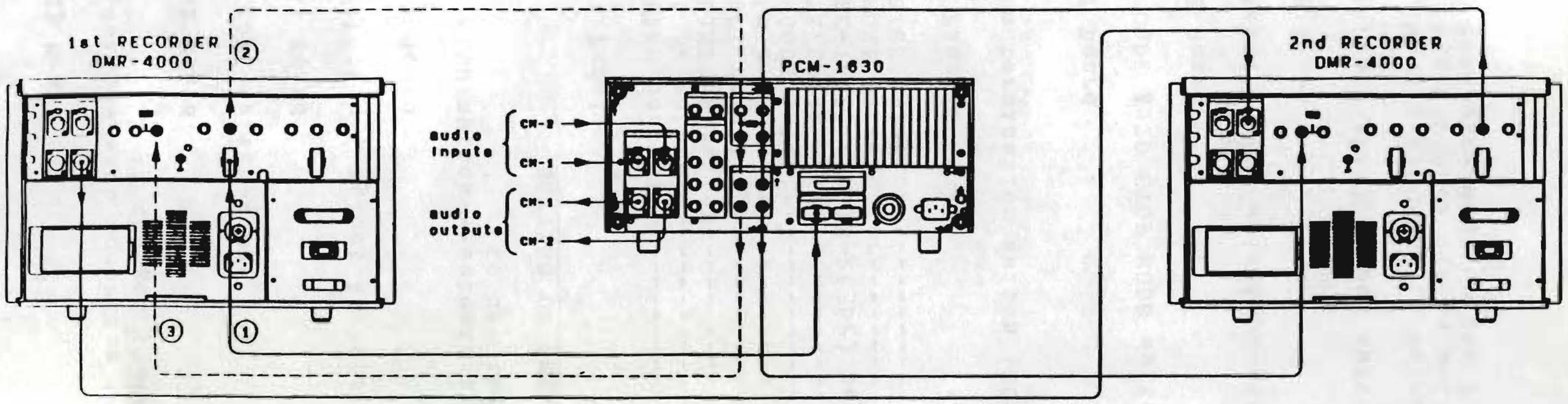
-DM-49 Board

.Composite Digital Output switch--OFF(NORMAL)

NOTE: When a RECORDER is in record mode, the CONFI signal of the RECORDER can be monitored by using the METER switch, otherwise monitor the R/P signal.

Long Time Recording

PCM-1630
DMR-4000
DMR-4000



2.3.2 DMR-4000/DMR-2000/PCM-1630

SETTING OF DMR-4000 (1st RECORDER)

-Front Panel

```
.TRACKING control-----------FIXED
.METER selector------------selects main (R/P) or confidence
                           (CONFI) video signals
.AUX LIMITER switch--------------------insignificant
.RAW OUT selector----------------------MAIN
.AUX CH-2 selector---------------------TIME CODE
.TIME CODE selector--------------------FREE RUN
.REMOTE/LOCAL selector-----------------LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---insignificant
.AUX MONITOR selector-------------------insignificant
.PB/PB/EE selector-----------------PB/EE (fixed/switch protector)
```

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)-----ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---------insignificant

-TC-38 Board

```
.GENERATOR DF/NDF selector---for CD mastering use NDF, DF may be
                             used if required (conform to 44.056kHz)
```

-DM-49 Board

.Composite Digital Output switch-----OFF(NORMAL)

SETTING OF PCM-1630

-Front Panel

```
.ENC IN selector-----------------ANALOG
.DA IN selector------------------INT
.MUTE indication mode selector---selects the MUTE indicator mode,
                                 it is recommended to use HOLD
                                 for the most critical applications
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL
.PEAK indication mode selector---selects metering mode, use PEAK
                                 OVER holding for most critical
                                 application
```

-Rear Panel

.75 ohm termination switch (COMPOSITE SYNC INPUT)----------OFF

-AD-23 Board

.EMP switch---select the position according to the program material, whenever EMPHASIS mode is changed between selections of a CD it is necessary to leave a 2 second pause (silence).

-ENC-2 Board

.REC MUTE switch--- OFF (when this switch is ON, no recording will take place)

-SIF-1 Board

.Fs selector------- select 44.1kHz for CD mastering. 44.056kHz can be used where required, however this will not meet the criteria of the CD Mastering facility. If 44.056kHz is used, use DF time code to conform to the sampling rate.

-MT-16 Board

.PEAK HOLD switch-- this switch only affects the metering mode of the **PCM-1630**. In the most critical applications, no OVER level reading are acceptable, therefore it is recommended to set the PEAK OVER holding mode so that if an OVER level condition occurs, the LED will remain illuminated.

SETTING OF DMR-2000 (2nd RECORDER)

-Front Panel

.TRACKING CONTROL------------------FIXED
.CH-2 switch-----------------------TIME CODE
.AUX LIMITER switch----------------insignificant
.MONITOR SELECT switch-------------insignificant
.REMOTE/LOCAL switch---------------REMOTE-2/LOCAL
.TIME CODE mode selector-----------REGEN
.MEMORY switch---------------------OFF

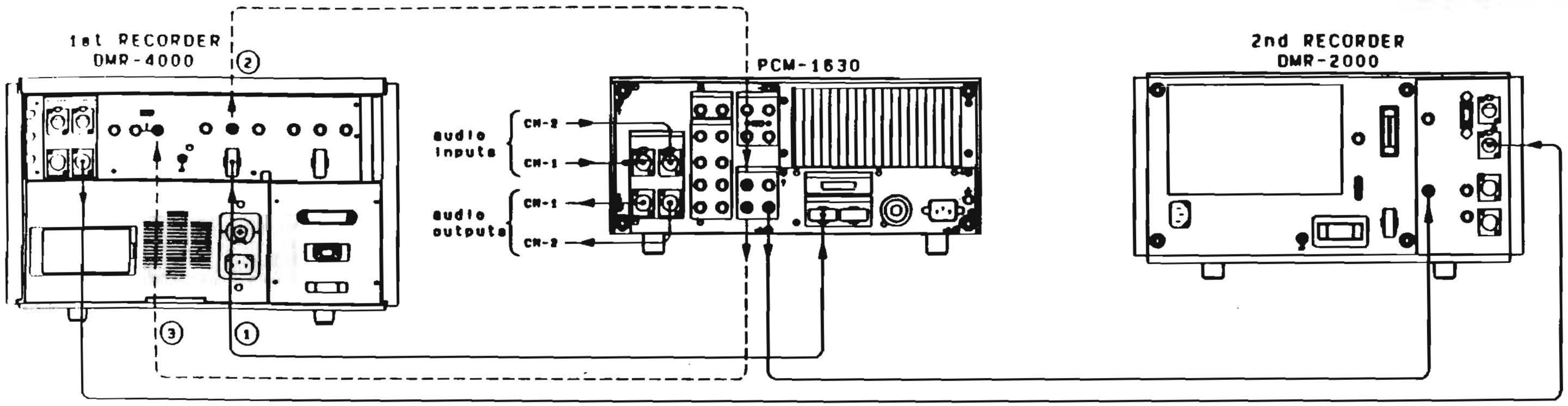
-Rear Panel

.NDF/DF selector-------------------select the position according to the 1st RECORDER

NOTE: When the 1st RECORDER is in RECORD mode, the CONFI signal of the 1st RECORDER can be monitored. The **DMR-2000** (2nd RECORDER) cannot be monitored in this fashion due to the fact that it does not have a CONFIDENCE HEAD.

Time Recording

PCM-1630
DMR-4000
DMR-2000



2.3.3 DMR-4000/BVU-800DB/PCM-1630

SETTING OF DMR-4000 (1st RECORDER)

-Front Panel

.TRACKING control----------FIXED
.METER selector------------selects main (R/P) or confidence
(CONFI) video signals
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------MAIN
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------FREE RUN
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---------insignificant
.AUX MONITOR selector------------------------insignificant
.PB/PB/EE selector---------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

..GENERATOR DF/NDF selector---use NDF for CD Mastering, DF may be
used for conformance to 44.056kHz Fs

-DM-49 Board

.Composite Digital Output switch---OFF(normal)

SETTING OF BVU-800DB (2nd RECORDER)

-Front Panel

.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL
.VIDEO INPUT SELECT switch-----------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2(36P)
.PB/PB/FF selector-------------------PB/EE
.REMOTE/LOCAL selector---------------LOCAL

fixed with switch protectors

-Rear Panel

.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch------------------OFF
.75 ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600 ohm ON/OFF switches (AUDIO IN)--ON

SETTING OF PCM-1630

-Front Panel

.ENC IN selector--------------------ANALOG
.DA IN selector---------------------INT
.MUTE indication mode selector------selects the MUTE indicator LED mode of operation. The LED can be illuminated momentarily when a mute condition exists (NORMAL) or remain continuously lit until reset by way of the switch (HOLD). For most critical applications use MUTE HOLD mode.
.MONITOR selector-------------------PB
.PB MODE selector-------------------A
.SCALE selector---------------------NORMAL
.PEAK indication mode selector------selects PEAK HOLD or NORMAL mode affecting only the meter display. For most critical applications use the PEAK HOLD mode.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---selects EMPHASIS, this is set subjectively according to the program material. If EMPHASIS is changed between selections on a CD, there must be a 2 second pause (silence) in the program.

-ENC-2 Board

.REC MUTE switch--------------------OFF

-SIF-1 Board

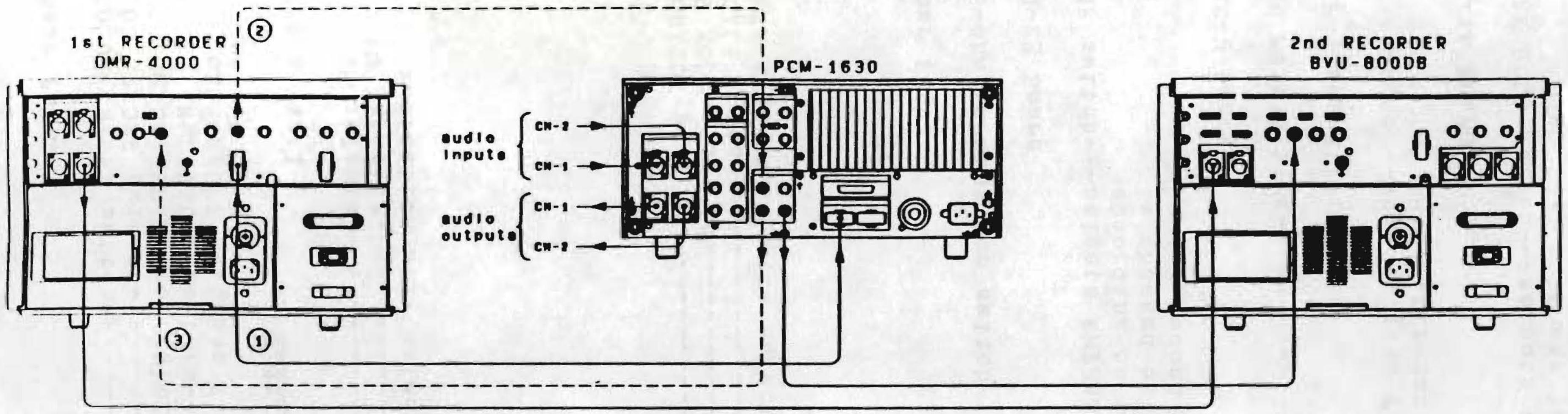
.Fs selector---use 44.1kHz for CD mastering (44.056kHz can be used if required (conform to color or DF time code)

-MT-16 Board

.PEAK HOLD switch---selects the metering mode. It is recommended to use the PEAK OVER HOLD mode.

Long Time Recording

PCM-1630
DMR-4000
BVU-800DB



2.3.4 DMR-4000/DMR-2000/PCM-1630

SETTING OF DMR-2000 (1st RECORDER)

-Front Panel

.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------FREE RUN
.MEMORY switch--------------------OFF

-Rear Panel

.NDF/DF selector------use NDF for CD Mastering, DF may be used for conformance to 44.056kHz Fs

SETTING OF DMR-4000 (2nd RECORDER)

-Front Panel

.TRACKING control----------FIXED
.METER selector------------selects main (R/P) or confidence (CONFI) video signals
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------MAIN
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------REGEN
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector--------insignificant
.AUX MONITOR selector-----------------------insignificant
.PB/PB/EE selector----PB/EE(fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)--ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector-------select the position according to the 1st RECORDER

-DM-49 Board

.Composite Digital Output switch----OFF(NORMAL)

NOTE: When the 2nd RECORDER is in record mode, the CONFI signal of the 2nd RECORDER can be monitored.

SETTING OF PCM-1630

-Front Panel

.ENC IN selector------------------ANALOG
.DA IN selector-------------------INT
.MUTE indication mode selector---selects the MUTE indicator LED mode of operation. The LED can be illuminated momentarily when a mute condition exists (NORMAL) or remain continuously lit until reset by way of the switch (HOLD). For most critical applications use MUTE HOLD mode.
.MONITOR selector-----------------PB
.PB MODE selector-----------------A
.SCALE selector-------------------NORMAL
.PEAK indication mode selector---selects PEAK HOLD or NORMAL mode affecting only the meter display. For most critical applications use the PEAK HOLD mode (set PEAK OVER HOLD).

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---selects EMPHASIS, this is set subjectively according to the program material. If EMPHASIS is changed between selections on a CD, there must be a 2 second pause (silence) in the program.

-ENC-2 Board

.REC MUTE switch---------------------OFF

-SIF-1 Board

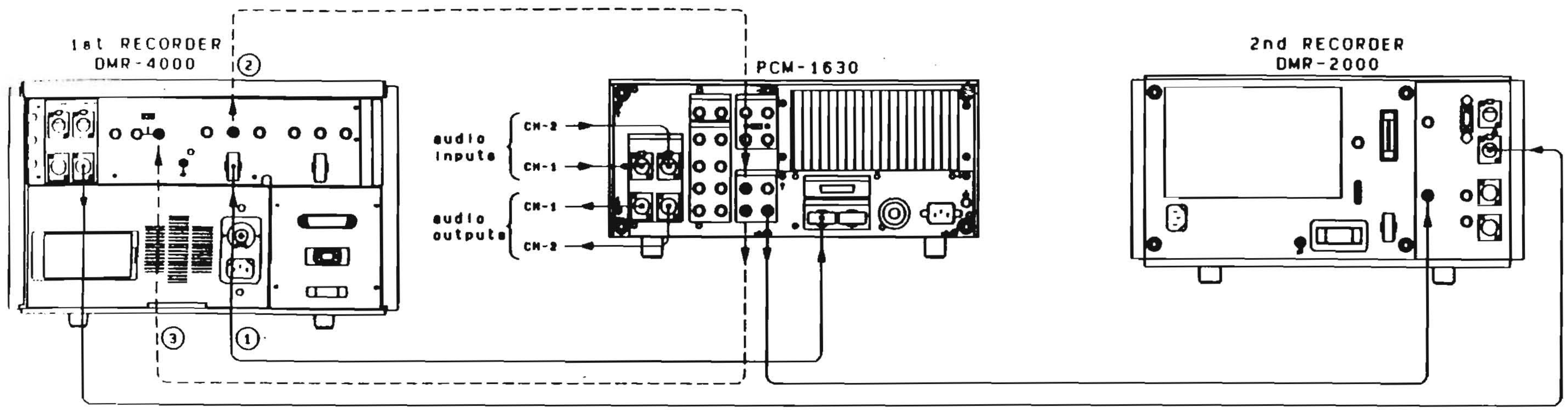
.Fs selector---use 44.1kHz for CD mastering (44.056kHz can be used if required (conform to color video, previous program material, or DF time code).

-MT-16 Board

.PEAK HOLD switch---selects the metering mode. It is recommended to use the PEAK OVER HOLD mode, where the OVER LEDs remain illuminated until reset. In this mode, an overlevel condition can be detected even if the user does not continuously watch the meter.

Long Time Recording

PCM-1630
DMR-4000
DMR-2000



2.3.5 DMR-2000/PCM-1630

SETTING OF DMR-2000 (1st RECORDER)

-Front Panel

```
.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------FREE RUN
.MEMORY switch--------------------OFF
```

-Rear Panel

```
.NDF/DF selector------use NDF for CD Mastering, DF may be
                      used for conformance to 44.056kHz Fs
                      or color video frame rate
```

SETTING OF DMR-2000 (2nd RECORDER)

-Front Panel

```
.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------REGEN
.MEMORY switch--------------------OFF
```

-Rear Panel

```
.NDF/DF selector------------------select the position according to
                                  the 1st RECORDER (same setting)
```

SETTING OF PCM-1630

-Front Panel

```
.ENC IN selector------------------ANALOG
.DA IN selector-------------------INT
.MUTE indication mode selector---selects the MUTE indicator LED
                                 mode of operation.  The LED
                                 can be illuminated momentarily
                                 when a mute condition exists
                                 (NORMAL) or remain
                                 continuously lit until reset
                                 by way of the switch (HOLD).
                                 For most critical applications
                                 use MUTE HOLD mode.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL
.PEAK indication mode selector---selects PEAK HOLD or NORMAL
                                 mode affecting only the meter
                                 display.  For most critical
                                 applications use the PEAK HOLD
                                 mode (set PEAK OVER HOLD).
```

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---selects EMPHASIS, this is set subjectively according to the program material. If EMPHASIS is changed between selections on a CD, there must be a 2 second pause (silence) in the program.

-ENC-2 Board

.REC MUTE switch--------------------OFF

-SIF-1 Board

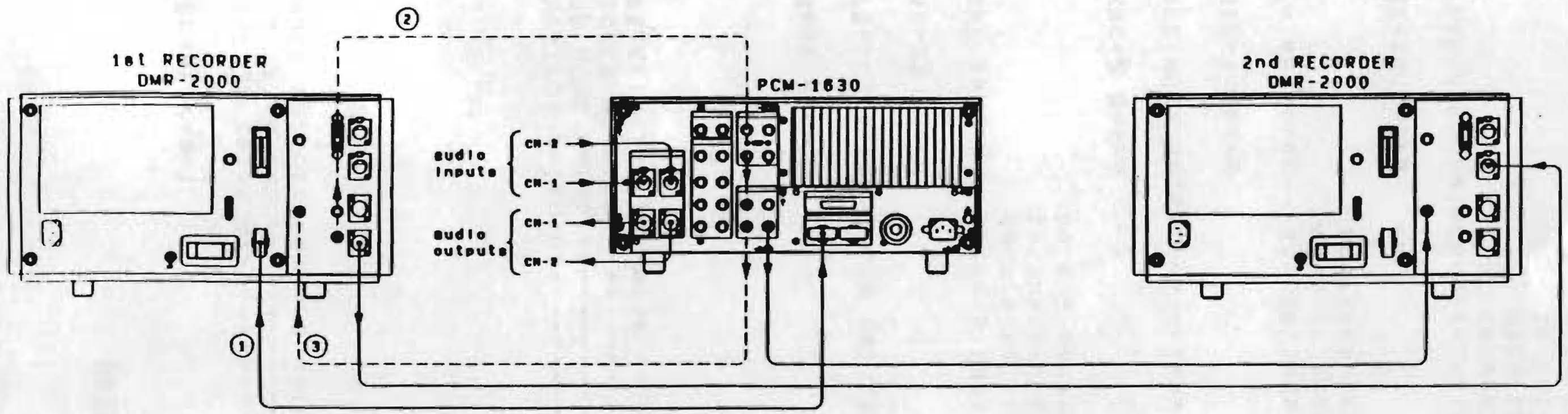
.Fs selector---use 44.1kHz for CD mastering (44.056kHz can be used if required (conform to color video, previous program material, or DF time code).

-MT-16 Board

.PEAK HOLD switch---selects the metering mode. It is recommended to use the PEAK OVER HOLD mode, where the OVER LEDs remain illuminated until reset. In this mode, an overlevel condition can be detected even if the user does not continuously watch the meter.

Long Time Recording

PCM-1630
DMR-2000
DMR-2000



2.3.6 DMR-2000/BVU-800DB/PCM-1630

SETTING OF DMR-2000 (1st RECORDER)

-Front Panel

.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------FREE RUN
.MEMORY switch--------------------OFF

-Rear Panel

.NDF/DF selector------use NDF for CD Mastering, DF may be used for conformance to 44.056kHz Fs or color video frame rate

SETTING OF BVU-800DB (2nd RECORDER)

-Front Panel

.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL
.VIDEO INPUT SELECT switch-----------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2(36P)
.PB-PB/EE selector-------------------PB/EE
.REMOTE/LOCAL selector---------------LOCAL

fixed with switch protectors

-Rear Panel

.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--ON

SETTING OF PCM-1630

-Front Panel

```
.ENC IN selector-----------------ANALOG
.DA IN selector------------------INT
.MUTE indication mode selector---selects the MUTE indicator LED
                                 mode of operation.  The LED
                                 can be illuminated momentarily
                                 when a mute condition exists
                                 (NORMAL) or remain
                                 continuously lit until reset
                                 by way of the switch (HOLD).
                                 For most critical applications
                                 use MUTE HOLD mode.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL
.PEAK indication mode selector---selects PEAK HOLD or NORMAL
                                 mode affecting only the meter
                                 display.  For most critical
                                 applications use the PEAK HOLD
                                 mode (set PEAK OVER HOLD).
```

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---selects EMPHASIS, this is set subjectively according to the program material. If EMPHASIS is changed between selections on a CD, there must be a 2 second pause (silence) in the program.

-ENC-2 Board

.REC MUTE switch--------------------OFF

-SIF-1 Board

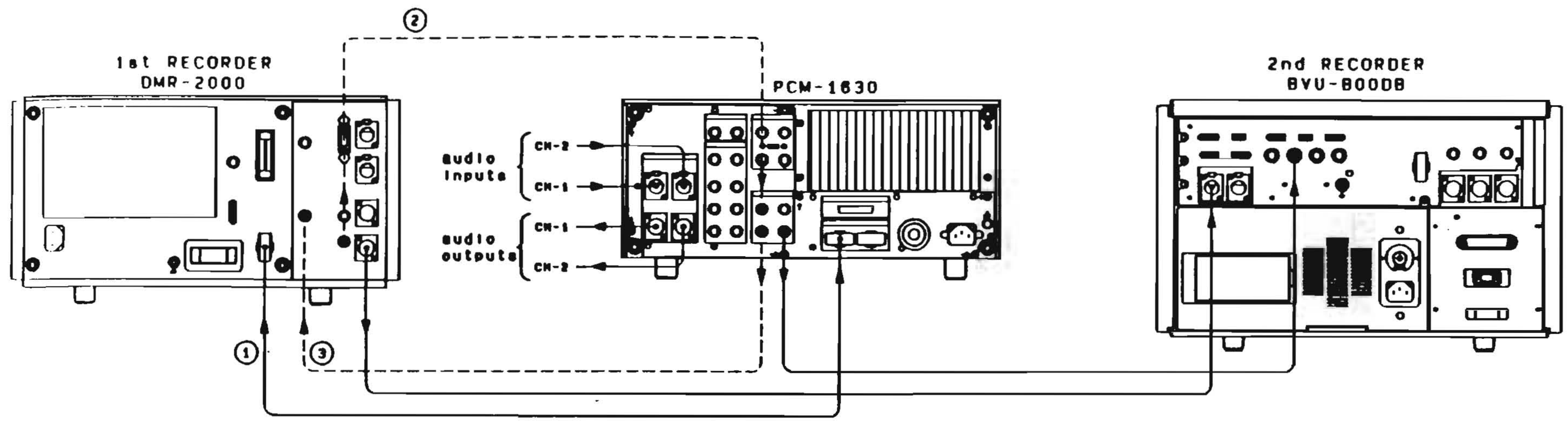
.Fs selector---use 44.1kHz for CD mastering. 44.056kHz can be used if required (conform to color video, previous program material, or DF time code).

-MT-16 Board

.PEAK HOLD switch---selects the metering mode. It is recommended to use the PEAK OVER HOLD mode, where the OVER LEDs remain illuminated until reset. In this mode, an overlevel condition can be detected even if the user does not continuously watch the meter.

Long Time Recording

PCM-1630
DMR-2000
BVU-800DB



2.3.7 DMR-4000/PCM-1610

SETTING OF DMR-4000 (1st RECORDER)

-Front Panel

.TRACKING control----------FIXED
.METER selector------------selects main (R/P) or confidence
(CONFI) video signals to video meter
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------MAIN
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------FREE RUN
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---------insignificant
.AUX MONITOR selector------------------------insignificant
.PB/PB/EE selector---------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---use NDF for CD Mastering, DF may be
used for conformance to 44.056kHz Fs

-DM-49 Board

.Composite Digital Output switch---OFF(normal)

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch-------insignificant
.MONITOR/METER switch--------------PB
.MUTING mode selector--------------selects the muting mode
.D/A INPUT selector----------------INTERNAL
.A/D INPUT selector----------------ANALOG

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---selects EMPHASIS, this is set subjectively according to the program material. If EMPHASIS is changed between selections on a CD, there must be a 2 second pause (silence) in the program.

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---use 44.1kHz for CD mastering (44.056kHz can be used if required (conform to color video, previous program material, or DF time code).

SETTING OF DMR-4000 (2nd RECORDER)

-Front Panel

.TRACKING control----------FIXED
.METER selector------------selects main (R/P) or confidence (CONFI) video signals
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------MAIN
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------REGEN
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector--------insignificant
.AUX MONITOR selector-----------------------insignificant
.PB/PB/EE selector----PB/EE(fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)--ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector-------select the position according to the 1st RECORDER

-DM-49 Board

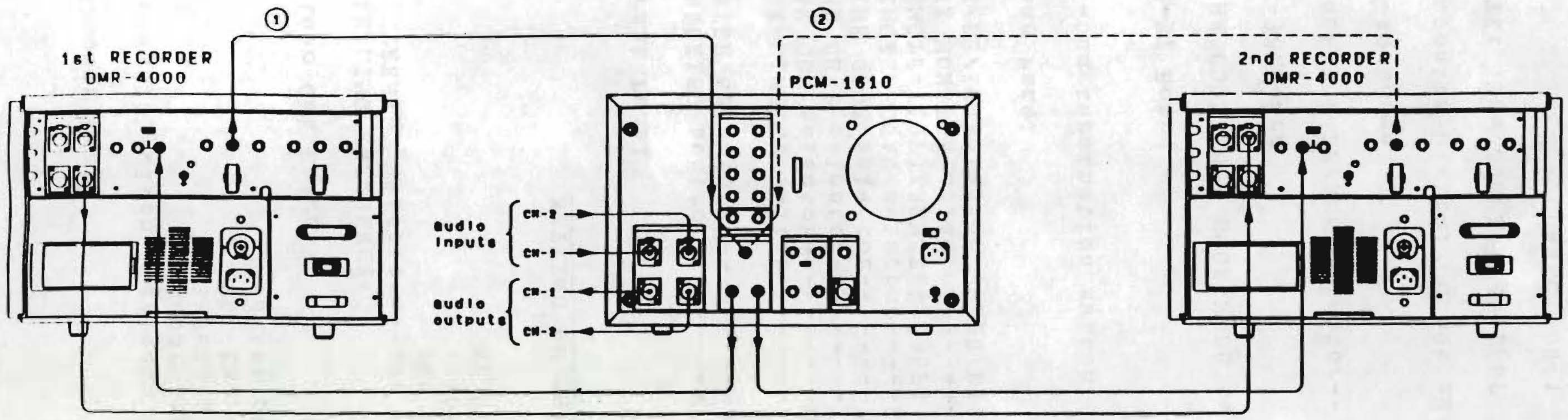
.Composite Digital Output switch----OFF(NORMAL)

NOTE: The CONFI signal of 1st or 2nd RECORDER can be monitored:

CONNECTION 1 -- 1st RECORDER
CONNECTION 2 -- 2nd RECORDER
(refer to Figure 2-16)

Long Time Recording

PCM-1610
DMR-4000
DMR-4000



2.3.8 DMR-4000/DMR-2000/PCM-1610

SETTING OF DMR-4000 (1st RECORDER)

-Front Panel

```
.TRACKING control----------FIXED
.METER selector------------selects main (R/P) or confidence
                           (CONFI) video signals to video meter
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------MAIN
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------FREE RUN
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---------insignificant
.AUX MONITOR selector------------------------insignificant
.PB/PB/EE selector---------PB/EE (fixed with a switch protector)
```

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

```
.GENERATOR DF/NDF selector---use NDF for CD Mastering, DF may be
                             used for conformance to 44.056kHz Fs
```

-DM-49 Board

.Composite Digital Output switch---OFF(normal)

SETTING OF PCM-1610

-Front Panel

```
.TIME CODE GENERATOR switch-------insignificant
.MONITOR/METER switch-------------PB
.MUTING mode selector-------------selects the muting mode
.D/A INPUT selector---------------INTERNAL
.A/D INPUT selector---------------ANALOG
```

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---selects EMPHASIS, this is set subjectively according to the program material. If EMPHASIS is changed between selections on a CD, there must be a 2 second pause (silence) in the program.

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---use 44.1kHz for CD mastering (44.056kHz can be used if required (conform to color video, previous program material, or DF time code).

SETTING OF DMR-2000 (2nd RECORDER)

-Front Panel

.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------REGEN
.MEMORY switch--------------------OFF

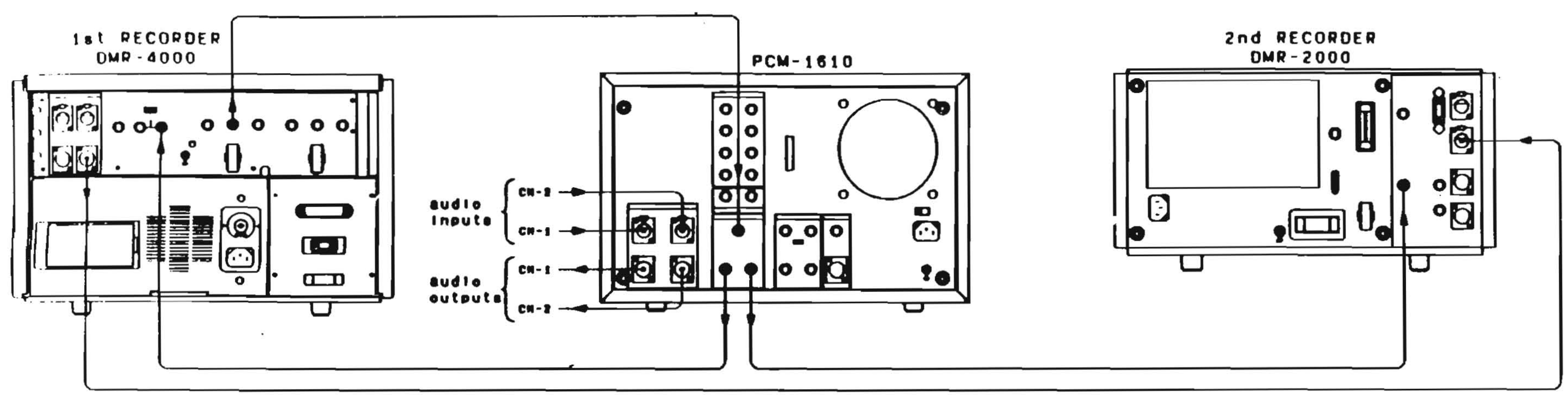
-Rear Panel

.NDF/DF selector-------------select the position according to the 1st RECORDER (same setting)

NOTE: When the 1st RECORDER is in RECORD mode, the CONFI signal of the 1st RECORDER can be monitored through the **PCM-1610** providing a playback signal derived from the confidence playback head installed in the **DMR-4000**.

Long Time Recording

PCM-1610
DMR-4000
DMR-2000



2.3.9 DMR-4000/BVU-800DB/PCM-1610

SETTING OF DMR-4000 (1st RECORDER)

-Front Panel

.TRACKING control----------FIXED
.METER selector------------selects main (R/P) or confidence (CONFI) video signals to video meter
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------MAIN
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------FREE RUN
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---------insignificant
.AUX MONITOR selector------------------------insignificant
.PB/PB/EE selector---------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---use NDF for CD Mastering, DF may be used for conformance to 44.056kHz Fs

-DM-49 Board

.Composite Digital Output switch---OFF(normal)

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch-------insignificant
.MONITOR/METER switch-------------PB
.MUTING mode selector-------------selects the muting mode
.D/A INPUT selector---------------INTERNAL
.A/D INPUT selector---------------ANALOG

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---selects EMPHASIS, this is set subjectively according to the program material. If EMPHASIS is changed between selections on a CD, there must be a 2 second pause (silence) in the program.

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---use 44.1kHz for CD mastering (44.056kHz can be used if required (conform to color video, previous program material, or DF time code).

SETTING OF BVU-800DB (2nd RECORDER)

-Front Panel

.TRACKING control---------------------FIXED
.TIME CODE switch---------------------TC TRACK
.AUDIO MONITOR selector---------------insignificant
.AUDIO LIMITER switch-----------------insignificant
.MIXING SELECT switch-----------------OFF
.MODE SELECT switch-------------------NORMAL
.VIDEO INPUT SELECT switch------------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2(36P)
.PB-PB/EE selector--------------------PB/EE
.REMOTE/LOCAL selector----------------LOCAL

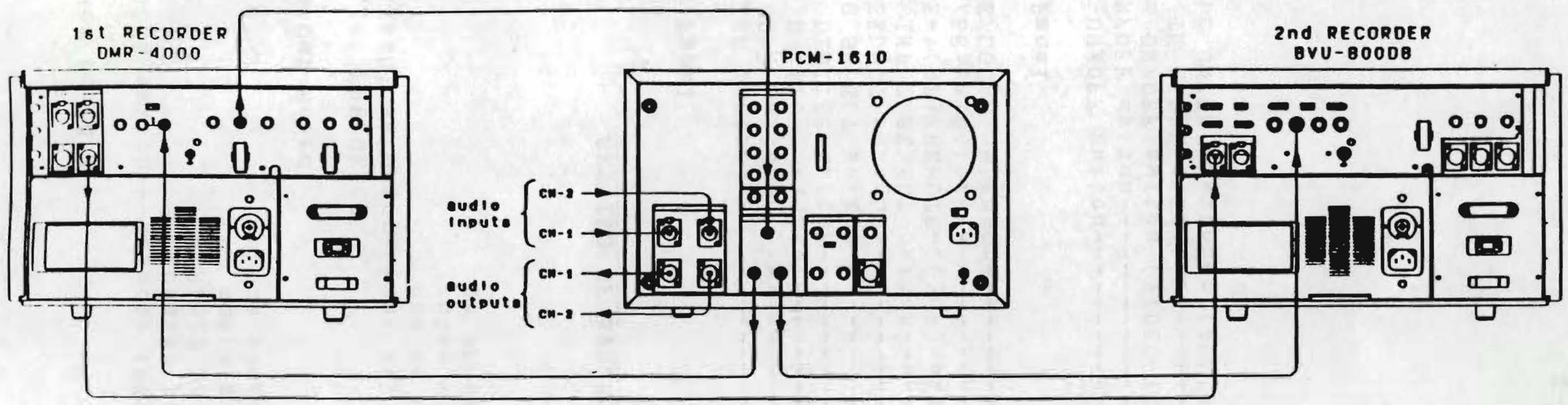
fixed with switch protectors

-Rear Panel

.COLOR ON/OFF switch------------------OFF
.DOC ON/OFF switch--------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors-------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--ON

Long Time Recording

PCM-1610
DMR-4000
BVU-800DB



2.3.10 DMR-2000/DMR-4000/PCM-1610

SETTING OF DMR-2000 (1st RECORDER)

-Front Panel

```
.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------FREE RUN
.MEMORY switch--------------------OFF
```

-Rear Panel

```
.NDF/DF selector---use NDF for CD Mastering, DF may be used for
                   conformance to 44.056kHz Fs or color video
```

SETTING OF PCM-1610

-Front Panel

```
.TIME CODE GENERATOR switch-------------insignificant
.MONITOR/METER switch-------------------PB
.MUTING mode switch---------------------select the position according
                                        to the desired muting mode
.D/A INPUT selector---------------------INTERNAL
.A/D INPUT selector---------------------ANALOG
```

-Rear Panel

```
.75-ohm termination switch
     (COMPOSITE SYNC INPUT)-------------insignificant
```

-Encoder Board

```
.EMPHASIS switch---selects EMPHASIS, this is set subjectively
                   according to the program material.  If
                   EMPHASIS is changed between selections on a
                   CD, there must be a 2 second pause (silence)
                   in the program.
```

-Video Out Board

```
.SAMPLING FREQUENCY
 (INTERNAL) selector---use 44.1kHz for CD mastering.  44.056kHz
                       can be used if required (conform to
                       color video, previous program material,
                       or DF time code).
```

SETTING OF DMR-4000 (2nd RECORDER)

-Front Panel

.TRACKING control----------FIXED
.METER selector------------selects main (R/P) or confidence (CONFI) video signals
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------MAIN
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------REGEN
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector--------insignificant
.AUX MONITOR selector-----------------------insignificant
.PB/PB/EE selector----PB/EE(fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)--ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector-------select the position according to the 1st RECORDER

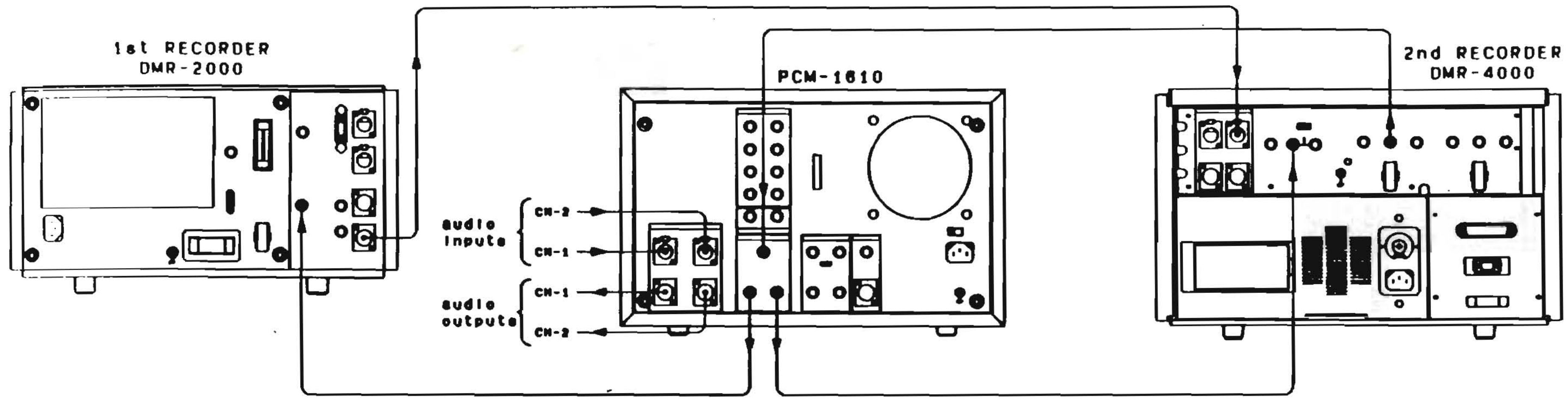
-DM-49 Board

.Composite Digital Output switch----OFF(NORMAL)

NOTE: When the 2nd RECORDER is in record mode, the CONFI signal of the 2nd RECORDER can be monitored through the **PCM-1610**. When this is done, the playback audio is derived from the confidence heads providing a signal which has been recorded then played back from the confidence head.

Long Time Recording

PCM-1610
DMR-2000
DMR-4000



2.3.11 DMR-2000/PCM-1610

SETTING OF DMR-2000 (1st RECORDER)

-Front Panel

.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------FREE RUN
.MEMORY switch--------------------OFF

-Rear Panel

.NDF/DF selector---use NDF for CD Mastering, DF may be used for conformance to 44.056kHz Fs or color video

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch------insignificant
.MONITOR/METER switch------------PB
.MUTING mode switch--------------select the position according to the desired muting mode
.D/A INPUT selector--------------INTERNAL
.A/D INPUT selector--------------ANALOG

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---set subjectively according to the program material. If EMPHASIS is changed between selections on a CD, there must be a 2 second pause (silence).

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---use 44.1kHz for CD mastering (44.056kHz can be used if required).

SETTING OF DMR-2000 (2nd RECORDER)

-Front Panel

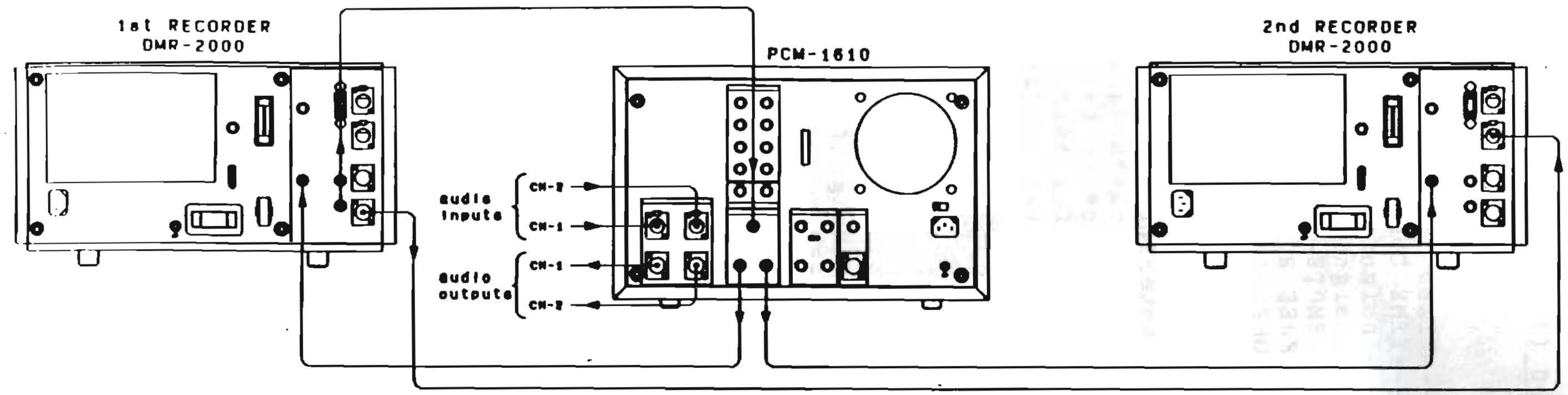
.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------REGEN
.MEMORY switch--------------------OFF

-Rear Panel

.NDF/DF selector----same as the 1st RECORDER

Long Time Recording

PCM-1610
DMR-2000
DMR-2000



2.3.12 DMR-2000/BVU-800DB/PCM-1610

SETTING OF DMR-2000 (1st RECORDER)

-Front Panel

.TRACKING CONTROL------------------FIXED
.CH-2 switch-----------------------TIME CODE
.AUX LIMITER switch----------------insignificant
.MONITOR SELECT switch-------------insignificant
.REMOTE/LOCAL switch---------------REMOTE-2/LOCAL
.TIME CODE mode selector-----------FREE RUN
.MEMORY switch---------------------OFF

-Rear Panel

.NDF/DF selector---use NDF for CD mastering purposes. DF may be used where the previous program material dictates, for conformance to 44.056kHz sampling frequency, or for conformance to color video frame rate (it is not acceptable for CD masters).

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch--------------insignificant
.MONITOR/METER switch--------------------PB
.MUTING mode switch----------------------select the position according to the the desired muting mode (inconsequential to the recording process)
.D/A INPUT selector----------------------INTERNAL
.A/D INPUT selector----------------------ANALOG

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)------insignificant

-Encoder Board

.EMPHASIS switch---set subjectively for the program material being recorded. For CD purposes, a change in the EMPHASIS mode between selections must be accompanied by a 2 second pause (silence) in the program material.

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector--use 44.1kHz for CD mastering purposes. 44.056kHz may be used if required for matching to previous program material or for conformance to color frame rate or drop frame time code.

SETTING OF BVU-800DB (2nd RECORDER)

-Front Panel

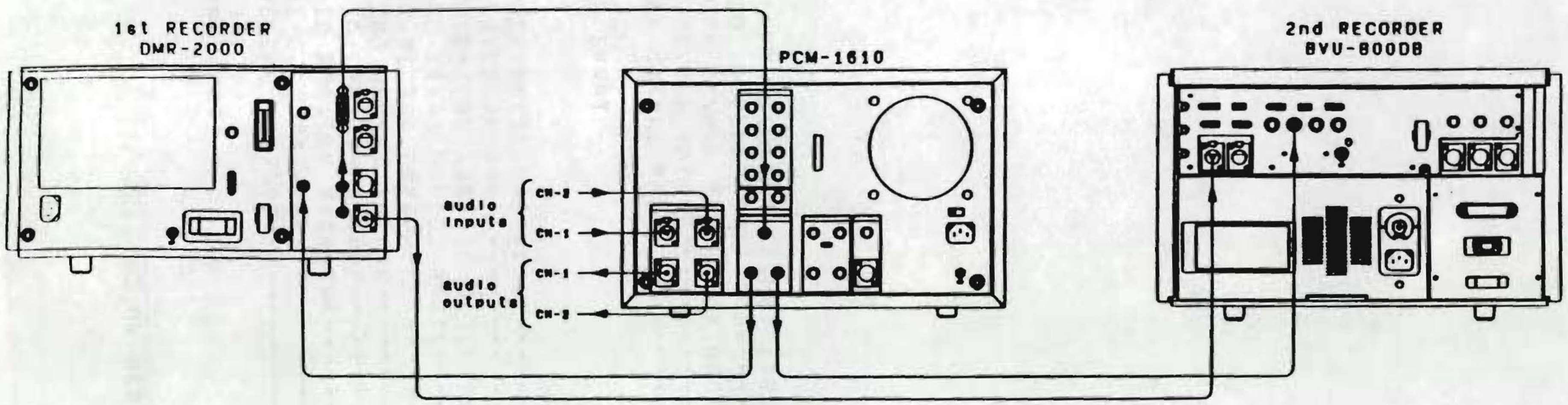
.TRACKING control---------------------	FIXED	
.TIME CODE switch---------------------	TC TRACK	
.AUDIO MONITOR selector---------------	insignificant	
.AUDIO LIMITER switch-----------------	insignificant	
.MIXING SELECT switch-----------------	OFF	
.MODE SELECT switch-------------------	NORMAL	fixed with
.VIDEO INPUT SELECT switch------------	LINE	switch
.REMOTE-1(9P)/REMOTE-2(36P)selector--	REMOTE-2(36P)	protectors
.PB-PB/EE selector--------------------	PB/EE	
.REMOTE/LOCAL selector----------------	LOCAL	

-Rear Panel

.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--ON

Long Time Recording

PCM-1610
DMR-2000
BVU-800DB



2.4.1 DMR-4000/PCM-1630 (DABK-1630)

SETTING OF DMR-4000 (PLAYER)

-Front Panel

.TRACKING control-----------------FIXED
.METER selector-------------------R/P
.AUX LIMITER switch---------------insignificant
.RAW OUT selector-----------------insignificant
.AUX CH-2 selector----------------TIME CODE
.TIME CODE selector---------------REC RUN
.REMOTE/LOCAL selector------------LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector------insignificant
.AUX MONITOR selector---------------------insignificant
.PB/PB/EE selector---PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)--------insignificant

-TC-38 Board

.GENERATOR DF/NDF selector-------------------insignificant

-DM-49 Board

.Composite Digital Output switch-------------OFF (NORMAL)

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DUBBING
.DA IN selector------------------INT
.MUTE indication mode selector---sets the MUTE indicator LED mode (inconsequential to the recording process). Use HOLD to check for mutes during the program.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL
.PEAK indication mode selector---selects the metering mode. HOLD mode is recommended for critical applications.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---insignificant (EMPHASIS determined by the tape playback data)

-ENC-2 Board

.REC MUTE switch------------------OFF (will mute the recording if in the ON position).

-SIF-1 Board

.Fs selector---select the position according FsID indicator so that the selected sampling frequency is the same as the sampling frequency of the digital audio data on the tape.

-MT-16 Board

.PEAK HOLD switch---this sets the metering mode and is inconsequential to the recording process. It is usually recommended to use PEAK OVER HOLD mode for the most critical applications as this will cause the OVER LEDs to remain illuminated until reset if an overlevel condition occurs.

SETTING OF DABK-1630

.RAW switch------------------------DUB

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. If the MANUAL mode is used, the RUN switch is used to print a header, the START switch is used to start the recorder error analysis routine, and the STOP switch is used to stop error analysis and rewind the tape.

SETTING OF DMR-4000 (2nd RECORDER)

-Front Panel

```
.TRACKING control----------FIXED
.METER selector------------select the position according
                                  to the use
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------insignificant
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------REC RUN (not dubbing time code)
                           REGEN (when dubbing time code)
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector----insignificant
.AUX MONITOR selector-------------------insignificant
.PB/PB/EE selector----PB/EE (fixed with a switch protector)
```

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

```
.TIME CODE AUTO STOP MODE switch (S1)---use AUTO STOP with REC RUN
                                        insignificant in REGEN
```

-TC-38 Board

.GENERATOR DF/NDF selector---set for same as PLAYER time code

-DM-49 Board

.Composite Digital Output switch--OFF(NORMAL)

NOTES
(refer to Figure 2-23)

When dubbing the TIME CODE with the DIGITAL AUDIO signal, make the connection a.

The DUBBING RAW function is possible when installing the **DABK-1630** into the **PCM-1630** and making the conneciton 4.

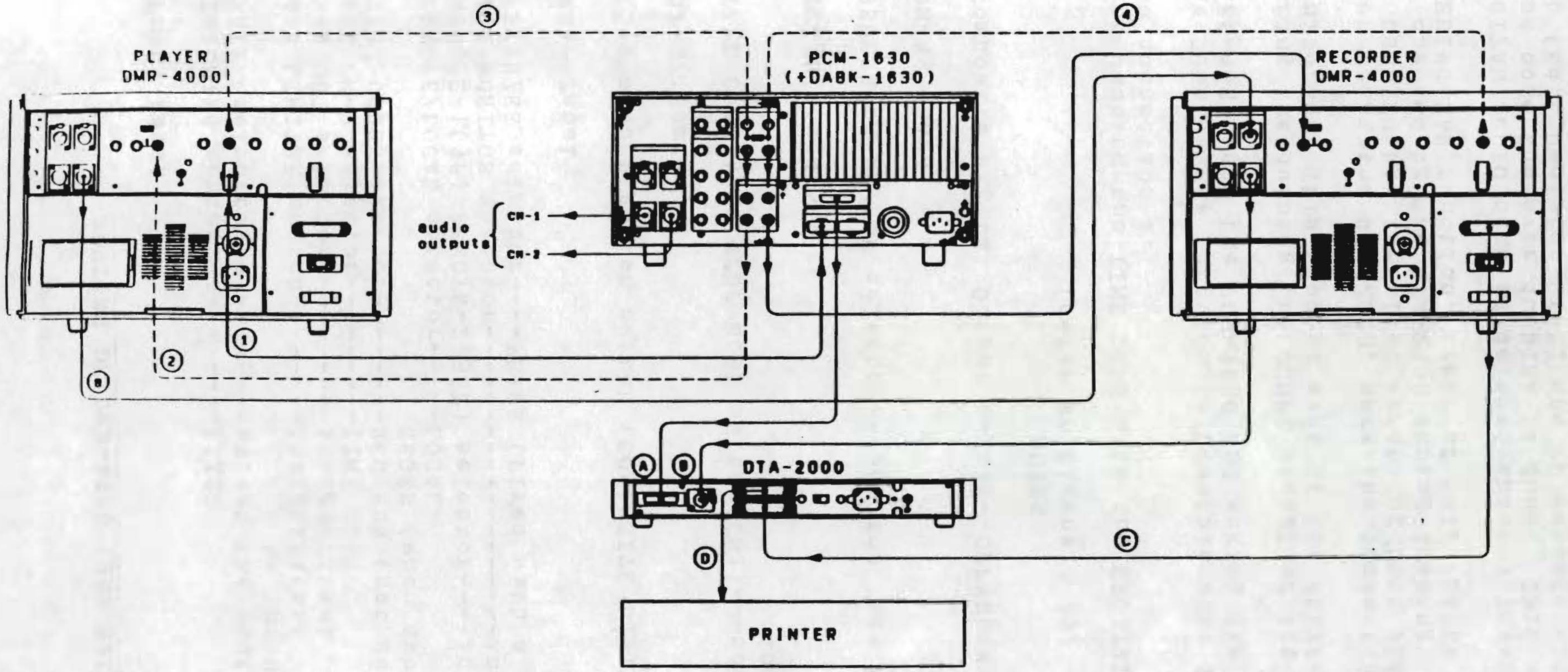
During the dubbing the CONFI signal of the RECORDER is monitored. This happens even if the PLAYER is not a **DMR-4000**.

When using the **DTA-2000**, make the connections A - D.
By DUBBING RAW function, errors of both PLAYER AND RECORDER can be checked by the **DTA-2000** during dubbing. (Without the DUBBING RAW function, error of only PLAYER can be checked)

DIGITAL AUDIO data is delayed about 9.7msec with respect to the time code whenever dubbing is done. This will affect written EDL (Edit Decision List) and PQ subcode accuracy.

DIGITAL DUBBING

PCM-1630(+DABK-1630)
DMR-4000
(Featuring the Dubbing RAW Function)



2.4.2 DMR-4000/PCM-1630/DTA-2000

SETTING OF DMR-4000 (1st RECORDER)

-Front Panel

.TRACKING control---------FIXED
.METER selector-----------selects the video meter signal source. R/P selects the main video heads (input video in RECORD). CONFI selects the confidence heads and this will always be a playback signal from the tape.
.AUX LIMITER switch-------insignificant
.RAW OUT selector---------insignificant
.AUX CH-2 selector--------TIME CODE
.TIME CODE selector-------REC RUN
.REMOTE/LOCAL selector----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---insignificant
.AUX MONITOR selector-----------------insignificant
.PB/PB/EE selector--------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)-----ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)----------------------------insignificant (time code generator not used by the player)

-TC-38 Board

.GENERATOR DF/NDF selector-------insignificant (time code generator is inactive on player)

-DM-49 Board

.Composite Digital Output switch----------OFF (NORMAL)

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DUBBING
.DA IN selector------------------INT
.MUTE indication mode selector--sets the MUTE indicator LED mode of operation. It is recommended to use HOLD so that the mute LED does not reset upon detection of a mute.
.MONITOR selector----------------PB
.PB MODE selector----------------RAR (with **DABK-1630**)
A (without **DABK-1630**)
.SCALE selector------------------NORMAL
.PEAK indication mode selector--selects the metering mode. For the most critical applications, use PEAK HOLD.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---------insignificant (EMPHASIS mode is controlled by the digital audio data on the PLAYER tape

-ENC-2 Board

.REC MUTE switch----OFF (if set to ON no recording will occur)

-SIF-1 Board

.Fs selector--------select the position according to the FsID indicator. This is set so that it is the same as the sampling frequency on the PLAYER tape.

-MT-16 Board

.PEAK HOLD switch---selects the metering mode only. This does not affect the recording process. It is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to warn the operator that overlevel has occurred.

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind the tape.

SETTING OF DMR-4000 (2nd RECORDER)

-Front Panel

```
.TRACKING control-----------FIXED
.METER selector------------select the position according
                                  to the use
.AUX LIMITER switch--------insignificant
.RAW OUT selector----------insignificant
.AUX CH-2 selector---------TIME CODE
.TIME CODE selector--------REC RUN (not dubbing time code)
                           REGEN (when dubbing time code)
.REMOTE/LOCAL selector-----LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---insignificant
.AUX MONITOR selector------------------insignificant
.PB/PB/EE selector-------PB/EE (fixed with a switch protector)
```

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

```
.TIME CODE AUTO STOP MODE switch (S1)---use AUTO STOP with REC RUN
                                        insignificant in REGEN
```

-TC-38 Board

.GENERATOR DF/NDF selector---set for same as PLAYER time code

-DM-49 Board

.Composite Digital Output switch-----OFF (NORMAL)

NOTES
(refer to Figure 2-24)

When dubbing the TIME CODE with the DIGITAL AUDIO signal, make the connection a.

The RAR function is possible when installing the **DABK-1630** into the **PCM-1630** and making the connection 4. (The RECORDER does not need to be the **DMR-4000** for this function.)

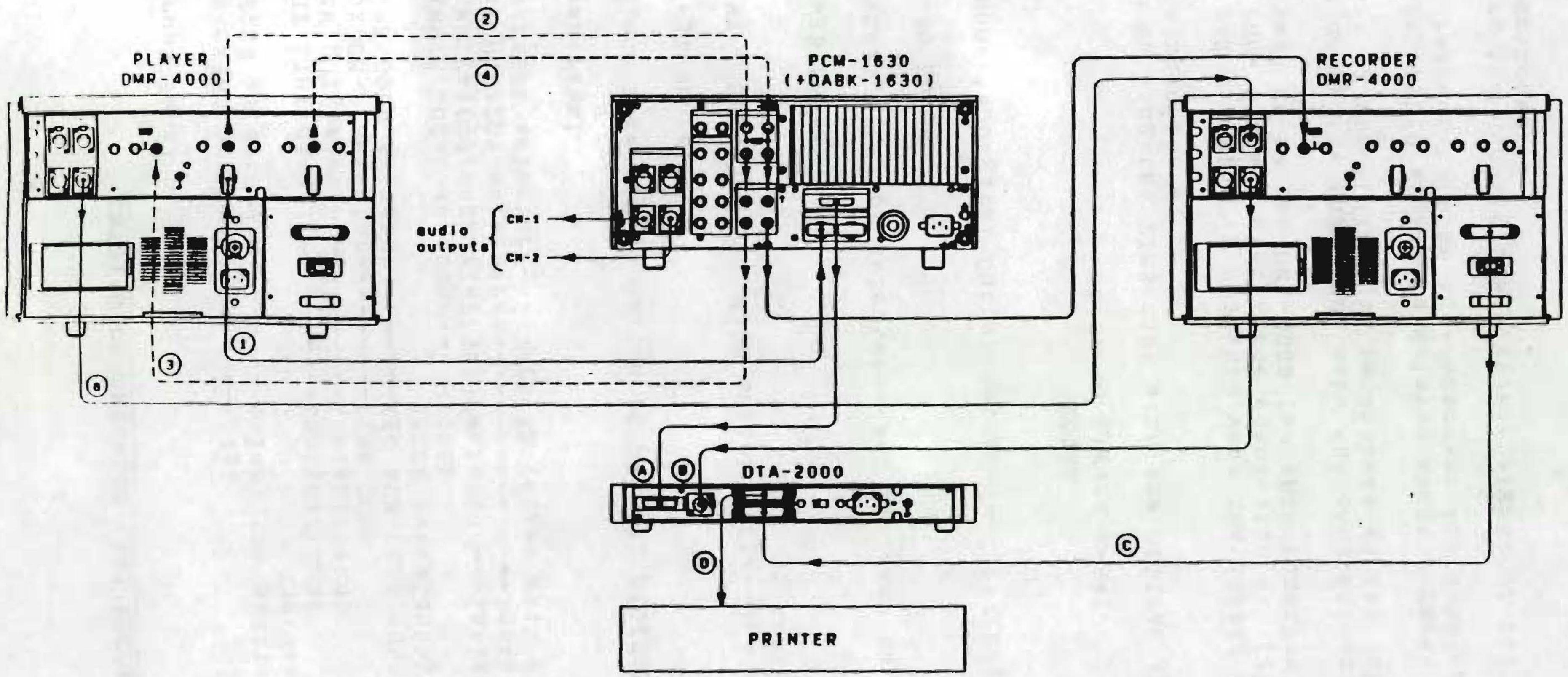
When using the **DTA-2000**, make the connections A - D. The errors of the PLAYER can be checked during dubbing.

DIGITAL AUDIO signal is delayed about 9.7msec (14.4msec when RAR) with respect to time code whenever the dubbing is done.

During the dubbing the playback signal of the PLAYER is monitored.

DIGITAL DUBBING

PCM-1630(+DABK-1630)
DMR-4000
(Featuring the RAR Function)



2.4.3 DMR-2000/PCM-1630/DTA-2000

SETTING OF DMR-2000 (PLAYER)

-Front Panel

.TRACKING CONTROL----------FIXED
.CH-2 switch---------------TIME CODE
.AUX LIMITER switch--------insignificant
.MONITOR SELECT switch-----insignificant
.REMOTE/LOCAL switch-------REMOTE-2/LOCAL
.TIME CODE mode selector---AUTO STOP
.MEMORY switch-------------selects the display mode
insignificant to the recording

-Rear Panel

.NDF/DF selector------------insignificant

SETTING OF DMR-2000 (RECORDER)

-Front Panel

.TRACKING CONTROL----------FIXED
.CH-2 switch---------------TIME CODE
.AUX LIMITER switch--------insignificant
.MONITOR SELECT switch-----insignificant
.REMOTE/LOCAL switch-------REMOTE-2/LOCAL
.TIME CODE mode selector---AUTO STOP (not dubbing time code)
REGEN (when dubbing time code)
.MEMORY switch-------------selects the display mode
(insignificant to the recording)

-Rear Panel

.NDF/DF selector-----------select the same position as the time code on original source tape as indicated on the PLAYER machine

NOTES
(refer to Figure 2-25)

When dubbing the TIME CODE with the DIGITAL AUDIO signal, make the connection a.

When using the **DTA-2000**, make the connections A - D. The errors of the PLAYER can be checked during dubbing.

DIGITAL AUDIO signal is delayed about 9.7msec with respect to time code whenever dubbing is done.

During the dubbing the playback signal of the PLAYER is monitored from the **PCM-1630** analog outputs.

SETTING OF PCM-1630

-Front Panel

.ENC IN selector----------------DUBBING
.DA IN selector-----------------INT
.MUTE indication mode selector--sets the MUTE indicator LED mode of operation. It is recommended to use HOLD so that the mute LED does not reset after detection of a mute.
.MONITOR selector---------------PB
.PB MODE selector---------------A
.SCALE selector-----------------NORMAL
.PEAK indication mode selector--selects the metering mode. For the most critical applications, use PEAK HOLD.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---------insignificant (EMPHASIS mode is controlled by the digital audio data on the PLAYER tape

-ENC-2 Board

.REC MUTE switch----OFF (if set to ON no recording will occur)

-SIF-1 Board

.Fs selector--------select the position according to the FsID indicator. This is set so that it is the same as the sampling frequency on the PLAYER tape.

-MT-16 Board

.PEAK HOLD switch---selects the metering mode only. This does not affect the recording process. It is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to warn the operator that overlevel has occurred.

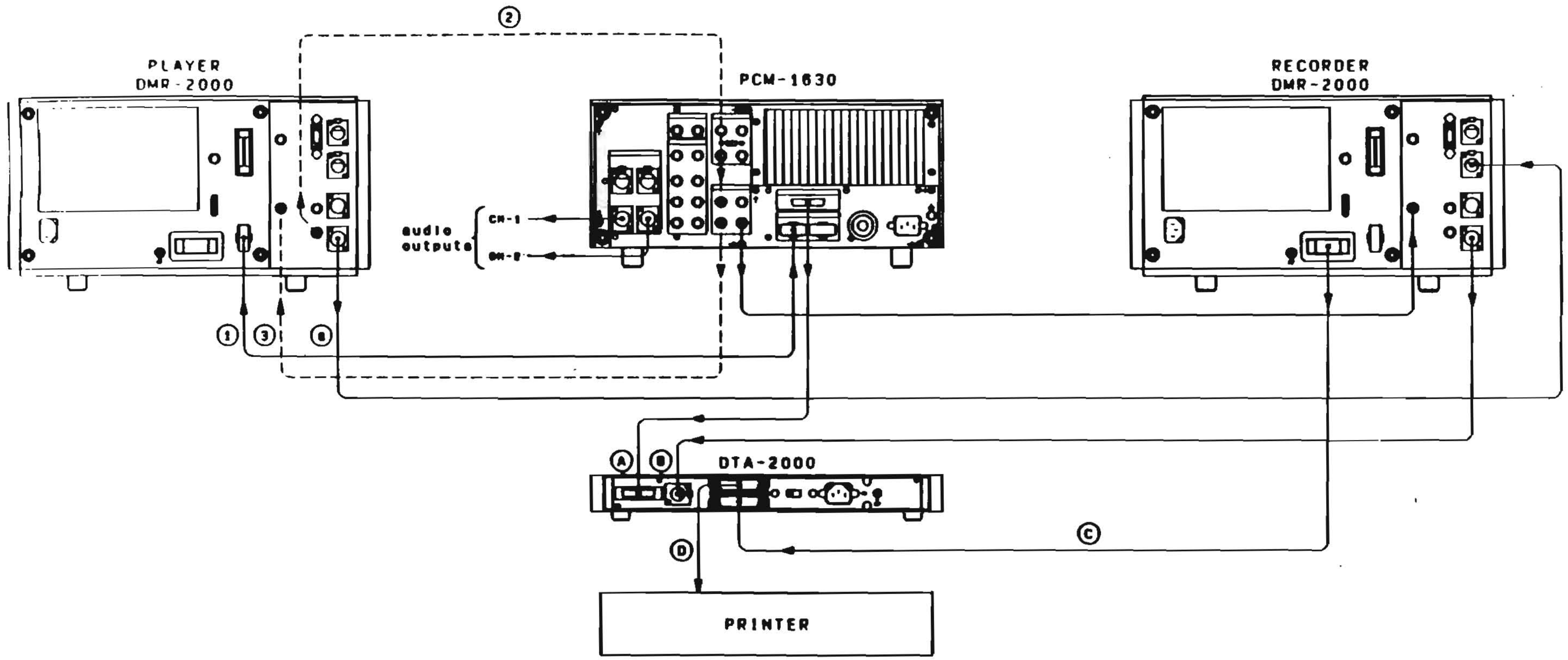
SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind the tape.

DIGITAL DUBBING

PCM-1630
DMR-2000



2.4.4 BVU-800DB/PCM-1630

SETTING OF BVU-800DB (PLAYER)

-Front Panel

.TRACKING control	FIXED	
.TIME CODE switch	TC TRACK	
.AUDIO MONITOR selector	CH-2	
.AUDIO LIMITER switch	insignificant	
.MIXING SELECT switch	OFF	
.MODE SELECT switch	NORMAL	fixed with switch protectors
.VIDEO INPUT SELECT switch	LINE	
.REMOTE-1(9P)/REMOTE-2(36P)selector	REMOTE-2(36P)	
.PB-PB/EE selector	PB/EE	
.REMOTE/LOCAL selector	LOCAL	

-Rear Panel

All rear panel switch positions are the same as for the **BVU-800DB** RECORDER (see below).

SETTING OF BVU-800DB (RECORDER)

-Front Panel

All front panel switch positions are the same as for the **BVU-800DB** PLAYER (see above).

-Rear Panel

.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75 ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--select the position according to the setting of the external TC generator (if used).

NOTES (refer to Figure 2-26)

When dubbing the TIME CODE with the DIGITAL AUDIO signal, make the connection a, b, and c.

The TIME CODE GENERATOR must have a regenerate function.

The connection c is for synchronization between the TIME CODE GENERATOR and the PROCESSOR.

When using the **DTA-2000**, make the connections A - D.
The errors of the PLAYER can be checked during dubbing.

DIGITAL AUDIO signal is delayed about 9.7msec with repect to time code whenever dubbing is done.

During the dubbing the playback signal of the PLAYER is monitored from the **PCM-1630** analog outputs.

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DUBBING
.DA IN selector------------------INT
.MUTE indication mode selector--sets the MUTE indicator LED mode of operation. It is recommended to use HOLD so that the mute LED does not reset upon detection of a mute.
.MONITOR selector---------------PB
.PB MODE selector---------------A
.SCALE selector-----------------NORMAL
.PEAK indication mode selector--selects the metering mode. For the most critical applications, use PEAK HOLD.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---------insignificant (EMPHASIS mode is controlled by the digital audio data on the PLAYER tape

-ENC-2 Board

.REC MUTE switch----OFF (if set to ON no recording will occur)

-SIF-1 Board

.Fs selector--------select the position according FsID indicator. This is set so that it is the same as the sampling frequency on the PLAYER tape.

-MT-16 Board

.PEAK HOLD switch---selects the metering mode only. This does not affect the recording process. It is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to warn the operator that overlevel has occurred.

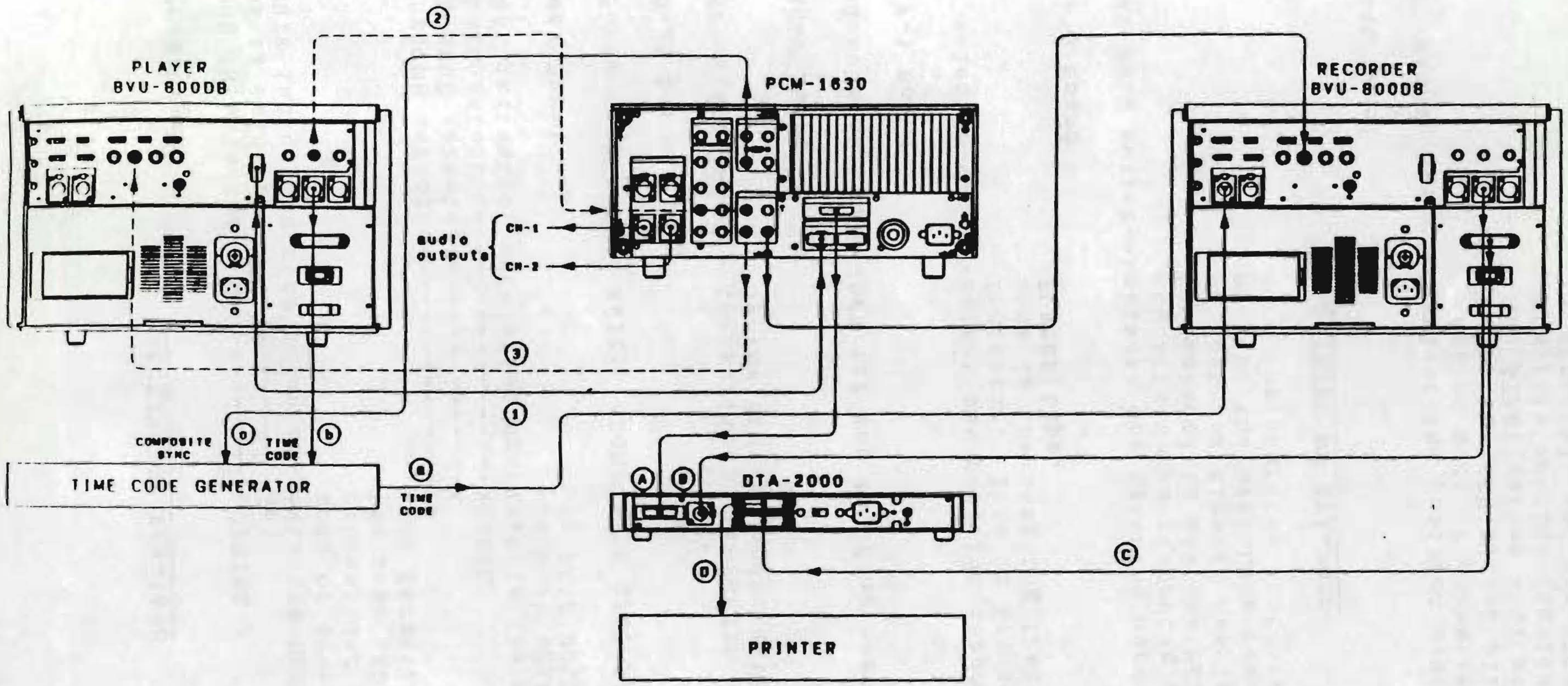
SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind the tape.

DIGITAL DUBBING

PCM-1630
BVU-800DB



2.4.5 DMR-4000/PCM-1610

SETTING OF DMR-4000 (PLAYER)

-Front Panel

.TRACKING control----------------FIXED
.METER selector------------------R/P
.AUX LIMITER switch--------------insignificant
.RAW OUT selector----------------insignificant
.AUX CH-2 selector---------------TIME CODE
.TIME CODE selector--------------FREE RUN
.REMOTE/LOCAL selector-----------LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector----insignificant
.AUX MONITOR selector-------------------insignificant
.PB/PB/EE selector-------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)-------insignificant

-TC-38 Board

.GENERATOR DF/NDF selector-------insignificant

-DM-49 Board

.Composite Digital Output switch---OFF (NORMAL)

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch--insignificant
.MONITOR/METER switch--------PB
.MUTING mode switch----------selects the MUTE indicator mode for HOLD or NORMAL (momentary)
.D/A INPUT selector----------INTERNAL
.A/D INPUT selector----------DUBBING

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---insignificant (set by PLAYER tape data)

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector-select the position according to the FsID indicator so that the the selected sampling frequency is the same as that on the PLAYER tape.

SETTING OF DMR-4000 (RECORDER)

-Front Panel

.TRACKING control---------FIXED
.METER selector-----------selects the source for the VIDEO/RF meter for main (R/P) or confidence (CONFI) head signals. CONFI is always playback from tape. R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector--------insignificant
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REC RUN (to use internal TC generator) REGEN (when dubbing time code)
.REMOTE/LOCAL selector---LOCAL
.REMOTE-1(9P)/REMOTE-2(36P)selector----insignificant
.AUX MONITOR selector-------------------insignificant
.PB/PB/EE selector------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch
(S1)------------------------------AUTO STOP mode when using REC RUN insignificant in REGEN mode

-TC-38 Board

.GENERATOR DF/NDF selector--select the position to be the same as the original source time code (see the PLAYER machine front panel indication)

-DM-49 Board

.Composite Digital Output switch-----OFF (NORMAL)

NOTES
(refer to Figure 2-27)

When dubbing the TIME CODE with the DIGITAL AUDIO signal, make the connection a.

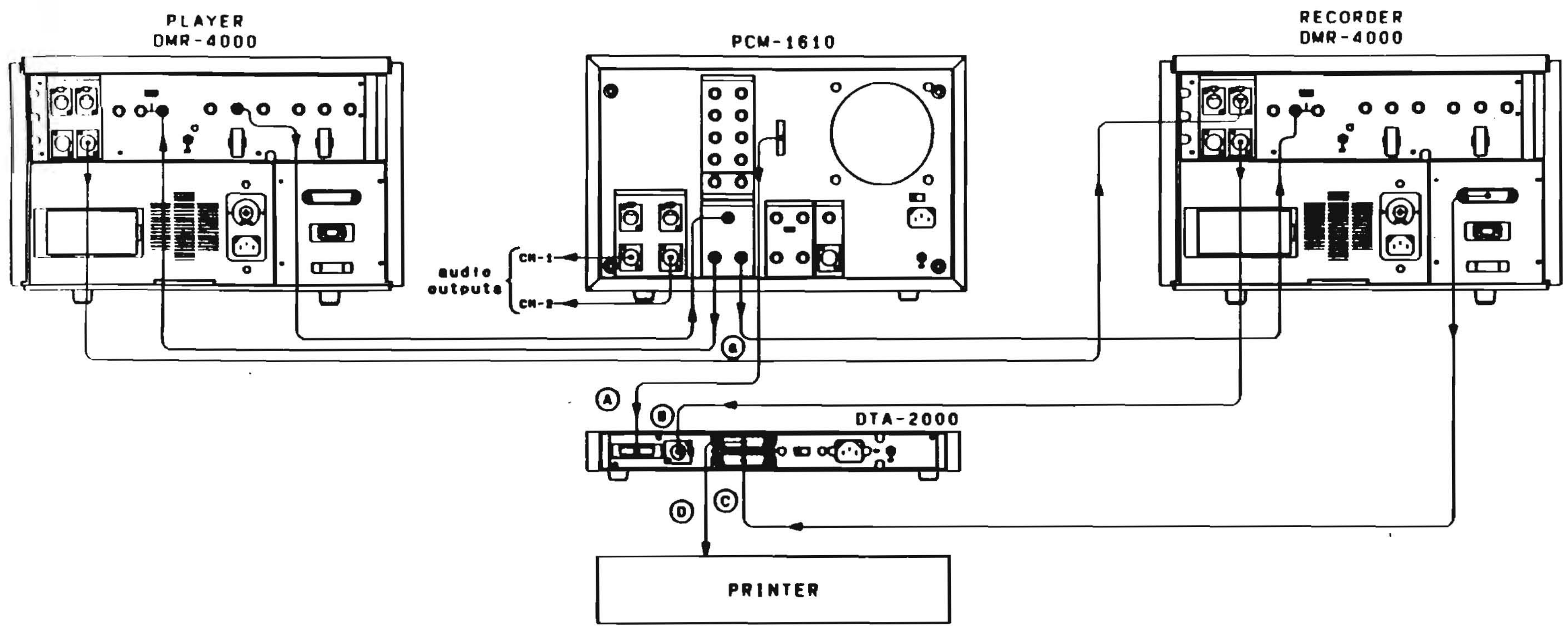
When using the **DTA-2000**, make the connections A - D. The errors of the PLAYER can be checked during dubbing.

DIGITAL AUDIO signal is delayed about 9.7msec with respect to the time code signal dubbing is done. This will affect the EDL (Edit Decision List) and PQ subcode values.

During the dubbing the playback signal of the PLAYER is monitored from the **PCM-1610** analog outputs.

DIGITAL DUBBING

PCM-1610
DMR-4000



2.4.6 DMR-2000/PCM-1610/DTA-2000

SETTING OF DMR-2000

-Front Panel

```
.TRACKING CONTROL----------FIXED
.CH-2 switch---------------TIME CODE
.AUX LIMITER switch--------insignificant
.MONITOR SELECT switch-----insignificant
.REMOTE/LOCAL switch-------REMOTE-2/LOCAL
.TIME CODE mode selector---AUTO STOP
.MEMORY switch-------------selects the display mode, does not
                           affect the recording process
```

-Rear Panel

```
.NDF/DF selector-----------insignificant
```

SETTING OF DMR-2000 (RECORDER)

-Front Panel

```
.TRACKING CONTROL----------FIXED
.CH-2 switch---------------TIME CODE
.AUX LIMITER switch--------insignificant
.MONITOR SELECT switch-----insignificant
.REMOTE/LOCAL switch-------REMOTE-2/LOCAL
.TIME CODE mode selector---AUTO STOP (when dubbing the
                                  time code REGEN)
.MEMORY switch-------------selects the display mode, does
                           not affect the recording process
```

-Rear Panel

```
.NDF/DF selector-----------set to be the same as the time code
                           on the original source tape (see the
                           front panel of the player).
```

NOTES

(refer to Figure 2-28)

When dubbing the TIME CODE with the DIGITAL AUDIO signal, make the connection a.

When using the **DTA-2000**, make the connections A - D. The errors of the PLAYER can be checked during dubbing.

DIGITAL AUDIO signal is delayed about 9.7msec with respect to the time code signal dubbing is done. This will affect the EDL (Edit Decision List) and PQ subcode values.

During the dubbing the playback signal of the PLAYER is monitored from the **PCM-1610** analog outputs.

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch----insignificant
.MONITOR/METER switch----------PB
.MUTING mode switch------------select the position according to the use
.D/A INPUT selector------------INTERNAL
.A/D INPUT selector------------DUBBING

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---insignificant (EMPHASIS mode determined by the digital audio data on the PLAYER tape)

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector-select the position according to the FsID indicator. The sampling rate will be set to be the same as the sampling rate on the PLAYER tape.

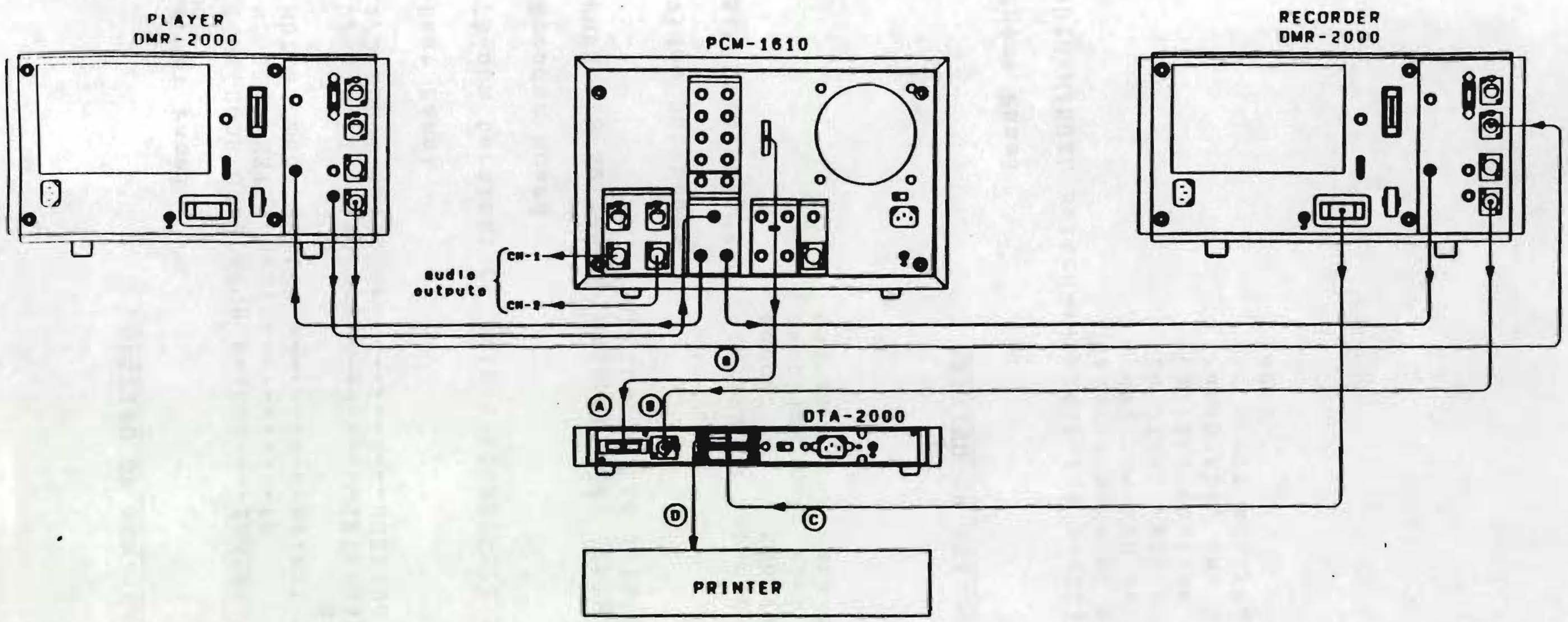
SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind the tape.

DIGITAL DUBBING

PCM-1610
DMR-2000



2.4.7 BVU-800DB/PCM-1610/DTA-2000

SETTING OF BVU-800DB (PLAYER)

-Front Panel

```
.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL          fixed with
.VIDEO INPUT SELECT switch-----------LINE              switch
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2(36P)   protectors
.PB-PB/EE selector-------------------PB/EE
.REMOTE/LOCAL selector---------------LOCAL
```

-Rear Panel

```
.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------insignificant
.600-ohm ON/OFF switches (AUDIO IN)--insignificant
```

SETTING OF PCM-1610

-Front Panel

```
.TIME CODE GENERATOR switch---insignificant
.MONITOR/METER switch---------PB
.MUTING mode switch-----------selects the MUTE indicator mode
                              (inconsequential to the recording)
.D/A INPUT selector-----------INTERNAL
.A/D INPUT selector-----------DUBBING
```

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)--insignificant

-Encoder Board

.EMPHASIS switch---insignificant (determined by the PLAYER tape)

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector-select the position according to the FsID indicator so that the selected sampling frequency is the same as the sampling frequency on the PLAYER tape.

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind the tape.

SETTING OF BVU-800DB (RECORDER)

-Front Panel

```
.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL          ┐ fixed with
.VIDEO INPUT SELECT switch-----------LINE            │   switch
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2(36P)   │ protectors
.PB-PB/EE selector-------------------PB/EE           ┘
.REMOTE/LOCAL selector---------------LOCAL
```

-Rear Panel

```
.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--select the position according
                                     to the external time code generator outputs
```

NOTES (refer to Figure 2-29)

When dubbing the TIME CODE with the DIGITAL AUDIO signal, make the connection a, b, and c.

The TIME CODE GENERATOR must have a regenerate function.

The connection c is for synchronization between the TIME CODE GENERATOR and the PROCESSOR.

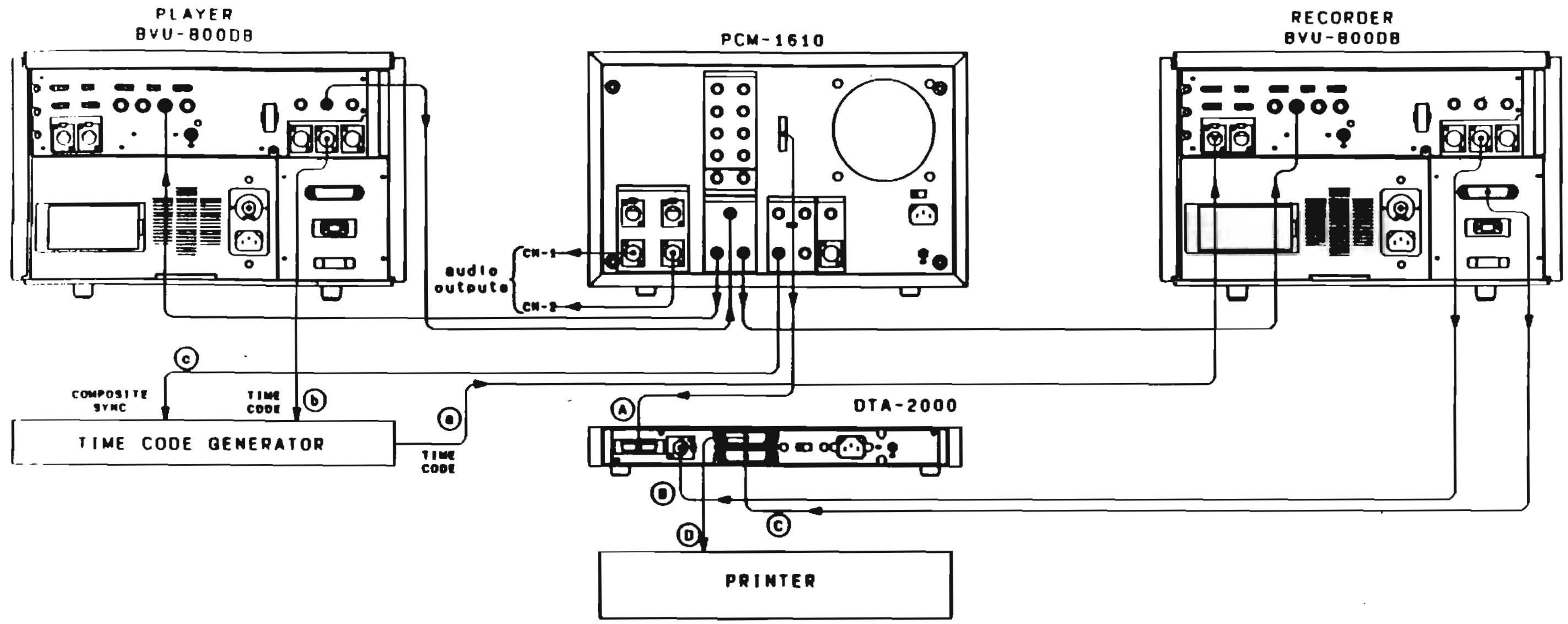
When using the **DTA-2000**, make the connections A - D.
The errors of the PLAYER can be checked during dubbing.

DIGITAL AUDIO signal is delayed about 9.7msec with repect to time code whenever dubbing is done.

During the dubbing the playback signal of the PLAYER is monitored from the **PCM-1610** analog outputs.

DIGITAL DUBBING

PCM-1610
BVU-800DB



2.5.1 DMR-4000/PCM-1630 (DABK-1630)/DTA-2000

SETTING OF DMR-4000 (PLAYER)

-Front Panel

.TRACKING control--------FIXED
.METER selector----------selects the source for the VIDEO/RF meter for main (R/P) or confidence (CONFI) head signals. CONFI is always playback from tape. R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector--------insignificant
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REC RUN
.REMOTE/LOCAL selector---REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector-----REMOTE-1(9P)
.AUX MONITOR selector--------------------insignificant
.PB/PB/EE selector------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant (time code generator not used)

-TC-38 Board

.GENERATOR DF/NDF selector---insignificant (TC generator inactive)

-DM-49 Board

.Composite Digital Output switch---------------OFF (NORMAL)

SETTING OF PCM-1630

-Front Panel

.ENC IN selector---------------DUBBING
.DA IN selector----------------INT
.MUTE indication mode selector--sets the MUTE indicator LED mode of operation. It is recommended to use HOLD so that the mute LED does not reset upon detection of a mute.
.MONITOR selector---------------PB
.PB MODE selector---------------A
.SCALE selector-----------------NORMAL
.PEAK indication mode selector--selects the metering mode. For the most critical applications, use PEAK HOLD.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch--------------------insignificant (determined by the digital audio data on the PLAYER)

-ENC-2 Board

.REC MUTE switch-----OFF (if ON, no recording will take place)

-SIF-1 Board

.Fs selector--------select the position according to the FsID LED so that the selector is the same setting as the sampling frequency of the PLAYER tape.

-MT-16 Board

.PEAK HOLD switch---selects the metering mode only. This does not affect the recording process. It is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to warn the operator that overlevel has occurred.

SETTING OF DABK-1630

.RAW switch-----------------------DUB

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape.

NOTE: The audio outputs from the **PCM-1630** are as follows:

PLAYER PB: PB SIGNAL of PLAYER (in this case the RECORDER must be in E-E mode: STOP, FF, REW).

RECORDER PB: PB signal of RECORDER

PREVIEW: PB signal of RECORDER (before IN point, after OUT point) or the PB signal of PLAYER (between IN point and OUT point).

EDIT: CONFI signal of RECORDER

SETTING OF DMR-4000 (RECORDER)

-Front Panel

.TRACKING control--------FIXED
.METER selector----------selects the source for the VIDEO/RF meter for main (R/P) or confidence (CONFI) head signals. CONFI is always playback from tape. R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector--------insignificant
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REC RUN
.REMOTE/LOCAL selector---LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---insignificant
.AUX MONITOR selector------------------insignificant
.PB/PB/EE selector------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---AUTO STOP mode causes the time code generator to stop when the RECORDER is stopped, otherwise the generator runs continously.

-TC-38 Board

.GENERATOR DF/NDF selector----select the position according to the original source time code which is indicated on the PLAYER machine front panel indicators.

-DM-49 Board

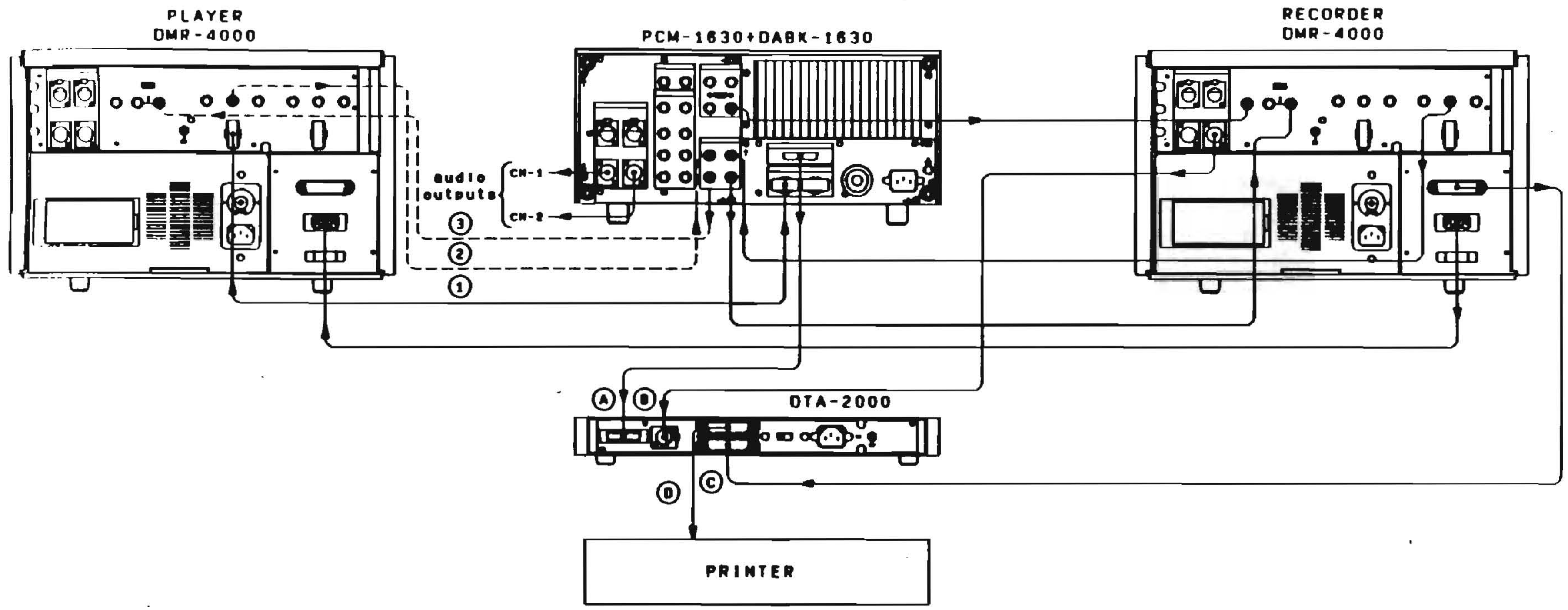
.Composite Digital Output switch----------ON (EDIT)

NOTE
(refer to Figure 2-31)

When using the **DTA-2000**, make connections A - D. During Editing, the errors of both the PLAYER and the RECORDER tapes can be checked.

Elementary Editing

PCM-1630+DABK-1630
DMR-4000
DMR-4000



2.5.2 BVU-800DB (BK-806)/DMR-4000/PCM-1630 (DABK-1630)/DTA-2000

SETTING OF BVU-800DB (PLAYER)

-Front Panel

```
.TRACKING control-------------FIXED
.TIME CODE switch-------------TC TRACK (w/BK-806
                              AUDIO CH-2 (w/o BK-806)
.AUDIO MONITOR selector-------insignificant
.AUDIO LIMITER switch---------insignificant
.MIXING SELECT switch---------insignificant
.MODE SELECT switch------------------NORMAL
.VIDEO INPUT SELECT switch-----------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--PB/EE
.PB-PB/EE selector-------------------PB/REMOTE
.REMOTE/LOCAL selector---REMOTE-1(9P)(remove the switch protector)
```

-Rear Panel

```
.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------insignificant
.600-ohm ON/OFF switches (AUDIO IN)--insignificant
```

SETTING OF BK-806

```
.INT TC/EXT TC select switch---------insignificant
.NDF switch--------------------------insignificant
.ERROR BYPASS switch-----------------ON
.Editing mode switch-----------------AUTO
```

SETTING OF PCM-1630

-Front Panel

```
.ENC IN selector---------------DUBBING
.DA IN selector----------------INT
.MUTE indication mode selector--sets the MUTE indicator LED
                                mode of operation.  It is
                                recommended to use HOLD so that
                                the mute LED does not reset
                                after detection of a mute.
.PEAK indication mode selector--selects the metering mode.  For
                                the most critical applications,
                                use PEAK HOLD.
.MONITOR selector---------------PB
.PB MODE selector---------------A
.SCALE selector-----------------NORMAL
.PEAK indication mode selector--selects the metering mode.  For
                                the most critical applications,
                                use PEAK HOLD.
```

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch-------------------insignificant (determined by the digital audio data on the PLAYER)

-ENC-2 Board

.REC MUTE switch-----OFF (if ON, no recording will take place)

-SIF-1 Board

.Fs selector--------select the position according to the FsID LED so that the selector is the same setting as the sampling frequency of the PLAYER tape.

-MT-16 Board

.PEAK HOLD switch---selects the metering mode only. This does not affect the recording process. It is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to warn the operator that overlevel has occurred.

SETTING OF DABK-1630

.RAW switch-----------------------DUB

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape.

NOTE: The audio outputs from the **PCM-1630** are as follows:

PLAYER PB: PB signal of PLAYER (in this case the RECORDER must be in E-E mode: STOP, FF, REW).

RECORDER PB: PB signal of RECORDER

PREVIEW: PB signal of RECORDER (before IN point, after OUT point) or the PB signal of PLAYER (between IN point and OUT point).

EDIT: CONFI signal of RECORDER

SETTING OF DMR-4000 (RECORDER)

-Front Panel

.TRACKING control---------FIXED
.METER selector-----------selects the source for the VIDEO/RF meter for main (R/P) or confidence (CONFI) head signals. CONFI is always playback from tape. R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector---------insignificant
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REC RUN
.REMOTE/LOCAL selector---LOCAL
.REMOTE-1(9P)/REMOTE-2(36P) selector---insignificant
.AUX MONITOR selector-----------------insignificant
.PB/PB/EE selector------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---AUTO STOP mode causes the time code generator to stop when the RECORDER is stopped, otherwise the generator runs continously.

-TC-38 Board

.GENERATOR DF/NDF selector----select the position according to the original source time code which is indicated on the PLAYER machine front panel indicators.

-DM-49 Board

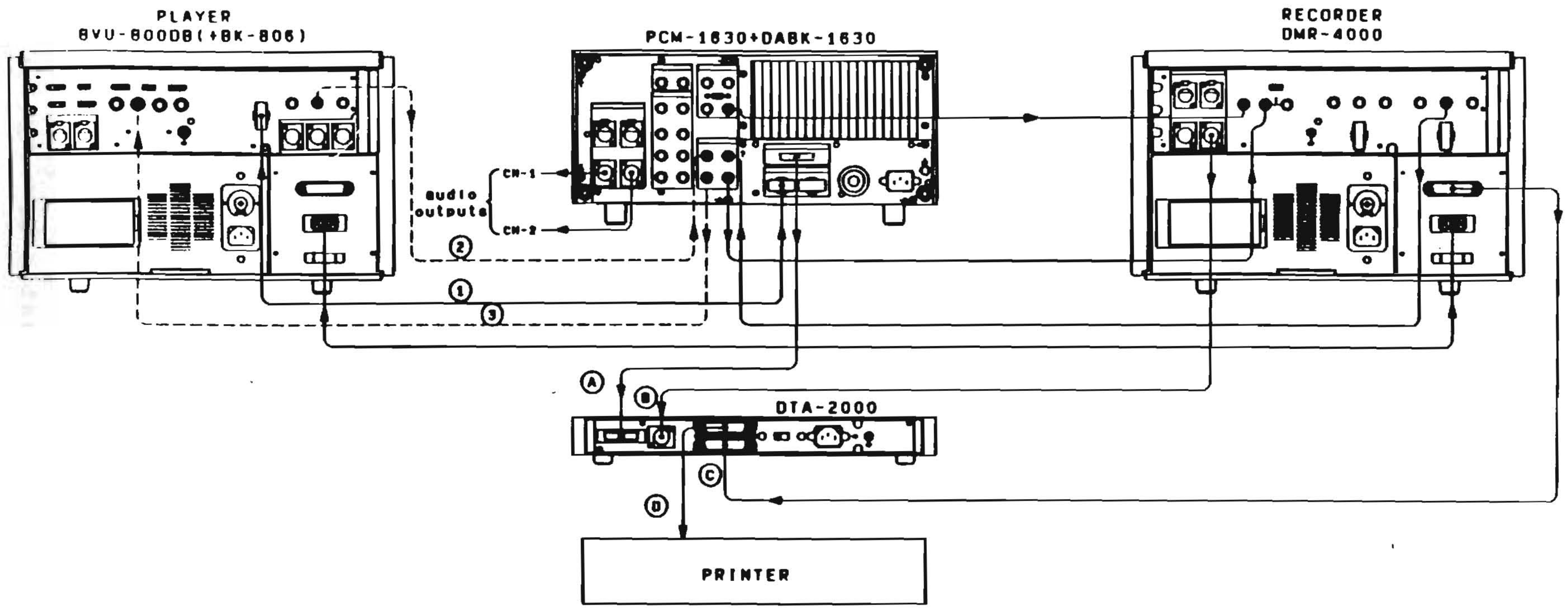
.Composite Digital Output switch----------ON (EDIT)

NOTE
(refer to Figure 2-32)

When using the **DTA-2000**, make connections A - D. During Editing, the errors of both the PLAYER and the RECORDER tapes can be checked.

Elementary Editing

PCM-1630+DABK-1630
BVU-800DB(+BK-806)
DMR-4000



2.6 PRECISE EDITING WITH THE EDITOR

By using the **DAE-1100(A)** digital audio editor, editing of an accuracy with +/-363usec can be performed. The editor performs the calculations for any subframe edits and transfers the information to the RECORDER which edits to the time code frame. The PLAYER and the RECORDER are controlled by the keyboard of the **DAE-1100(A)** in the same manner as in conventional analog audio editing. Precise edit points are located by way of the SEARCH dial which scrolls through a RAM memory as slow play of the digital audio signals directly from the rotary head recorders is not possible due to the psuedo-video composite digital audio signals. Although the examples of this section illustrate the cases that the same kind of rotary head recorder is used on PLAYER and RECORDER sides, different machines can be used.

By adding the second PLAYER (PLAYER-B), the system can be used as 2-PLAYER system. The connection of the PLAYER-B can be made in the same manner as the PLAYER-A machine, and the signals to the PCM processor (and to the RECORDER) are automatically switched by the editor when the appropriate machine is selected by the operator by means of the selector switch on the keyboard.

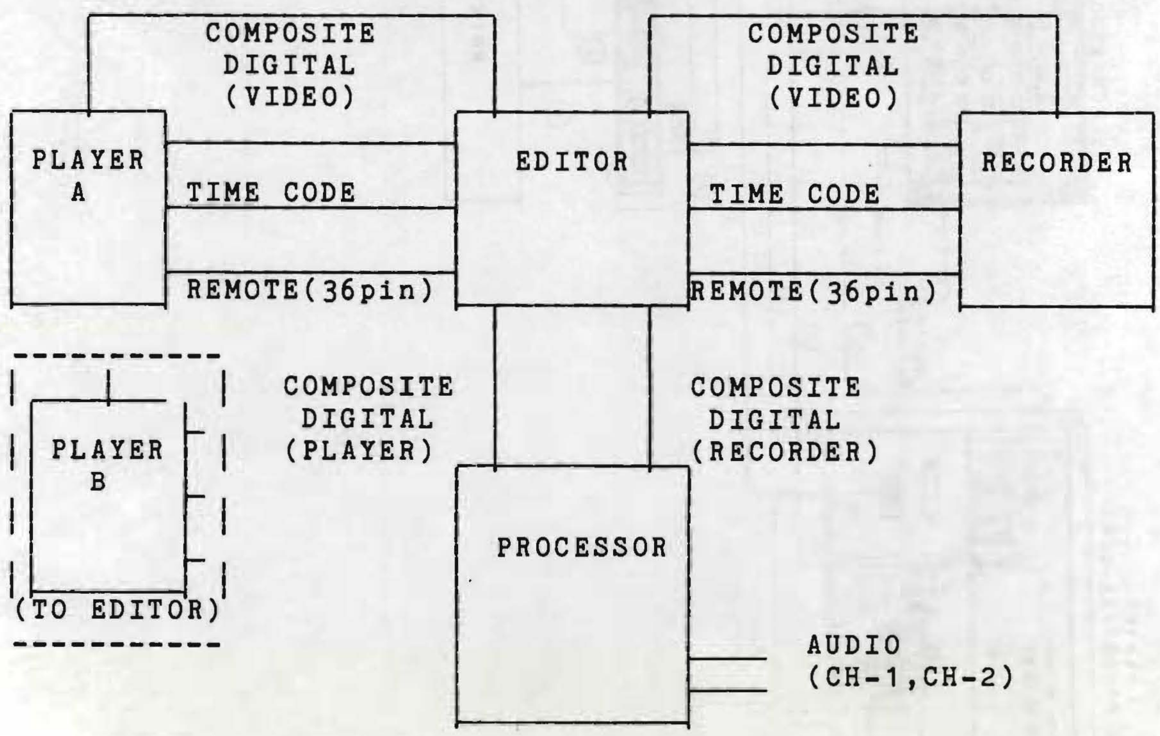


Figure 2-33 Digital Audio Editing System Block Diagram

SETTING OF DMR-4000 (RECORDER)

-Front Panel

.TRACKING control--------FIXED
.METER selector----------selects the source for the VIDEO/RF meter for main (R/P) or confidence (CONFI) head signals. CONFI is always playback from tape. R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector--------SUB
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REGEN
.REMOTE/LOCAL selector---REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector----------REMOTE-2(36P)
.AUX MONITOR selector-------------------------insignificant
.PB/PB/EE selector--------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)----insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---for CD mastering use NDF, make sure the EDITOR is set to the same position as the RECORDER

-DM-49 Board

.Composite Digital Output switch------OFF (NORMAL)

SETTING OF DMR-4000 (PLAYER)

-Front Panel

.TRACKING control----------------FIXED
.METER selector------------------R/P
.AUX LIMITER switch--------------insignificant
.RAW OUT selector----------------insignificant
.AUX CH-2 selector---------------TIME CODE
.TIME CODE selector--------------REC RUN
.REMOTE/LOCAL selector-----------REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector--------REMOTE-2(36P)
.AUX MONITOR selector----------------------insignificant
.PB/PB/EE selector------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)--------insignificant

-TC-38 Board

.GENERATOR DF/NDF selector-------insignificant (time code reader)

-DM-49 Board

.Composite Digital Output switch-------OFF (NORMAL)

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DIGITAL
.DA IN selector------------------EXT
.MUTE indication mode selector--sets the MUTE indicator LED mode of operation. It is recommended to use HOLD so that the mute LED does not reset upon detection of a mute.
.PEAK indication mode selector--selects the metering mode. For the most critical applications, use PEAK HOLD.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)-----insignificant

-AD-23 Board

.EMP switch--------------------insignificant (determined by the digital audio data on the PLAYER)

-ENC-2 Board

.REC MUTE switch-----OFF (if ON, no recording will take place)

-SIF-1 Board

.Fs selector--------select the position according to the FsID LED so that the selector is the same setting as the sampling frequency of the PLAYER tape.

-MT-16 Board

.PEAK HOLD switch---selects the metering mode only. This does not affect the recording process. It is recommended to use the PEAK OVER HOLD mode.

SETTING OF DABK-1630

.RAW switch------------------------EDT

SETTING OF DAE-1100A (or DAE-1100+DABK-1100)

-Front Panel

.DATA selector----------------SER
.SYNC selector----------------SER
.DROP FRAME selector----------select the position according to the time code. For CD mastering, always use 44.1kHz sampling rate with SMPTE NDF time code.

-Rear Panel

.IN SEL switches -------------v

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

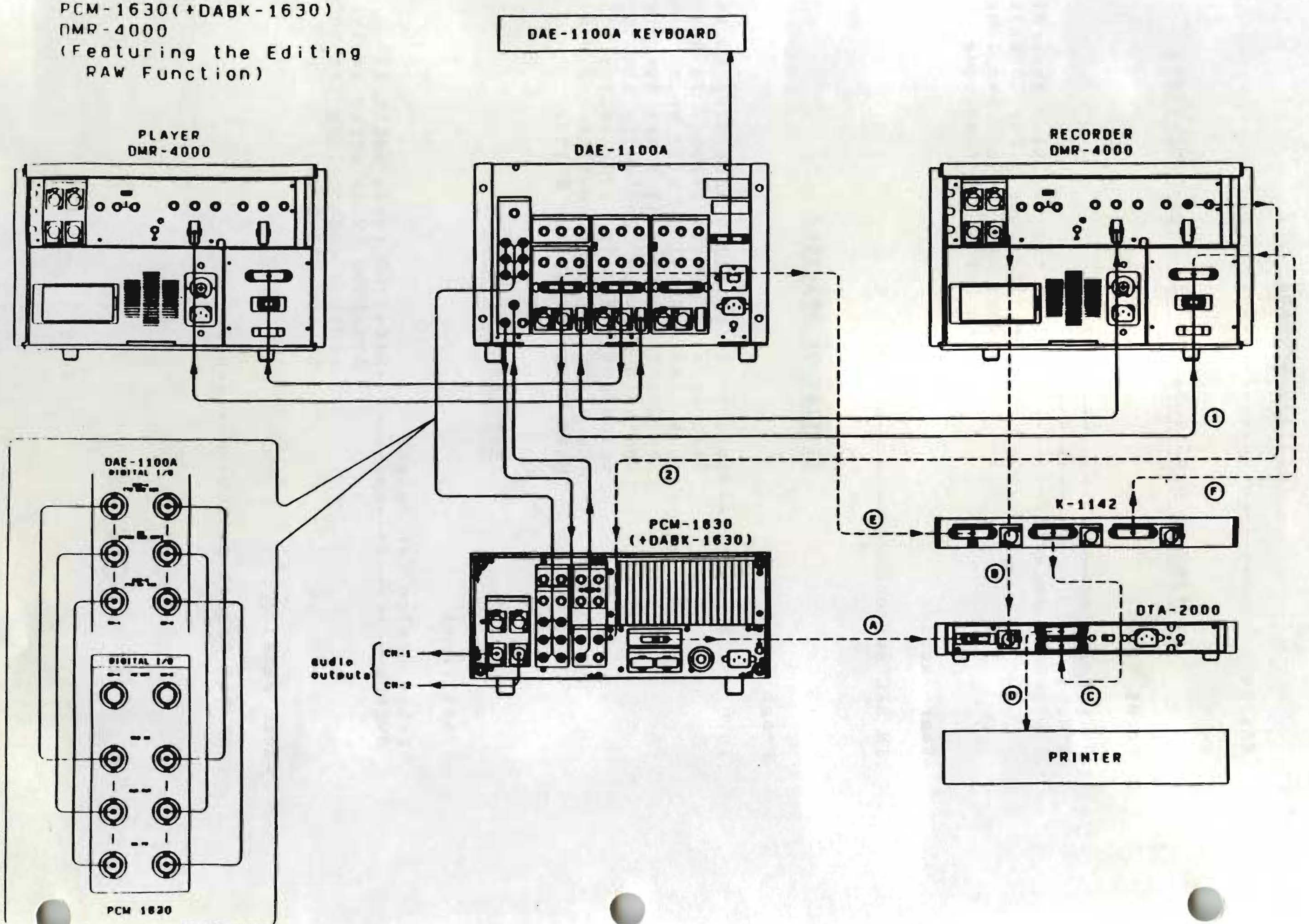
.System Controller Select Switch-----------------------**DAE-1100** (When editing)
DTA-2000 (When error analysis routine controlling the RECORDER by the **DTA-2000**).

-Rear Panel

.DAE/DAQ Select switch--------DAE

Precise Editing with the Editor

DAE-1100A
PCM-1630(+DABK-1630)
DMR-4000
(Featuring the Editing
RAW Function)



2.6.2 DMR-4000/PCM-1630 (DABK-1630)/DAE-1100A/DTA-2000/K-1142

SETTING OF DMR-4000 (RECORDER)

-Front Panel

.TRACKING control--------FIXED
.METER selector----------selects the source for the VIDEO/RF meter for main (R/P) or confidence (CONFI) head signals. CONFI is always playback from tape. R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector--------SUB
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REGEN
.REMOTE/LOCAL selector---REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector----REMOTE-2(36P)
.AUX MONITOR selector-------------------insignificant
.PB/PB/EE selector------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---for CD mastering use NDF, make sure the EDITOR is set to the same position as the RECORDER

-DM-49 Board

.Composite Digital Output switch---OFF (NORMAL)

SETTING OF DMR-4000 (PLAYER)

-Front Panel

.TRACKING control-----FIXED
.METER selector-------(see note for RECORDER)
.AUX LIMITER switch---insignificant
.RAW OUT selector-----insignificant
.AUX CH-2 selector----TIME CODE
.TIME CODE selector---REC RUN
.REMOTE/LOCAL selector---REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector---REMOTE-2(36P)
.AUX MONITOR selector------------------insignificant
.PB/PB/EE selector-------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)-------insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---for CD mastering use NDF, make sure the EDITOR is set to the same position as the RECORDER

-DM-49 Board

.Composite Digital Output switch----OFF (NORMAL)

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DIGITAL
.DA IN selector------------------EXT
.MUTE indication mode selector--sets the MUTE indicator LED mode of operation. It is recommended to use HOLD so that the mute LED does not reset after detection of a mute.
.PEAK indication mode selector--selects the metering mode. For the most critical applications, use PEAK HOLD.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)-----insignificant

-AD-23 Board

.EMP switch---insignificant (determined by the PLAYER tape data)

-ENC-2 Board

.REC MUTE switch-----OFF (if ON, no recording will take place)

-SIF-1 Board

.Fs selector--------select the position according to the FsID LED so that the selector is the same setting as the sampling frequency of the PLAYER tape.

-MT-16 Board

.PEAK HOLD switch---selects the metering mode only. This does not affect the recording process. It is recommended to use the PEAK OVER HOLD mode.

SETTING OF DABK-1630

.RAW switch------------------------OFF

SETTING OF DAE-1100A (or DAE-1100+DABK-1100)

-Front Panel

.DATA selector--------SER
.SYNC selector--------SER
.DROP FRAME selector--same as TC on tape. For CD mastering always use NDF time code.

-Rear Panel

.IN SEL switches -------------v

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis and control of the RECORDER)

-Rear Panel

.DAE/DAQ Select switch--------DAE

NOTES
(refer to Figure 2-34)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - F and do not make connection 1.

The EDITING RAW function is possible when installing the **DABK-1630** into the **PCM-1630** and making connection 2. The PLAYER does not need to be the **DMR-4000** for this function.

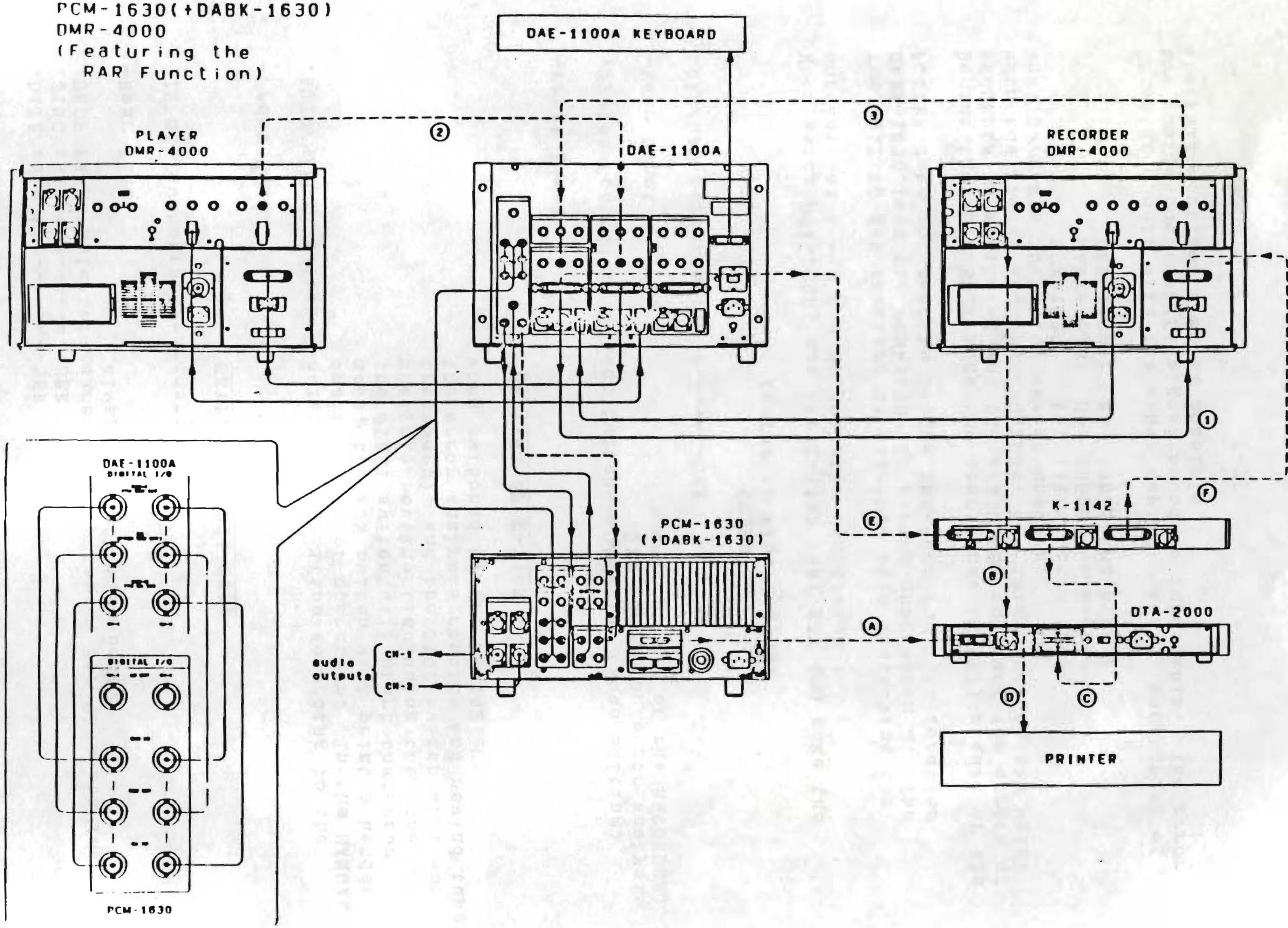
During the AUTO EDIT mode the confidence (CONFI) signal of the RECORDER is monitored and the **DTA-2000** can check the errors of both the PLAYER and the RECORDER. For this function the units must have the following serial numbers:

PCM-1630 : No. 11301 and higher
DABK-1630: No. 10601 and higher
DAE-1100 : No. 10601 and higher

If using a unit with the other serial numbers, monitoring of the confidence (CONFI) signal sound is impossible. The error analysis routine is still possible.

Precise Editing with the Editor

DAE-1100A
PCM-1630(+DABK-1630)
DMR-4000
(Featuring the
RAR Function)



2.6.3 DMR-2000/PCM-1630/DAE-1100A/DTA-2000/K-1142

SETTING OF DMR-2000 (RECORDER)

-Front Panel

.TRACKING CONTROL------------FIXED
.CH-2 switch-----------------TIME CODE
.AUX LIMITER switch----------insignificant
.MONITOR SELECT switch-------insignificant
.REMOTE/LOCAL switch---------REMOTE-2/LOCAL
.TIME CODE mode selector-----REGEN
.MEMORY switch---------------OFF

-Rear Panel

.NDF/DF selector-------for CD mastering use NDF, make sure the EDITOR is set to the same position as the RECORDER.

SETTING OF DMR-2000 (PLAYER)

-Front Panel

.TRACKING CONTROL------------FIXED
.CH-2 switch-----------------TIME CODE
.AUX LIMITER switch----------insignificant
.MONITOR SELECT switch-------insignificant
.REMOTE/LOCAL switch---------REMOTE-2/LOCAL
.TIME CODE mode selector-----AUTO STOP
.MEMORY switch---------------selects the display mode for the front panel numerical display, does not affect the recording

-Rear Panel

.NDF/DF selector-------------insignificant (determined by tape). The time code generator is inactive during the playback mode and the time code which is already recorded on the tape will determined the type of time code present on the TIME CODE OUTPUT connector on the rear of the machine.

SETTING OF DAE-1100A (or DAE-1100+DABK-1100)

-Front Panel

.DATA selector----------------SER
.SYNC selector----------------SER
.DROP FRAME selector----------select the position according to the time code used on the tapes. For CD mastering, use NDF.

-Rear Panel

.IN SEL switches -------------v

SETTING OF PCM-1630

-Front Panel

.ENC IN selector------------------DIGITAL
.DA IN selector-------------------EXT
.MUTE indication mode selector---selects the muting indicator mode. The LED can be set to stay lit until reset or to automatically turn off after the muting condition has ceased. For the most critical applications, set to HOLD position.
.MONITOR selector-----------------PB
.PB MODE selector-----------------A
.SCALE selector-------------------NORMAL
.PEAK indication mode selector---selects the PEAK indicator mode. This switch operates in conjunction with the switch on the MT-16 card. For the most critical applications, set this to HOLD mode.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---insignificant (determined by the PLAYER tape)

-ENC-2 Board

.REC MUTE switch----OFF (if this is ON, no recording will take place, all zeroes will be transfered to the RECORDER)

-SIF-1 Board

.Fs selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape (with respect to the PLAYER tape).

-MT-16 Board

.PEAK HOLD switch---selects the PEAK HOLD mode when the front panel switch is in the HOLD position. For the most critical applications it is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to alert the operator of such a condition.

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

.DAE/DAQ Select switch--------DAE

NOTES

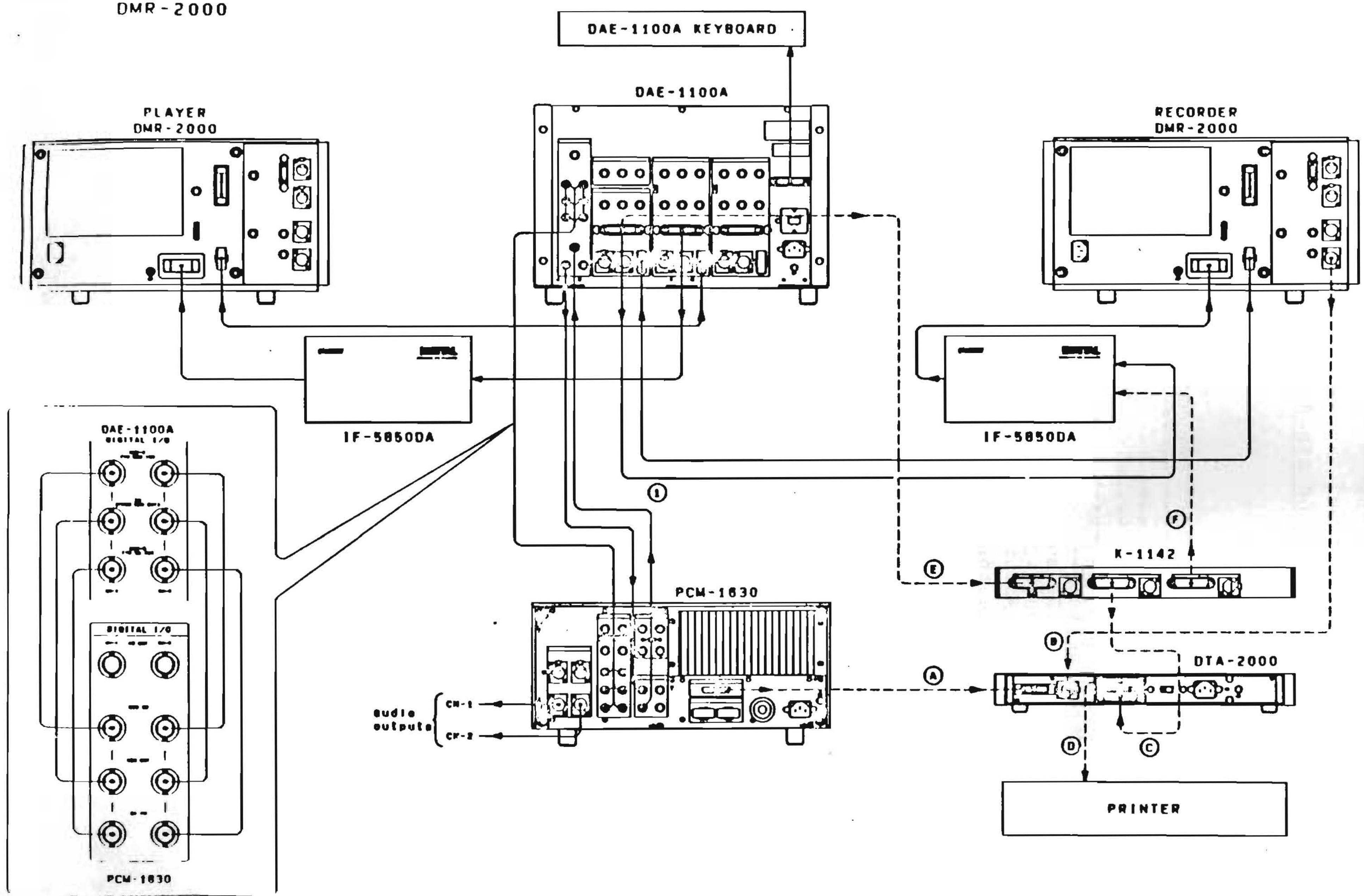
(refer to Figure 2-35)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - F. (In this case, do not make connection 1.)

The RAR function during PB mode is not possible when using the **DMR-2000** machine

Precise Editing with the Editor

DAE-1100A
PCM-1630
DMR-2000



2.6.4 BVU-800DB/PCM-1630/DAE-1100A/DTA-2000/K-1142

SETTING OF BVU-800DB (RECORDER)

-Front Panel

.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL
.VIDEO INPUT SELECT switch-----------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2
.PB-PB/EE selector-------------------PB/EE
.REMOTE/LOCAL selector---------------REMOTE

(MIXING SELECT switch through PB-PB/EE selector: fixed with switch protectors)

-Rear Panel

.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--ON

SETTING OF BVU-800DB (PLAYER)

-Front Panel

.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------CH-2
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL
.VIDEO INPUT SELECT switch-----------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2
.PB-PB/EE selector-------------------PB/EE
.REMOTE/LOCAL selector---------------REMOTE

(MIXING SELECT switch through PB-PB/EE selector: fixed with switch protectors)

-Rear Panel

.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--OFF

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DIGITAL
.DA IN selector------------------EXT
.MUTE indication mode selector---selects the muting indicator mode. The LED can be set to stay lit until reset or to automatically turn off after the muting condition has ceased. For the most critical applications, set to HOLD position.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL
.PEAK indication mode selector---selects the PEAK indicator mode. This switch operates in conjunction with the switch on the MT-16 card. For the most critical applications, set this to HOLD mode.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---insignificant (determined by the PLAYER tape)

-ENC-2 Board

.REC MUTE switch----OFF (if this is ON, no recording will take place, all zeroes will be transfered to the RECORDER)

-SIF-1 Board

.Fs selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape (with respect to the PLAYER tape).

-MT-16 Board

.PEAK HOLD switch---selects the PEAK HOLD mode when the front panel switch is in the HOLD position. For the most critical applications it is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to alert the operator of such a condition.

SETTING OF DAE-1100A (or DAE-1100+DABK-1100)

-Front Panel

.DATA selector---------------SER
.SYNC selector---------------SER
.DROP FRAME selector---------select the position according to the time code used on the tapes. For CD mastering, use NDF.

-Rear Panel

.IN SEL switches -------------v

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

.DAE/DAQ Select switch--------DAE

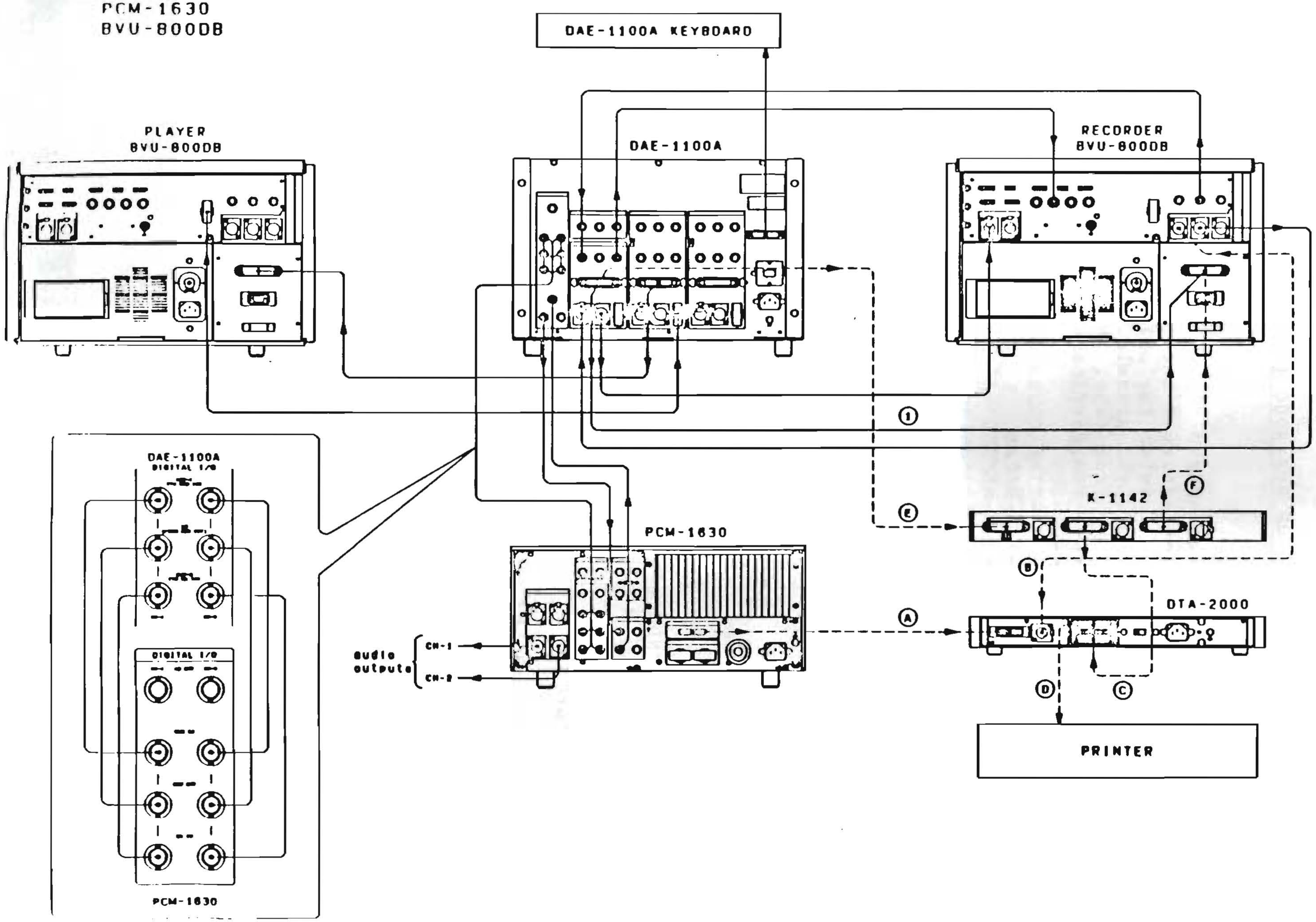
NOTES

(refer to Figure 2-36)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - F. (In this case, do not make connection 1.)

Precise Editing with the Editor

DAE-1100A
PCM-1630
BVU-800DB



2.6.5 DMR-4000/PCM-1610/DAE-1100A/DTA-2000/K-1142

SETTING OF DMR-4000 (RECORDER)

-Front Panel

.TRACKING control--------FIXED
.METER selector----------selects the source for the VIDEO/RF meter for main (R/P) or confidence (CONFI) head signals. CONFI is always playback from tape. R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector--------SUB
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REGEN
.REMOTE/LOCAL selector---REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector---REMOTE-2(36P)
.AUX MONITOR selector-----------------insignificant
.PB/PB/EE selector---PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)--insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)-------insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---for CD mastering use NDF, make sure the EDITOR is set to the same position as the RECORDER

-DM-49 Board

.Composite Digital Output switch----OFF (NORMAL)

SETTING OF DAE-1100A (or DAE-1100+DABK-1100)

-Front Panel

.DATA selector---------------SER
.SYNC selector---------------SER
.DROP FRAME selector---------select the position according to the time code used on the tapes. For CD mastering, use NDF.

-Rear Panel

.IN SEL switches -------------v

SETTING OF DMR-4000 (PLAYER)

-Front Panel

.TRACKING control----------------FIXED
.METER selector------------------R/P
.AUX LIMITER switch--------------insignificant
.RAW OUT selector----------------insignificant
.AUX CH-2 selector---------------TIME CODE
.TIME CODE selector--------------REC RUN
.REMOTE/LOCAL selector-----------REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector----REMOTE-2(36P)
.AUX MONITOR selector--------------------insignificant
.PB/PB/EE selector----PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---insignificant (generator inactive)

-DM-49 Board

.Composite Digital Output switch-OFF(NORMAL)

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch---insignificant
.MONITOR/METER switch---------PB
.MUTING mode switch-----------selects the muting indicator mode. The LED can be set to stay lit until reset or to automatically turn off after the muting condition has ceased. For the most critical applications, set to HOLD position.
.D/A INPUT selector-----------EXTERNAL
.A/D INPUT selector-----------DIGITAL

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---insignificant (determined by the digital audio data on the PLAYER tape)

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape (with respect to the PLAYER tape).

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

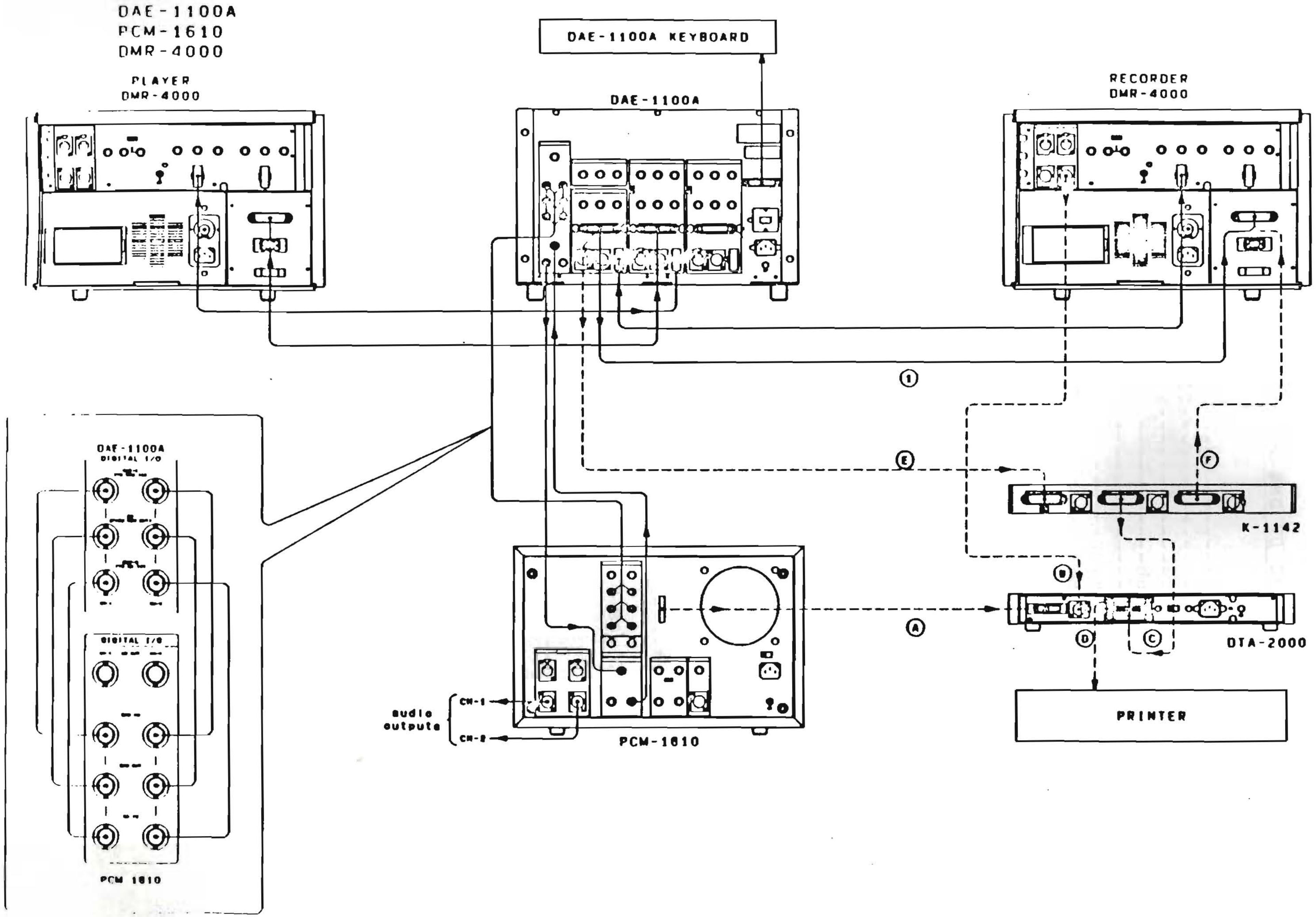
.DAE/DAQ Select switch--------DAE

NOTES

(refer to Figure 2-37)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - F. (In this case, do not make connection 1.)

Precise Editing with the Editor



2.6.6 DMR-2000/PCM-1610/DAE-1100A/DTA-2000/K-1142

SETTING OF DMR-2000 (RECORDER)

-Front Panel

.TRACKING CONTROL------------------FIXED
.CH-2 switch-----------------------TIME CODE
.AUX LIMITER switch----------------insignificant
.MONITOR SELECT switch-------------insignificant
.REMOTE/LOCAL switch---------------REMOTE-2/LOCAL
.TIME CODE mode selector-----------REGEN
.MEMORY switch---------------------OFF

-Rear Panel

.NDF/DF selector---set same position as editor DROP FRAME sel.

SETTING OF DMR-2000 (RECORDER)

-Front Panel

.TRACKING CONTROL------------------FIXED
.CH-2 switch-----------------------TIME CODE
.AUX LIMITER switch----------------insignificant
.MONITOR SELECT switch-------------insignificant
.REMOTE/LOCAL switch---------------REMOTE-2/LOCAL
.TIME CODE mode selector-----------AUTO STOP
.MEMORY switch---------------------OFF

-Rear Panel

.NDF/DF selector-------------------insignificant

SETTING OF DAE-1100A (or DAE-1100+DABK-1100)

-Front Panel

.DATA selector----------SER
.SYNC selector----------SER
.DROP FRAME selector---select the position according to the time code used on the tapes. For CD mastering, use NDF.

-Rear Panel

.IN SEL switches --------------v

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the K-1142.

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch---insignificant
.MONITOR/METER switch---------PB
.MUTING mode switch-----------selects the muting indicator mode. The LED can be set to stay lit until reset or to automatically turn off after the muting condition has ceased. For the most critical applications, set to HOLD position.
.D/A INPUT selector-----------EXTERNAL
.A/D INPUT selector-----------DIGITAL

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---insignificant (determined by the digital audio data on the PLAYER tape)

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape (with respect to the PLAYER tape).

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

.DAE/DAQ Select switch--------DAE

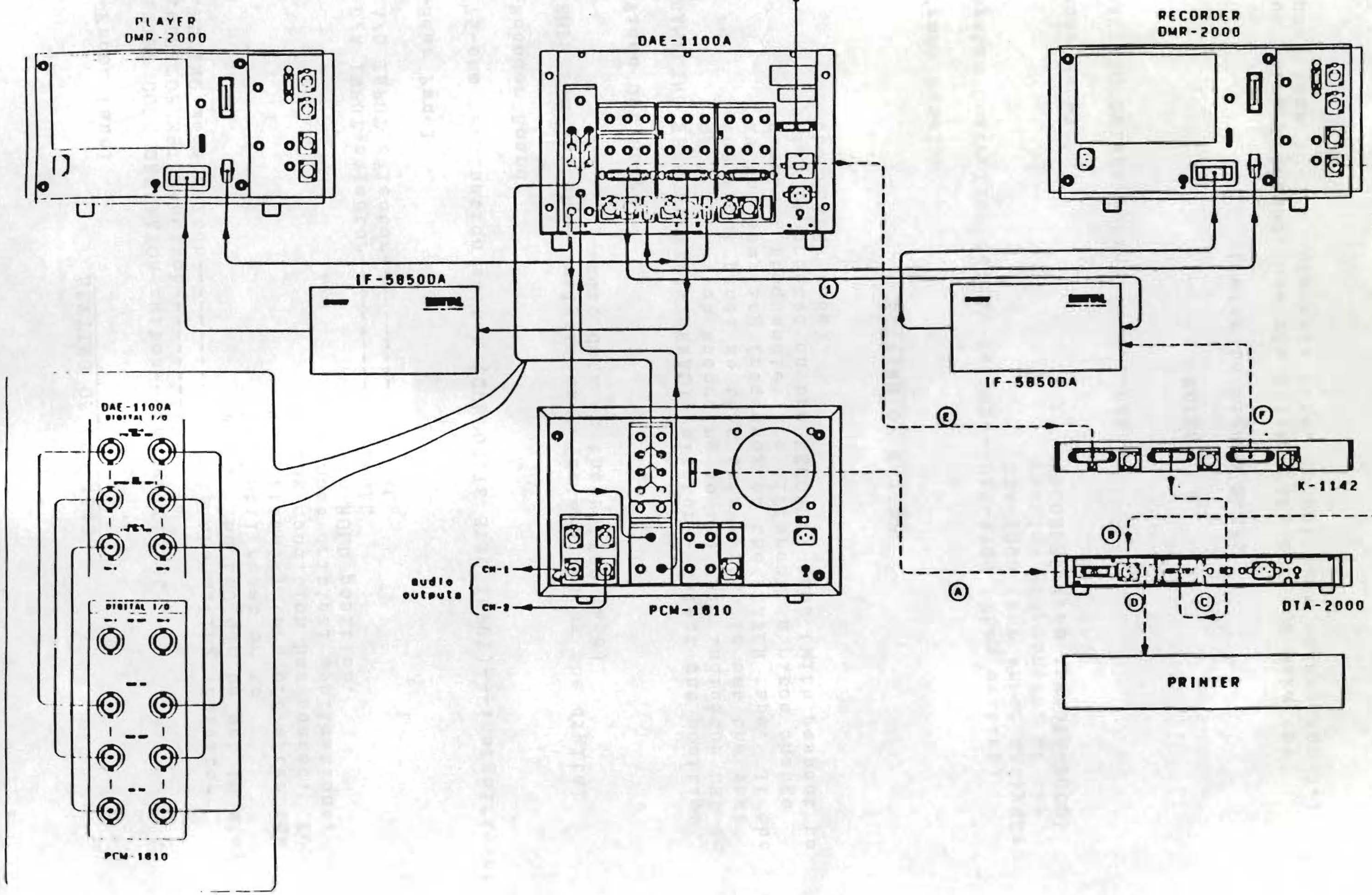
NOTES

(refer to Figure 2-38)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - F. (In this case, do not make connection 1.)

Precise Editing with the Editor

DAE-1100A
PCM-1610
DMR-2000



2.6.7 BVU-800DB/PCM-1610/DAE-1100A/DTA-2000/K-1142

SETTING OF BVU-800DB (RECORDER)

-Front Panel

.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL
.VIDEO INPUT SELECT switch-----------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2
.PB-PB/EE selector-------------------PB/EE
fixed with switch protectors
.REMOTE/LOCAL selector---------------REMOTE

-Rear Panel

.COLOR ON/OFF switch-------------------OFF
.DOC ON/OFF switch---------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-------ON
.AUDIO IN LEVEL selectors--------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)---ON

SETTING OF BVU-800DB (PLAYER)

-Front Panel

.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------CH-2
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL
.VIDEO INPUT SELECT switch-----------LINE
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2
.PB-PB/EE selector-------------------PB/EE
fixed with switch protectors
.REMOTE/LOCAL selector---------------REMOTE

-Rear Panel

.COLOR ON/OFF switch-------------------OFF
.DOC ON/OFF switch---------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-------ON
.AUDIO IN LEVEL selectors--------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)---OFF

SETTING OF PCM-1610

The switch positions are listed on the chart on page 2-115. It is important to place the SAMPLING FREQUENCY (INTERNAL) selector switch in the position which matches the PLAYER tape time code (indicated by the FsID LED on the front panel). The MONITOR/METER switch must be set to PB, the D/A INPUT is set to EXTERNAL, and the A/D INPUT is set to DIGITAL, all other switches are inconsequential to the recording.

SETTING OF DAE-1100A (or DAE-1100+DABK-1100)

-Front Panel

.DATA selector and SYNC selector----------------SER
.DROP FRAME selector---select the position according to the time code used on the tapes. For CD mastering, use NDF.

-Rear Panel

.IN SEL switches -------------v

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

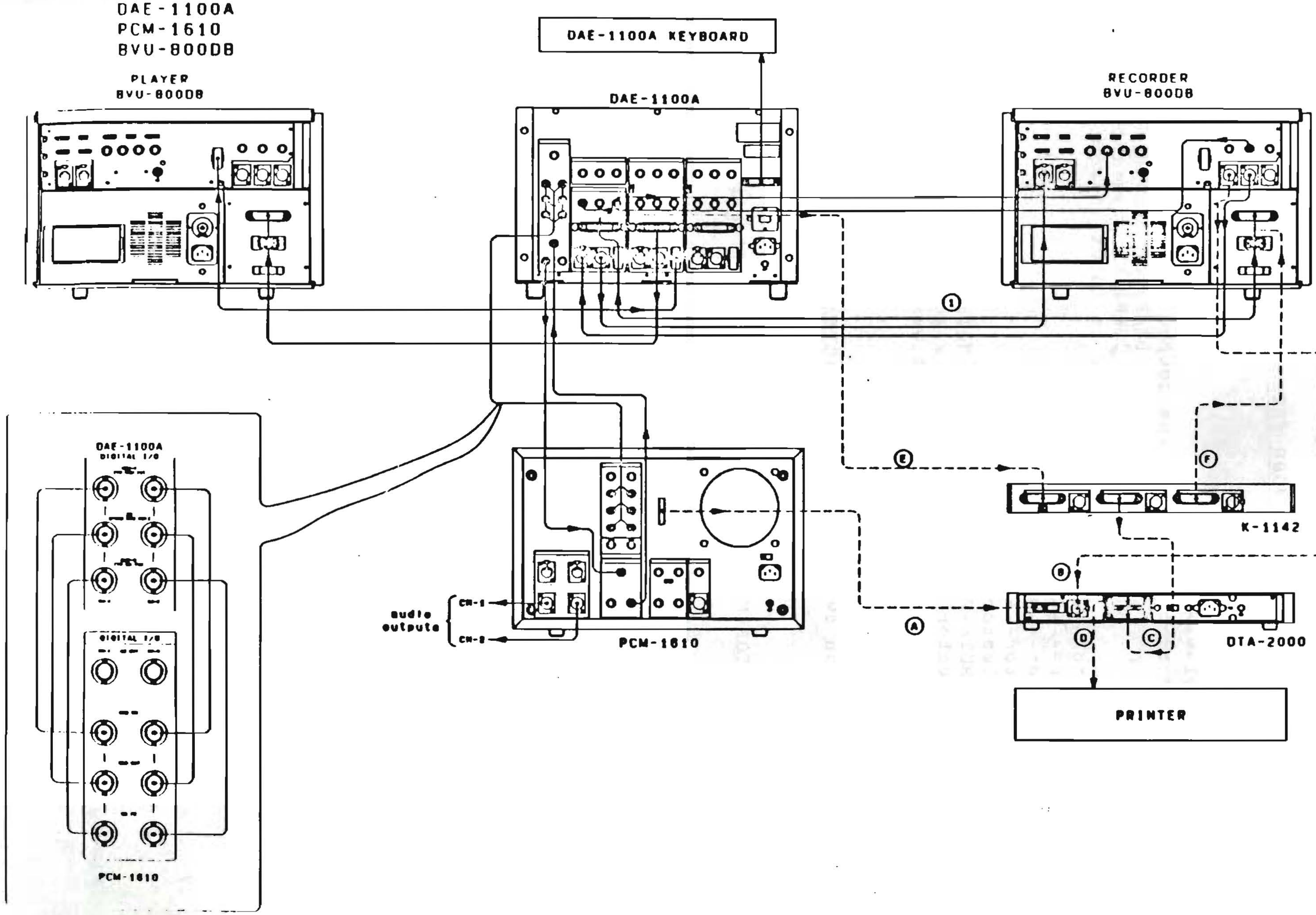
.DAE/DAQ Select switch--------DAE

NOTES
(refer to Figure 2-38)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - F. (In this case, do not make connection 1.)

Precise Editing with the Editor

DAE-1100A
PCM-1610
BVU-800DB



2.6.8 DMR-4000/PCM-1630 (DABK-1630)/DAE-1100/DTA-2000/K-1142

SETTING OF DMR-4000 (RECORDER)

-Front Panel

.TRACKING control--------FIXED
.METER selector----------selects the source for the VIDEO/RF meter for main (R/P) or confidence (CONFI) head signals. CONFI is always playback from tape. R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector--------SUB
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REGEN
.REMOTE/LOCAL selector---REMOTE
.REMOTE-1(9P)/REMOTE-2(36P)selector---REMOTE-2(36P)
.AUX MONITOR selector-----------------insignificant
.PB/PB/EE selector---PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---for CD mastering use NDF, make sure the EDITOR is set to the same position as the RECORDER

-DM-49 Board

.Composite Digital Output switch--------OFF (NORMAL)

SETTING OF DAE-1100

-Front Panel

.DATA selector---------------SER
.SYNC selector---------------SER
.DROP FRAME selector---------select the position according to the time code used on the tapes. For CD mastering, use NDF.

-Rear Panel

.75-ohm terminatation switch (VIDEO IN)-------------ON

SETTING OF DABK-1630

.RAW switch-----------------------EDT

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DIGITAL
.DA IN selector------------------EXT
.MUTE indication mode selector---selects the muting indicator mode. The LED can be set to stay lit until reset or to automatically turn off after the muting condition has ceased. For the most critical applications, set to HOLD position.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL
.PEAK indication mode selector---selects the PEAK indicator mode. This switch operates in conjunction with the switch on the MT-16 card. For the most critical applications, set this to HOLD mode.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---insignificant (determined by the PLAYER tape)

-ENC-2 Board

.REC MUTE switch----OFF (if this is ON, no recording will take place, all zeroes will be transfered to the RECORDER)

-SIF-1 Board

.Fs selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape (with respect to the PLAYER tape).

-MT-16 Board

.PEAK HOLD switch---selects the PEAK HOLD mode when the front panel switch is in the HOLD position. For the most critical applications it is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to alert the operator of such a condition.

SETTING OF DMR-4000 (PLAYER)

-Front Panel

.TRACKING control-----------------FIXED
.METER selector-------------------R/P
.AUX LIMITER switch---------------insignificant
.RAW OUT selector-----------------insignificant
.AUX CH-2 selector----------------TIME CODE
.TIME CODE selector---------------REC RUN
.REMOTE/LOCAL selector------------REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector---REMOTE-2(36P)
.AUX MONITOR selector-------------------insignificant
.PB/PB/EE selector----PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)-----insignificant

-TC-38 Board

.GENERATOR DF/NDF selector-------insignificant

-DM-49 Board

.Composite Digital Output switch-----OFF (NORMAL)

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

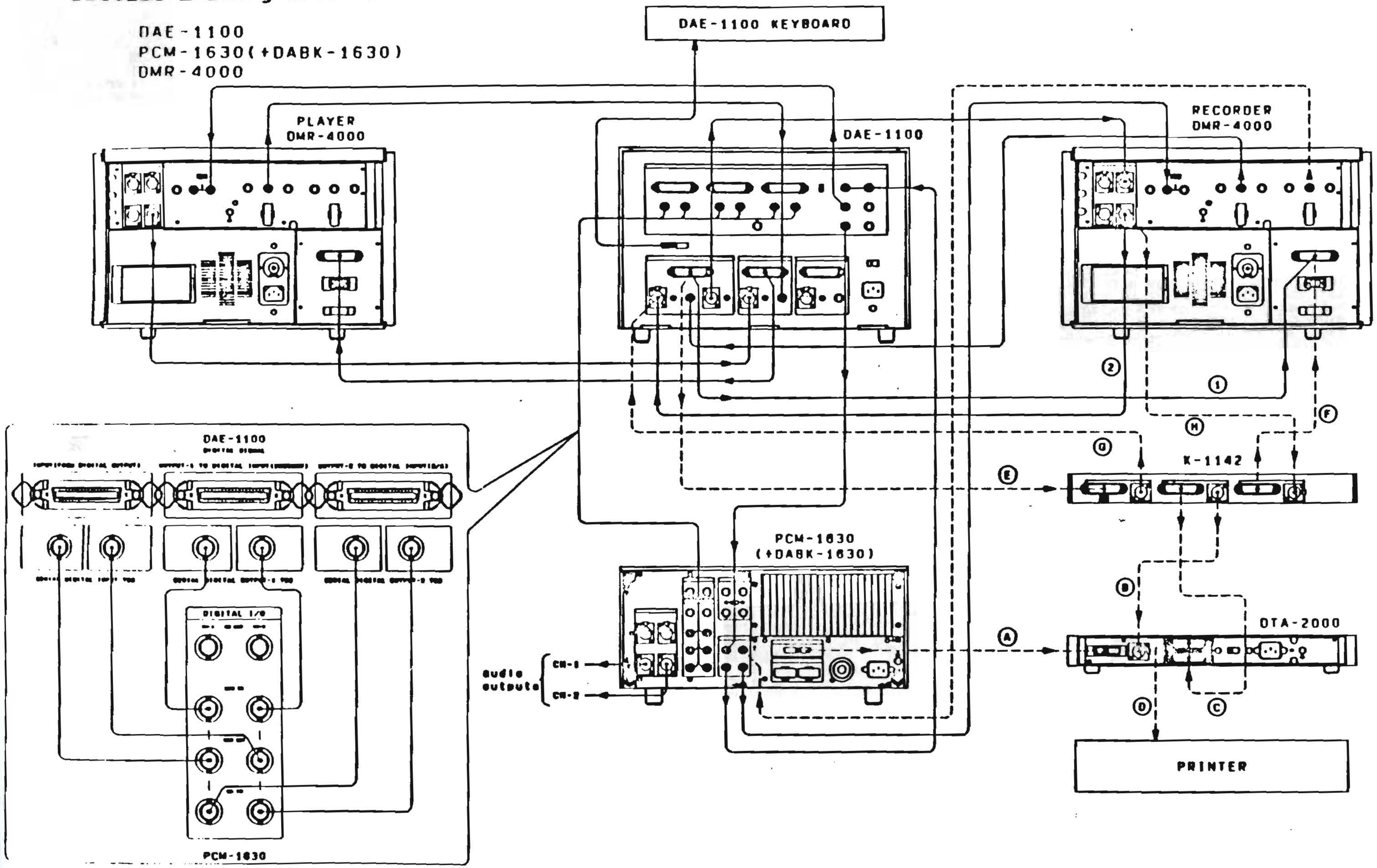
-Rear Panel

.DAE/DAQ Select switch--------DAE

NOTE (refer to Figure 2-40)
When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - F and do not make connection 1.

Precise Editing with the Editor

DAE-1100
PCM-1630(+DABK-1630)
DMR-4000



2.6.9 DMR-2000/PCM-1630/DAE-1100/DTA-2000/K-1142

SETTING OF DMR-2000 (RECORDER AND PLAYER)

-Front Panel

.TRACKING CONTROL-----------------FIXED
.CH-2 switch----------------------TIME CODE
.AUX LIMITER switch---------------insignificant
.MONITOR SELECT switch------------insignificant
.REMOTE/LOCAL switch--------------REMOTE-2/LOCAL
.TIME CODE mode selector----------REGEN (RECORDER)
AUTO STOP (PLAYER)
.MEMORY switch--------------------OFF

-Rear Panel

.NDF/DF selector----select the position according to the time code being used. The EDITOR and the RECORDER must have the same setting, the PLAYER position is insignificant.

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DIGITAL
.DA IN selector------------------EXT
.MUTE indication mode selector---selects the muting indicator mode. The LED can be set to stay lit until reset or to automatically turn off after the muting has ceased.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL
.PEAK indication mode selector---selects the PEAK indicator mode.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---insignificant (determined by the PLAYER tape)

-ENC-2 Board

.REC MUTE switch----OFF (if ON, no recording will take place)

-SIF-1 Board

.Fs selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape.

-MT-16 Board

.PEAK HOLD switch---selects the PEAK HOLD mode when the front panel switch is in the HOLD position. For the most critical applications it is recommended to use the PEAK OVER HOLD mode.

SETTING OF DAE-1100

-Front Panel

.DATA selector----------------SER
.SYNC selector----------------SER
.DROP FRAME selector---------select the position according to the time code used on the tapes. For CD mastering, use NDF.

-Rear Panel

.75-ohm terminatation switch (VIDEO IN)-------------ON

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

.DAE/DAQ Select switch--------DAE

NOTES (refer to Figure 2-41)

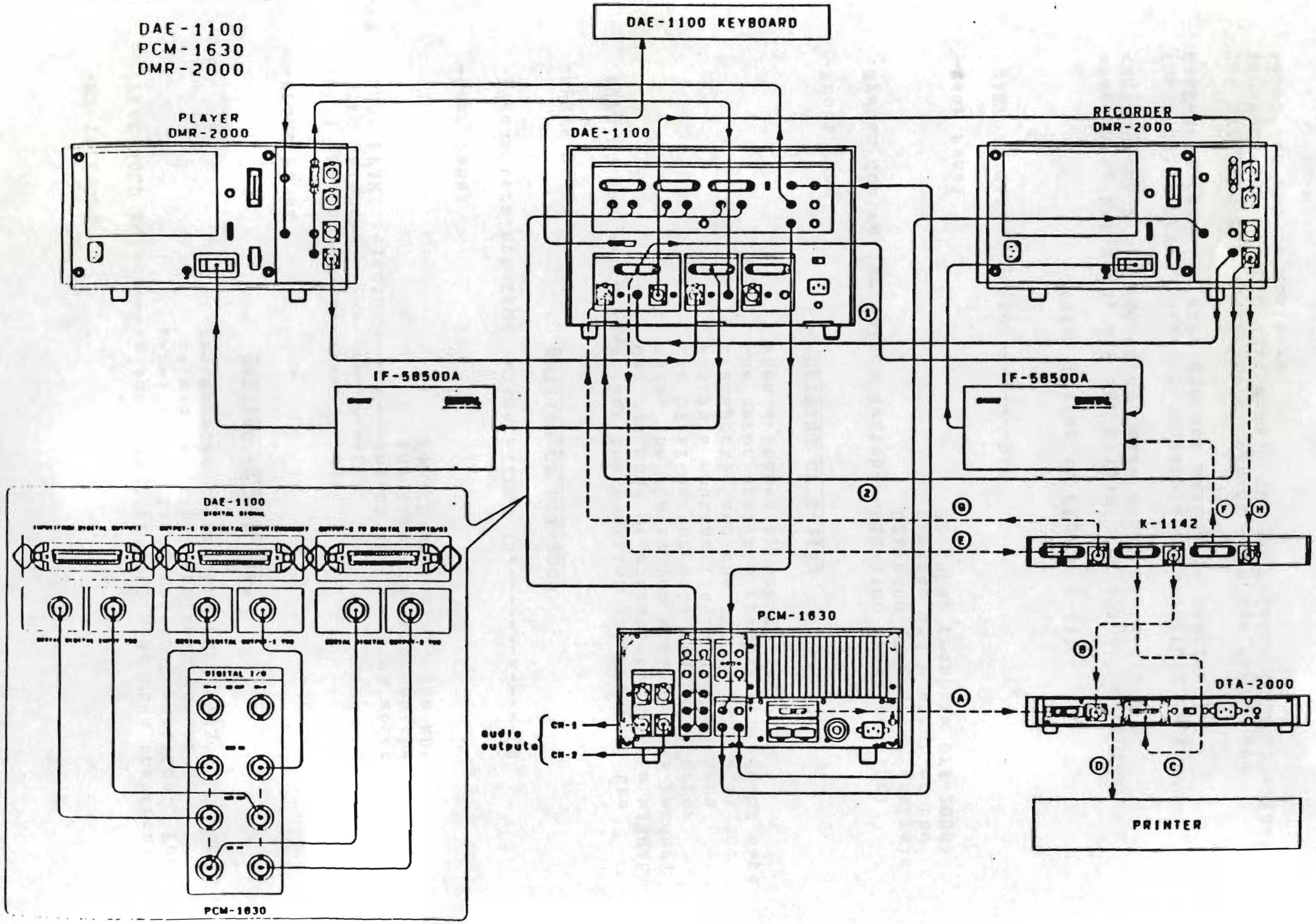
When using **DTA-2000,** use the **K-1142** PARA BOX and make the connections A - H and do not make connections 1 and 2.

The EDITING RAW function is possible when installing the **DABK-1630** into the **PCM-1630** and making connection 3.

The **DTA-2000** can check the errors of both the PLAYER and RECORDER during AUTO edit mode. The confidence (CONFI) signal sound can not be monitored.

Precise Editing with the Editor

DAE-1100
PCM-1630
DMR-2000



2.6.10 BVU-800DB/PCM-1630/DAE-1100/DTA-2000/K-1142

SETTING OF BVU-800DB (RECORDER)

-Front Panel

```
.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF
.MODE SELECT switch------------------NORMAL          fixed with
.VIDEO INPUT SELECT switch-----------LINE             switch
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2        protectors
.PB-PB/EE selector-------------------PB/EE
.REMOTE/LOCAL selector---------------REMOTE
```

-Rear Panel

```
.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------HIGH
.600-ohm ON/OFF switches (AUDIO IN)--ON
```

SETTING OF BVU-800DB (PLAYER)

-Front Panel

```
.TRACKING control--------------------FIXED
.TIME CODE switch--------------------TC TRACK
.AUDIO MONITOR selector--------------insignificant
.AUDIO LIMITER switch----------------insignificant
.MIXING SELECT switch----------------OFF              fixed with
.MODE SELECT switch------------------NORMAL            switch
.VIDEO INPUT SELECT switch-----------LINE             protectors
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2
.PB-PB/EE selector-------------------PB/EE
.REMOTE/LOCAL selector---------------REMOTE
```

-Rear Panel

```
.COLOR ON/OFF switch-----------------OFF
.DOC ON/OFF switch-------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)-----ON
.AUDIO IN LEVEL selectors------------insignificant
.600-ohm ON/OFF switches (AUDIO IN)--insignificant
```

SETTING OF PCM-1630

-Front Panel

.ENC IN selector-----------------DIGITAL
.DA IN selector------------------EXT
.MUTE indication mode selector---selects the muting indicator mode. The LED can be set to stay lit until reset or to automatically turn off after the muting condition has ceased. For the most critical applications, set to HOLD position.
.MONITOR selector----------------PB
.PB MODE selector----------------A
.SCALE selector------------------NORMAL
.PEAK indication mode selector---selects the PEAK indicator mode. This switch operates in conjunction with the switch on the MT-16 card. For the most critical applications, set this to HOLD mode.

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-AD-23 Board

.EMP switch---insignificant (determined by the PLAYER tape)

-ENC-2 Board

.REC MUTE switch----OFF (if this is ON, no recording will take place, all zeroes will be transfered to the RECORDER)

-SIF-1 Board

.Fs selector---select the position of this switch according FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape (with respect to the PLAYER tape).

-MT-16 Board

.PEAK HOLD switch---selects the PEAK HOLD mode when the front panel switch is in the HOLD position. For the most critical applications it is recommended to use the PEAK OVER HOLD mode so that any time an overlevel condition occurs, the OVER LEDs remain illuminated to alert the operator of such a condition.

SETTING OF DAE-1100

-Front Panel

.DATA selector---------------SER
.SYNC selector---------------SER
.DROP FRAME selector---------select the position according to the time code used on the tapes. For CD mastering, use NDF.

-Rear Panel

.75-ohm terminatation switch (VIDEO IN)-------------ON

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142.**

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

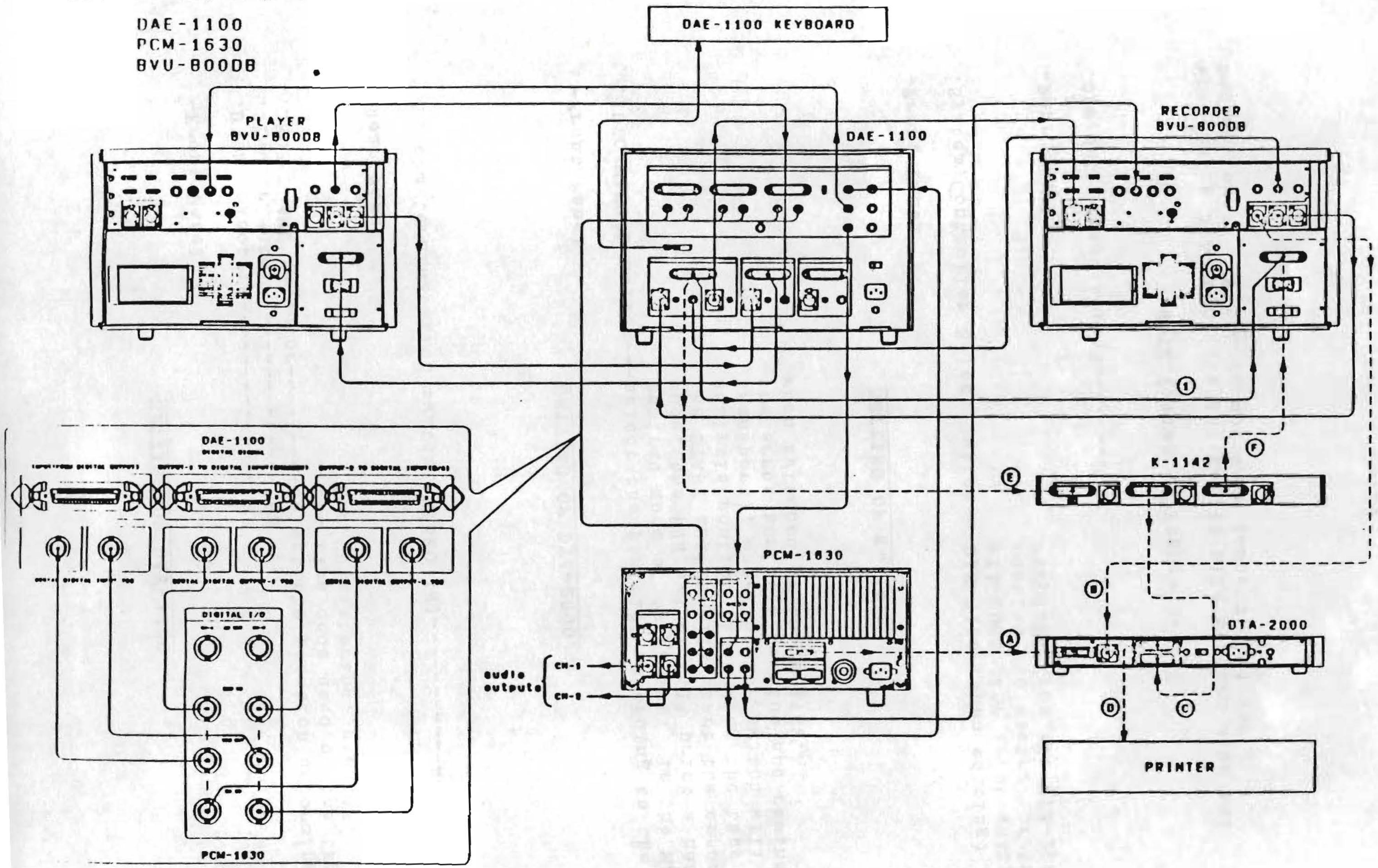
.DAE/DAQ Select switch--------DAE

NOTE (refer to Figure 2-42)

When using **DTA-2000,** use the **K-1142** PARA BOX and make the connections A - F and do not make connection 1 and 2.

Precise Editing with the Editor

DAE-1100
PCM-1630
BVU-800DB



2.6.11 DMR-4000/PCM-1610/DAE-1100A/DTA-2000/K-1142

SETTING OF DMR-4000 (RECORDER)

-Front Panel

```
.TRACKING control--------FIXED
.METER selector----------selects the source for the VIDEO/RF
                         meter for main (R/P) or confidence (CONFI)
                         head signals.  CONFI is always playback
                         from tape.  R/P is input video in RECORD.
.AUX LIMITER switch------insignificant
.RAW OUT selector--------SUB
.AUX CH-2 selector-------TIME CODE
.TIME CODE selector------REGEN
.REMOTE/LOCAL selector---REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector---REMOTE-2(36P)
.AUX MONITOR selector-----------------insignificant
.PB/PB/EE selector------PB/EE (fixed with a switch protector)
```

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---ON

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)-------insignificant

-TC-38 Board

```
.GENERATOR DF/NDF selector---for CD mastering use NDF, make sure
                             the EDITOR is set to the same
                             position as the RECORDER
```

-DM-49 Board

.Composite Digital Output switch---------OFF (NORMAL)

SETTING OF DAE-1100A (or DAE-1100+DABK-1100)

-Front Panel

```
.DATA selector----------------SER
.SYNC selector----------------SER
.DROP FRAME selector----------select the position according to
                              the time  code being used.  For
                              CD mastering, always use NDF.
                              The setting of this switch must
                              be the same as the setting of the
                              RECORDER machine GENERATOR DF/NDF
                              switch.
```

-Rear Panel

.IN SEL switches -------------ON

SETTING OF DMR-4000 (PLAYER)

-Front Panel

.TRACKING control----------------FIXED
.METER selector------------------R/P
.AUX LIMITER switch--------------insignificant
.RAW OUT selector----------------insignificant
.AUX CH-2 selector---------------TIME CODE
.TIME CODE selector--------------REC RUN
.REMOTE/LOCAL selector-----------REMOTE
.REMOTE-1(9P)/REMOTE-2(36P) selector---REMOTE-2(36P)
.AUX MONITOR selector------------------insignificant
.PB/PB/EE selector------PB/EE (fixed with a switch protector)

-Rear Panel

.75-ohm termination switch (COMPOSITE DIGITAL INPUT)---insignificant

-SY-37 Board

.TIME CODE AUTO STOP MODE switch (S1)---insignificant

-TC-38 Board

.GENERATOR DF/NDF selector---insignificant (generator inactive)

-DM-49 Board

.Composite Digital Output switch---------OFF (NORMAL)

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF PCM-1610

-Front Panel

```
.TIME CODE GENERATOR switch------insignificant
.MONITOR/METER switch------------PB
.MUTING mode switch--------------selects the muting indicator
                                 mode.  The LED can be set to
                                 stay lit until reset or to
                                 automatically turn off after
                                 the muting has ceased.
.D/A INPUT selector--------------EXTERNAL
.A/D INPUT selector--------------DIGITAL
```

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---insignificant (determined by PLAYER tape)

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

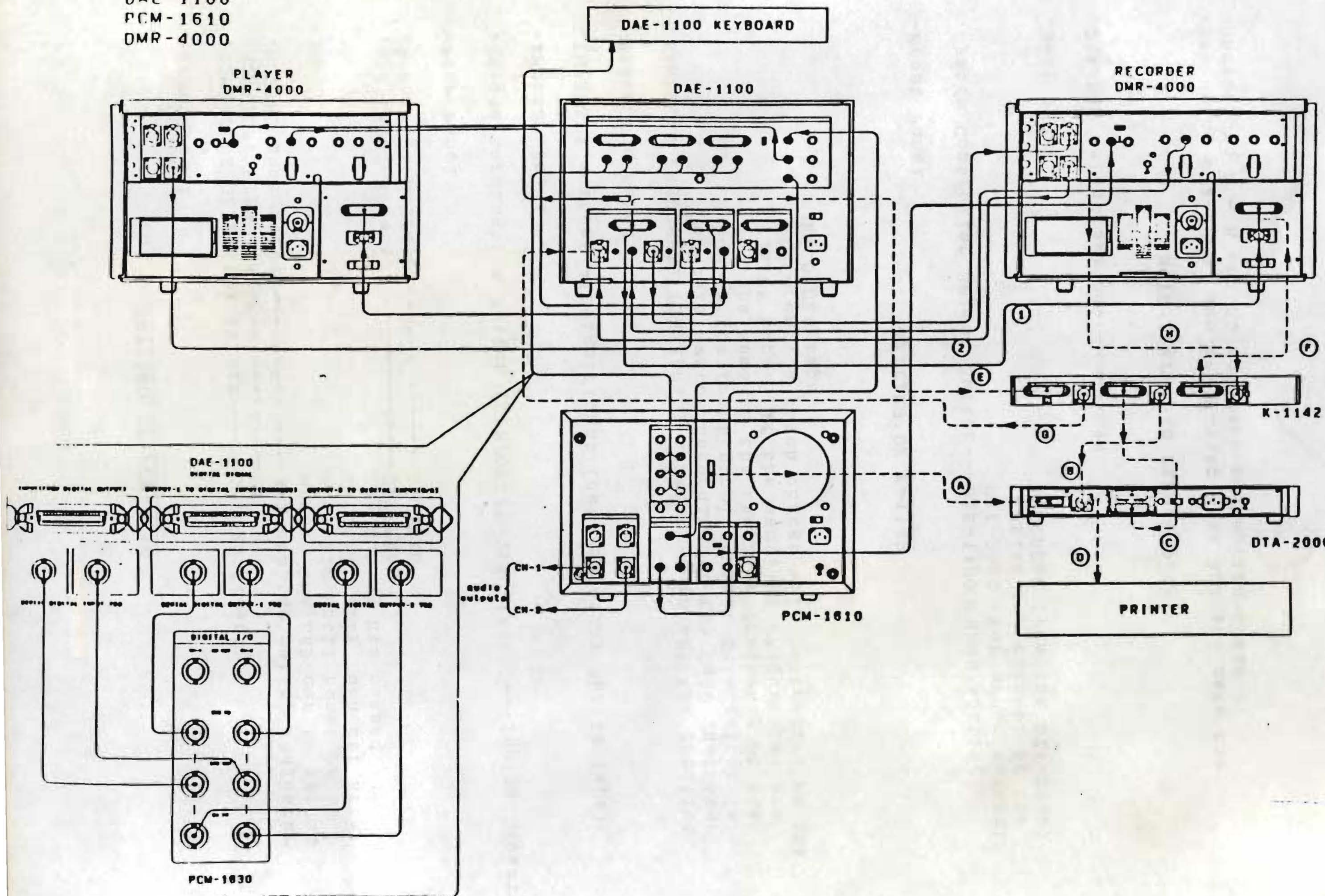
.DAE/DAQ Select switch--------DAE

NOTE (refer to Figure 2-43)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - H and do not make connection 1 and 2.

Precise Editing with the Editor

DAE-1100
PCM-1610
DMR-4000



2.6.12 DMR-2000/PCM-1610/DAE-1100/DTA-2000/K-1142

SETTING OF DMR-2000 (RECORDER)

-Front Panel

.TRACKING CONTROL------------------FIXED
.CH-2 switch-----------------------TIME CODE
.AUX LIMITER switch----------------insignificant
.MONITOR SELECT switch-------------insignificant
.REMOTE/LOCAL switch---------------REMOTE-2/LOCAL
.TIME CODE mode selector-----------REGEN
.MEMORY switch---------------------OFF

-Rear Panel

.NDF/DF selector-------------For CD mastering use NDF, make sure the EDITOR is set to the same position as the RECORDER

SETTING OF DMR-2000 (PLAYER)

-Front Panel

.TRACKING CONTROL------------------FIXED
.CH-2 switch-----------------------TIME CODE
.AUX LIMITER switch----------------insignificant
.MONITOR SELECT switch-------------insignificant
.REMOTE/LOCAL switch---------------REMOTE-2/LOCAL
.TIME CODE mode selector-----------AUTO STOP
.MEMORY switch---------------------OFF

-Rear Panel

.NDF/DF selector-------------------insignificant

SETTING OF PCM-1610

-Front Panel

.TIME CODE GENERATOR switch------insignificant
.MONITOR/METER switch------------PB
.MUTING mode switch--------------selects the muting indicator mode. The LED can be set to stay lit until reset or to automatically turn off after the muting has ceased.
.D/A INPUT selector--------------EXTERNAL
.A/D INPUT selector--------------DIGITAL

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---insignificant (determined by PLAYER tape)

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape.

SETTING OF DAE-1100

-Front Panel

.DATA selector-----------------SER
.SYNC selector-----------------SER
.DROP FRAME selector----------select the position according to the time code being used. For CD mastering, always use NDF. The setting of this switch must be the same as the setting of the RECORDER machine GENERATOR DF/NDF switch.

-Rear Panel

.VIDEO IN 75-ohm termination switch-------------ON

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

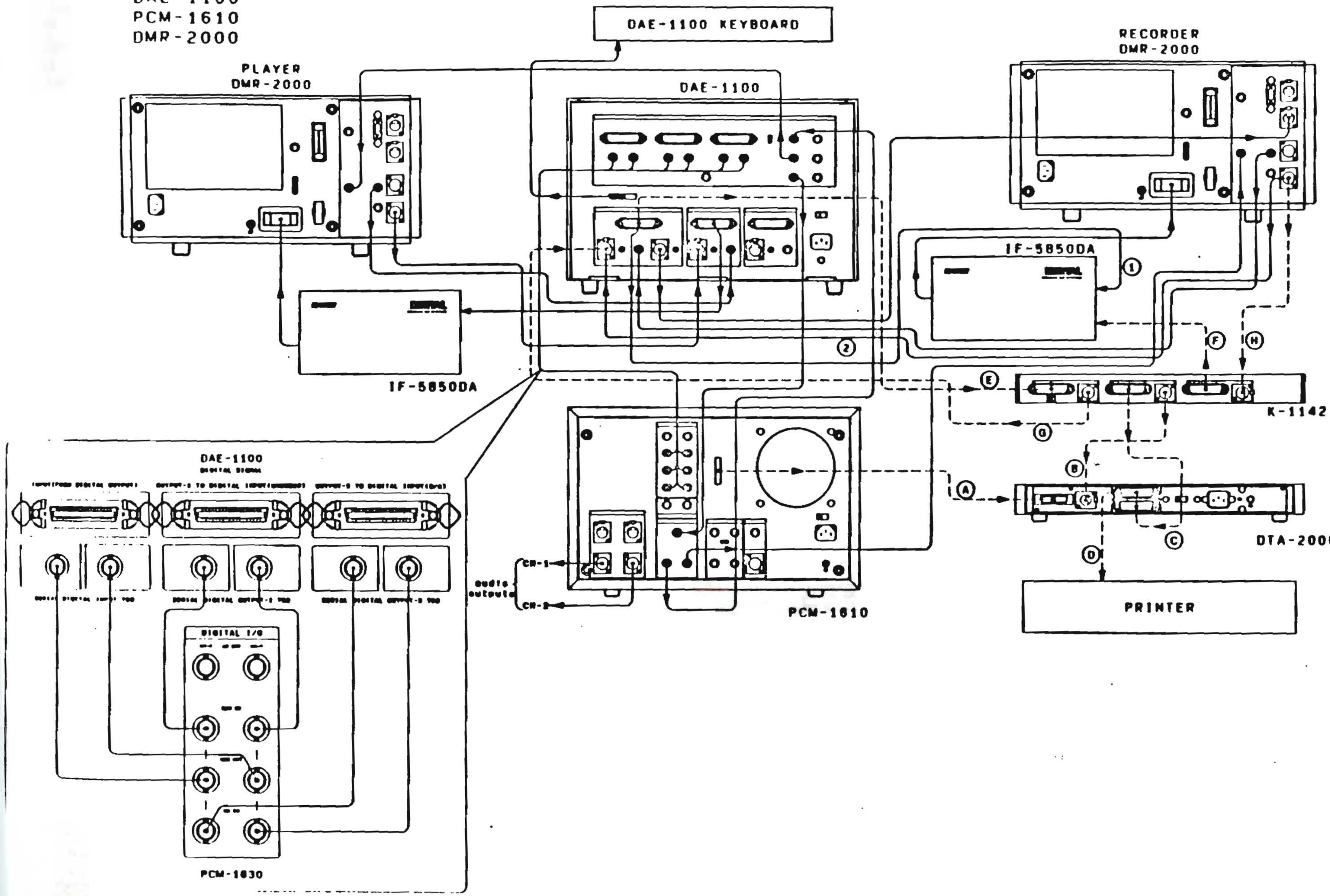
.DAE/DAQ Select switch--------DAE

NOTE (refer to Figure 2-44)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - H and do not make connection 1 and 2.

Precise Editing with the Editor

DAE-1100
PCM-1610
DMR-2000



2.6.13 BVU-800DB/PCM-1610/DAE-1100/DTA-2000/K-1142

SETTING OF BVU-800DB (RECORDER AND PLAYER)

-Front Panel

```
.TRACKING control---------------------FIXED
.TIME CODE switch---------------------TC TRACK
.AUDIO MONITOR selector---------------insignificant
.AUDIO LIMITER switch-----------------insignificant
.MIXING SELECT switch-----------------OFF            ┐
.MODE SELECT switch-------------------NORMAL         │ fixed with
.VIDEO INPUT SELECT switch------------LINE           │  switch
.REMOTE-1(9P)/REMOTE-2(36P)selector--REMOTE-2       │ protectors
.PB-PB/EE selector--------------------PB/EE          ┘
.REMOTE/LOCAL selector----------------REMOTE
```

-Rear Panel

```
.COLOR ON/OFF switch------------------OFF
.DOC ON/OFF switch--------------------OFF
.75-ohm ON/OFF switch (VIDEO IN)------ON
.AUDIO IN LEVEL selectors-------------HIGH (RECORDER)
                                      insignificant (PLAYER)
.600-ohm ON/OFF switches (AUDIO IN)--ON (RECORDER)
                                      insignificant (PLAYER)
```

SETTING OF PCM-1610

-Front Panel

```
.TIME CODE GENERATOR switch------insignificant
.MONITOR/METER switch------------PB
.MUTING mode switch--------------selects the muting indicator
                                 mode.  The LED can be set to
                                 stay lit until reset or to
                                 automatically turn off after
                                 the muting has ceased.
.D/A INPUT selector--------------EXTERNAL
.A/D INPUT selector--------------DIGITAL
```

-Rear Panel

.75-ohm termination switch (COMPOSITE SYNC INPUT)---insignificant

-Encoder Board

.EMPHASIS switch---insignificant (determined by PLAYER tape)

-Video Out Board

.SAMPLING FREQUENCY (INTERNAL) selector---select the position of this switch according to the FsID indicator LED on the front panel so that this switch is set the same as the sampling frequency on the PLAYER tape. If the sampling frequencies are different, a pitch change will be created on the RECORDER tape.

SETTING OF DAE-1100

-Front Panel

.DATA selector-----------------SER
.SYNC selector-----------------SER
.DROP FRAME selector----------select the position according to the time code being used. For CD mastering, always use NDF. The setting of this switch must be the same as the setting of the RECORDER machine GENERATOR DF/NDF switch.

-Rear Panel

.VIDEO IN 75-ohm termination switch-------------ON

SETTING OF DTA-2000

-Front Panel

.AUTO/MANUAL switch---select the position according to the desired mode of operation. In the MANUAL mode, the RUN switch will print a header, the START switch will start the error analysis routine (including the tape transport), and the STOP switch will end the error analysis routine and rewind tape when switched by the **K-1142**.

SETTING OF K-1142

-Front Panel

.System Controller Select Switch---**DAE-1100** (When editing)
DTA-2000 (For error analysis routine and control of the RECORDER from the **DTA-2000**)

-Rear Panel

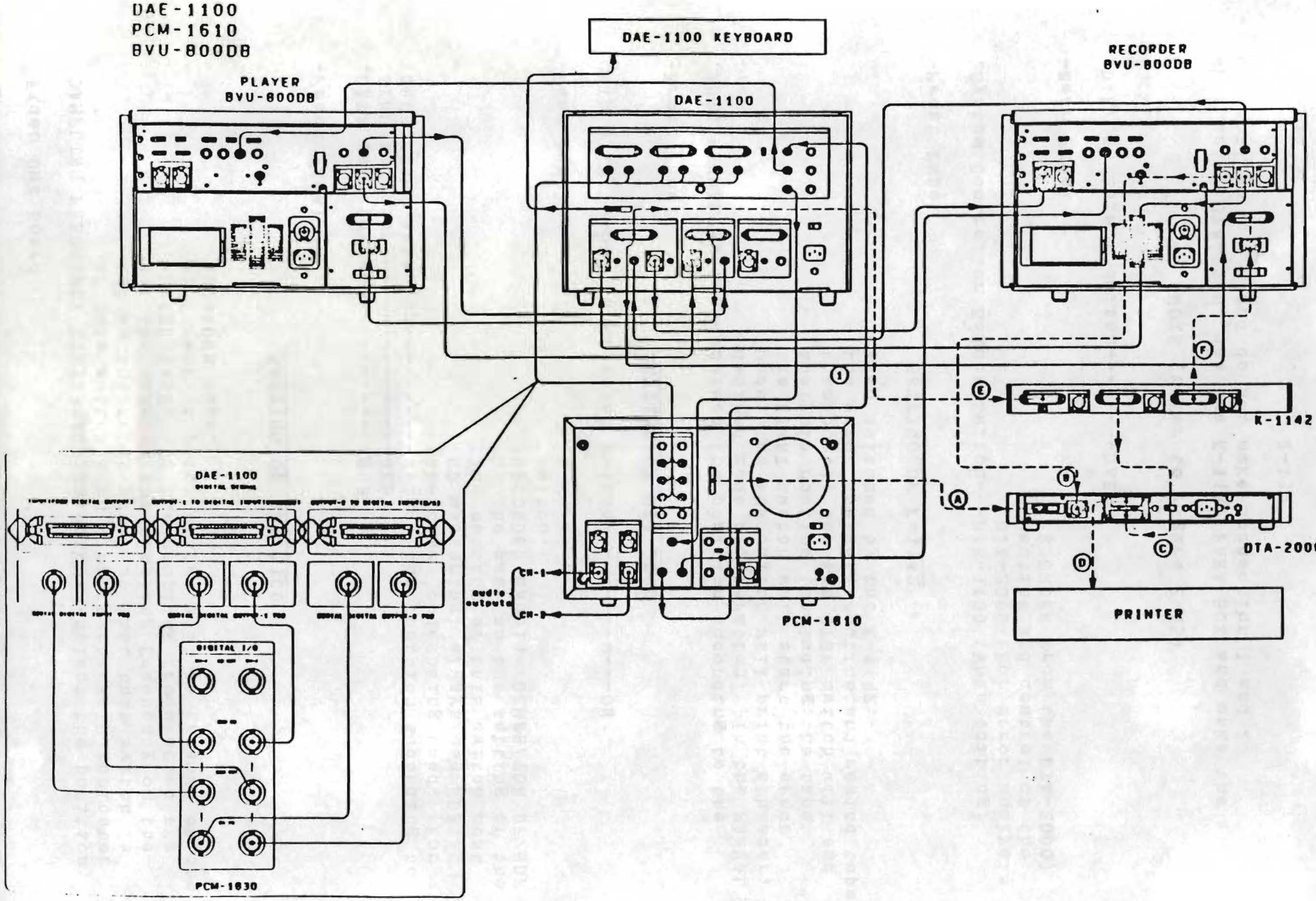
.DAE/DAQ Select switch--------DAE

NOTE (refer to Figure 2-45)

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - H and do not make connection 1 and 2.

Precise Editing with the Editor

DAE-1100
PCM-1610
BVU-800DB



2.7 PQ EDITING

This section describes the basic configurations available for PQ subcode editing. The PQ subcodes are added to the master tape for use by the CD mastering process. More specifically, the PQ subcodes make up the table of contents for the final product Digital Audio Compact Disc. From this information, the begin and end points of each song are marked along with the various index points (if desired). The **DAQ-1000** Cue Editor promulgates the PQ subcodes and records them to AUDIO CHANNEL-1 of the RECORDER rotary head machine at the top (beginning of the reel) of tape. If desired, a print-out of the PQ subcode information can also be obtained from the **DAQ-1000** built-in printer.

MODE	PAGE	NOTE
DIRECT MODE /EDIT MODE	2-143	As to the setting of the RECORDER, the PROCESSOR and the **DTA-2000**, refer to "C-1 Recorder and Playback"
EDITOR TRANSFER MODE	2-144	As to the setting of the PLAYER, the RECORDER, the PROCESSOR, the EDITOR and the **DTA-2000**, refer to "C-V Precise Editing with the Editor".

Table 2-6 PQ Subcode Editing Configurations

As to the setting of the RECORDER, the PROCESSOR and the **DTA-2000** refer to "C-1 Recording and Playback" except following switches:

.REMOTE/LOCAL selector **DMR-4000, BVU-800DB/DA**:REMOTE
.CH-1/L selector on **BVU-200B**: CH-1

To add the **DAQ-1000**, make the connections 1 - 5.

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - H. (In this case, do not make the connections 1 and 2.)

SETTING OF DAQ-1000

-Rear Panel

.600 Ω ON/OFF Select switch: OFF (when using **VO-5850(P)DA**)
ON (Otherwise)

SETTING OF K-1142

-Front Panel

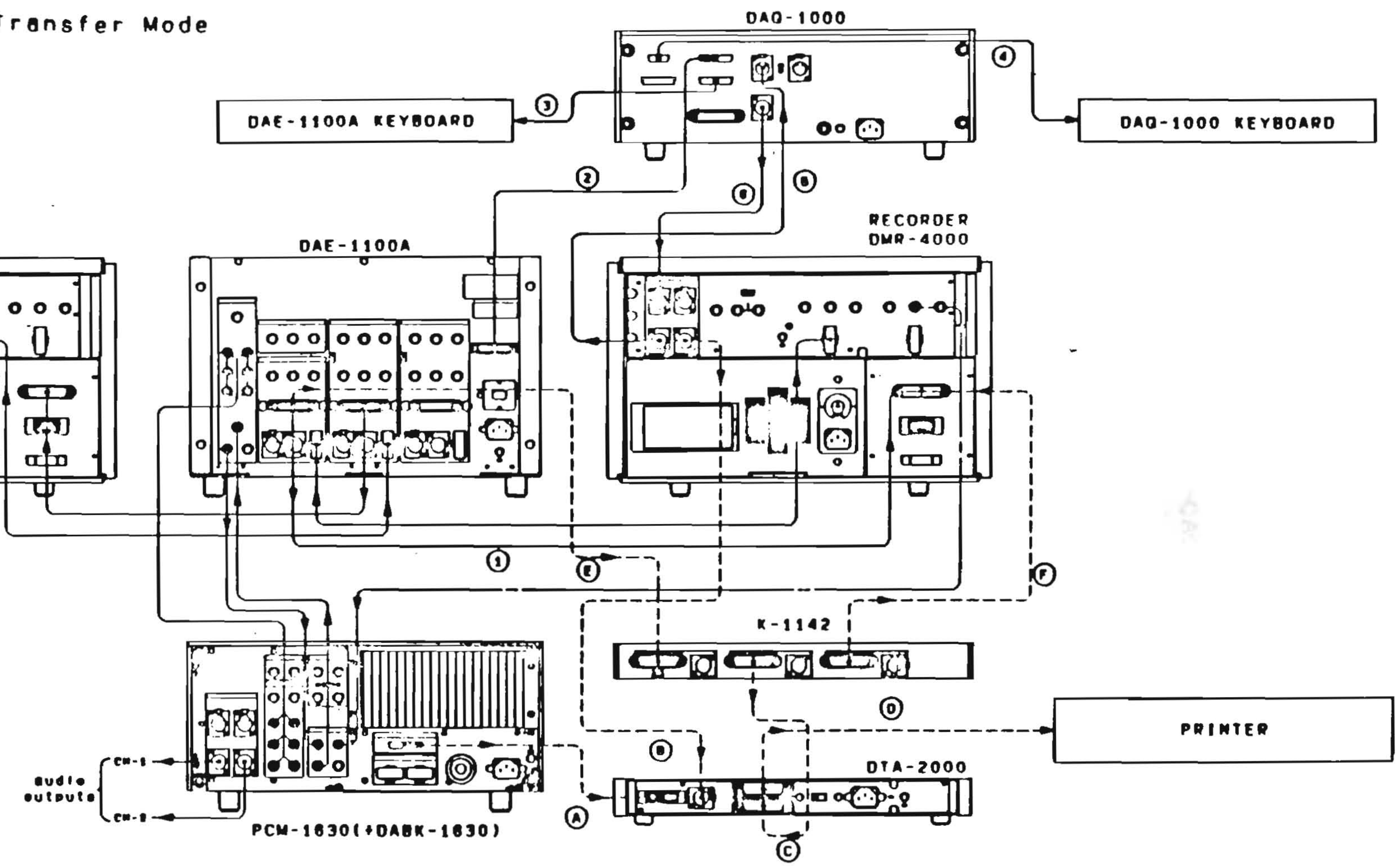
.System Controller Select switch: **DAE-1100** (When PQ editing)
DTA-2000 (When error analysis BY **DTA-2000**)

-Rear Panel

.DAE/DAQ select switch: **DAE**

PQ Editing

Editor Transfer Mode



As to the setting of the PLAYER, the RECORDER, the PROCESSOR the EDITOR, and **DTA-2000** refer to "C-V Precise Editing with the Editor" except following switch:

.CH-1/L selector switch on **BVU-200B**: CH-1

To add the **DAQ-1000**, make the connections 2 - 5.

When using **DTA-2000**, use the **K-1142** PARA BOX and make the connections A - H. (In this case, do not make the connections 1 and 2.)

SETTING OF DAQ-1000

-Rear Panel

.600 Ω ON/OFF Select switch:	OFF (when using **VO-5850(P)DA** as a RECORDER)
	ON (Otherwise)

SETTING OF K-1142

-Front Panel

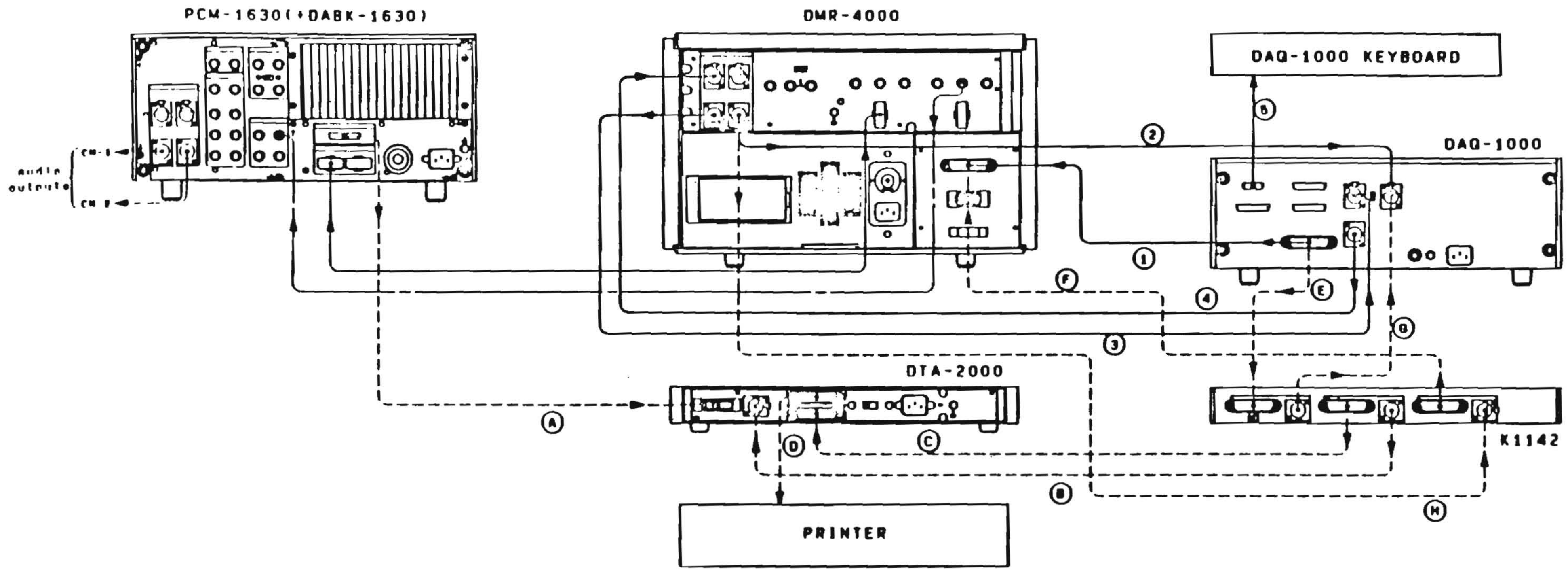
.System Controller Select switch:	**DAE-1100** (When editing or PQ editing)
	DTA-2000 (When error analysis controlling the RECORDER by **DTA-2000**)

-Rear Panel

.DAE/DAQ select switch:	**DAE**

PQ Editing

Direct Mode/Edit Mode



SECTION 3

CONTROLS AND INDICATORS

SECTION 3

CONTROLS AND INDICATORS

3.1 PCM-1630 PCM PROCESSOR

The **PCM-1630** PCM Processor is used to encode the digital audio signals for use by the rotary head recorders. When AD-23 and DA-15 cards are installed, it also has the capability of performing analog-to-digital and digital-to-analog audio conversions (standard). When DI and DO cards are installed in place, the **PCM-1630** only handles digital audio data in the AES/EBU format (to/from channel 1 connectors).

3.1.1 PCM-1630 Front Panel

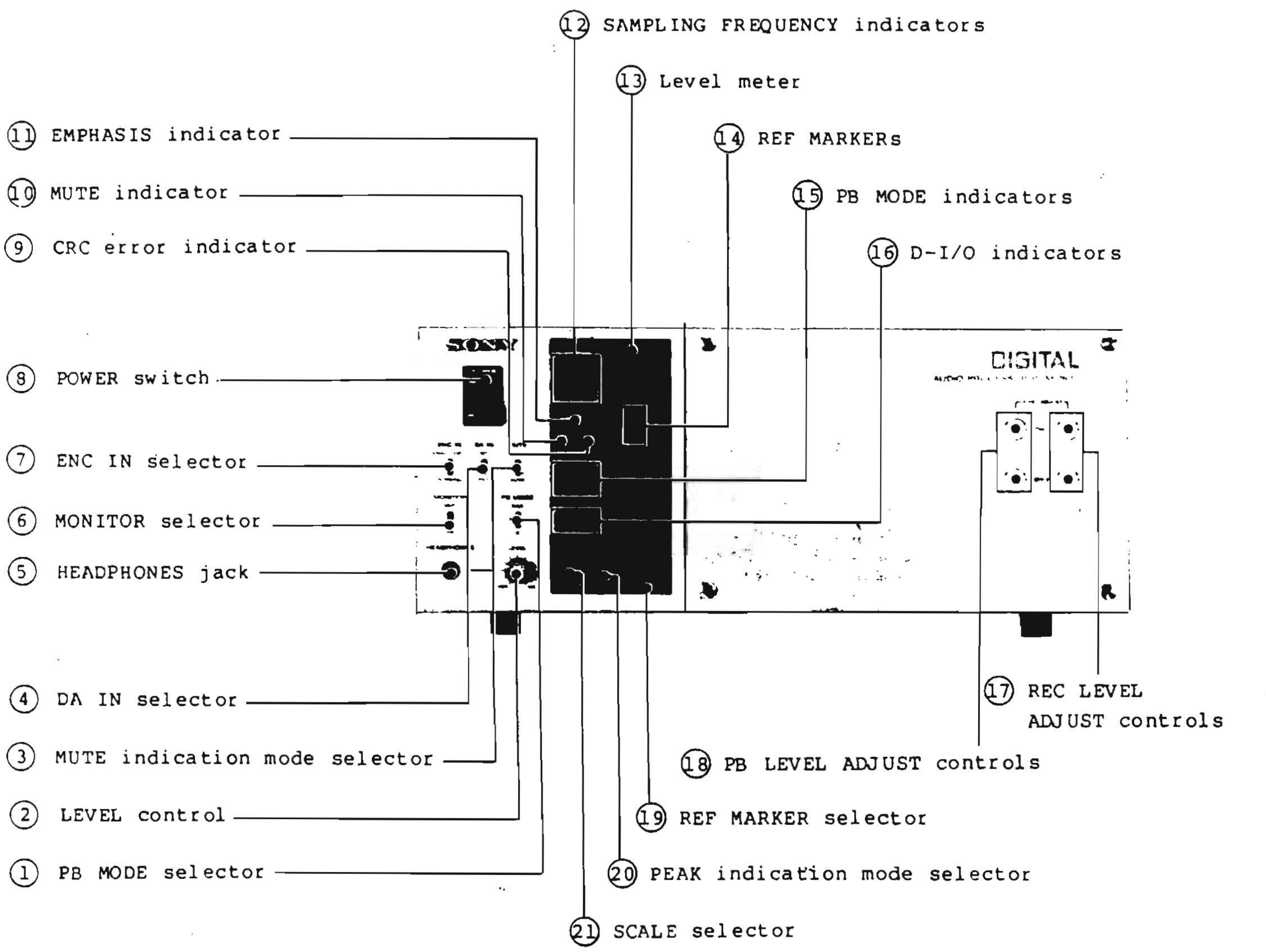


Figure 3-1 PCM-1630 Front Panel

1. PB (Playback) MODE selector

Used to select the playback signal source. The PB MODE indicators illuminate in accordance with the setting of this selector.

RAR: When an optional RAR-1 card **(DABK-1630)** is installed in the unit, the RAR (Read After Read) function activates when signals are input simultaneously to the COMPOSITE DIGITAL INPUT A and B connectors or to the COMPOSITE DIGITAL A and B connectors.

When an RAR-1 card is not installed, the unit operates the same as when this selector is set to "A" (the PB MODE "A" indicator illuminates).

A: The composite digital A input (input to the COMPOSITE DIGITAL INPUT A or COMPOSITE DIGITAL A connector) is selected as a playback signal. When optional RAR-1 board is installed in the unit and RAW (Read After Write) function of the board is used for dubbing or editing, set the selector position. For details, refer to the Operation and Maintenance Manual of the **DABK-1630** card.

B: The composite digital B input (input to the COMPOSITE DIGITAL INPUT B or COMPOSITE DIGITAL B connector) is selected as a playback signal.

2. LEVEL Control

Adjusts the volume of the headphones.

3. MUTE Indication Mode Selector

HOLD: Once the muting circuit activates, the MUTE indicator illuminates and stays lit until it is reset.

AUTO: The MUTE indicator lights up only when the muting circuit is active (during a muting condition).

4. DA IN (digital-to-analog input) Selector

Selects the data source to be routed to the input of the built-in D/A converter through the decoder.

INT: Signals input to the COMPOSITE DIGITAL INPUT connectors (BNC type) or the COMPOSITE DIGITAL connectors (8-pin) are selected (routed through the internal decoder).

EXT: Data signals input to the DA IN connectors (in the DIGITAL I/O connector section) are selected through another internal decoder.

5. HEADPHONES Jack (stereo phone jack)

Connect stereo headphones with an 8-ohm impedance.

6. MONITOR Selector

REC: Selects the digital audio signals from the RECODER for monitoring and level meter indication.

PB: Selects the digital audio signals from the PLAYER for monitoring and level meter indication.

7. ENC IN (Encoder Input) Selector

Selects the source data to the built-in encoder.

ANALOG (D-I): Selects the signals input to the ANALOG INPUT connectors.

DIGITAL: Selects the signals input to the ENC IN connectors (in the DIGITAL I/O connector section).

DUBBING: Selects the signals input to the COMPOSITE DIGITAL INPUT or COMPOSITE DIGITAL connectors.

8. POWER Switch

Turns the power on and off.

9. CRC (Cyclic Redundancy Check Code) Error Indicator

This indicator illuminates when the unit detects a CRC error in the playback signal.

10. MUTE Indicator

This indicator illuminates when the muting circuit activates, it turns off depending upon the setting of the MUTE indication mode selector.

11. EMPHASIS Indicator

This indicator illuminates when input data contains a pre-emphasis (EMPHASIS bit on), and the de-emphasis circuit of the unit activates.

12. SAMPLING FREQUENCY Indicators

Each indicator illuminates, depending upon the sampling frequency (44.056 or 44.1kHz) of the internal sync signal (INT), external sync signal (EXT) or signal from the tape being played back (FsID).

13. LEVEL Meter

The indicators on the level meter illuminate to indicate the input level of each channel during recording, and the recorded level during playback, depending upon the setting of the MONITOR selector and the PEAK indication mode selector. The scale of the level meter can be enlarged with the SCALE selector for easy and precise reading of the meter.

The OVER level indicators at the top of the indicator column for each channel illuminate to warn of an audio overload condition indicating that there is no headroom (all bits have been used).

14. REF (reference) MARKERS

The indicator corresponding to the reference level (-10 dB to -20 dB) set with the REF MARKER selector illuminates so that the reference signal input level can be adjusted easily. This only controls the LED indicator and has no other affect on the processor functions.

15. PB (playback) MODE Indicators

These indicators illuminate in accordance with the setting (RAR, A or B) of the PB MODE selector. The A indicator also illuminates when the PB MODE selector is set to RAR, without an optional RAR-1 board installed in the unit.

16. D-I/O (digital input/output) Indicators

The D-I or D-O indicator illuminates, depending upon whether the optional digital input or output cards are installed.

D-I: Illuminates when an optional DI-5 card is installed in the unit instead of the AD-23 card.

D-O: Illuminates when an optional DO-17 card is installed in the unit instead of the DA-15 card.

17. REC (recording) LEVEL ADJUST Controls

The recording level can be adjusted with these controls within a range of approximately +/-12dB. Clockwise rotation increases the signal level.

18. PB (playback) LEVEL ADJUST Controls

The output level of the playback signal can be adjusted with these controls within a range of approximately +/-12 dB. Clockwise rotation increases the playback signal level.

19. REF (reference) MARKER Selector

This selector sets the reference signal level within a range of -10dB to -20dB in 2dB steps. The selected reference level is indicated by the illumination of the corresponding **REF MARKER** indicator. The reference marker only affects thje metering of the processor. When the SCALE indicator switch is set to the FINE position, the reference marker will determine the metering window for the fine resolution scale.

20. PEAK Indication Mode Selector

Selects the manner in which peaks are indicated on the level meter. This selector is effective when the PEAK HOLD switch (SW1) on the MT-16 board is set to ON.

HOLD: The level meter indicates the level of the highest peak while simultaneously following the level of transient peaks below the highest peak. The peak level will be held on the scale until a higher peak occurs, in which case the higher peak is held.

AUTO: Successive peaks are held on the scale for approximately 1.5 seconds, except when a higher peak occurs before 1.5 seconds have elapsed, in which case that peak is immediately indicated and held for 1.5 seconds. When the mode select switch (SW4) on the MT-16 board is set to ON, the peaks are held for approximately 4 seconds.

When the PEAK HOLD switch on the MT-16 board is set to OFF, the level meter activates as a normal peak indicator meter.

21. SCALE Selector

This selector selects the scale of the level meter.

FINE: The level meter scale is enlarged, the resolution is increased, and the signal level is indicated in 0.2dB steps. If the signal level is above the maximum level of the enlarged scale, the LED of 0dB will blink, and if the signal level is below the minimum level, the LED of -60dB will blink. When this mode is used, the -60dB LED will indicate a signal level equal to the reference marker and each segment value is 0.2dB.

NORMAL: The level meter scale is as indicated on the front panel.

3.1.2 PCM-1630 Rear Panel

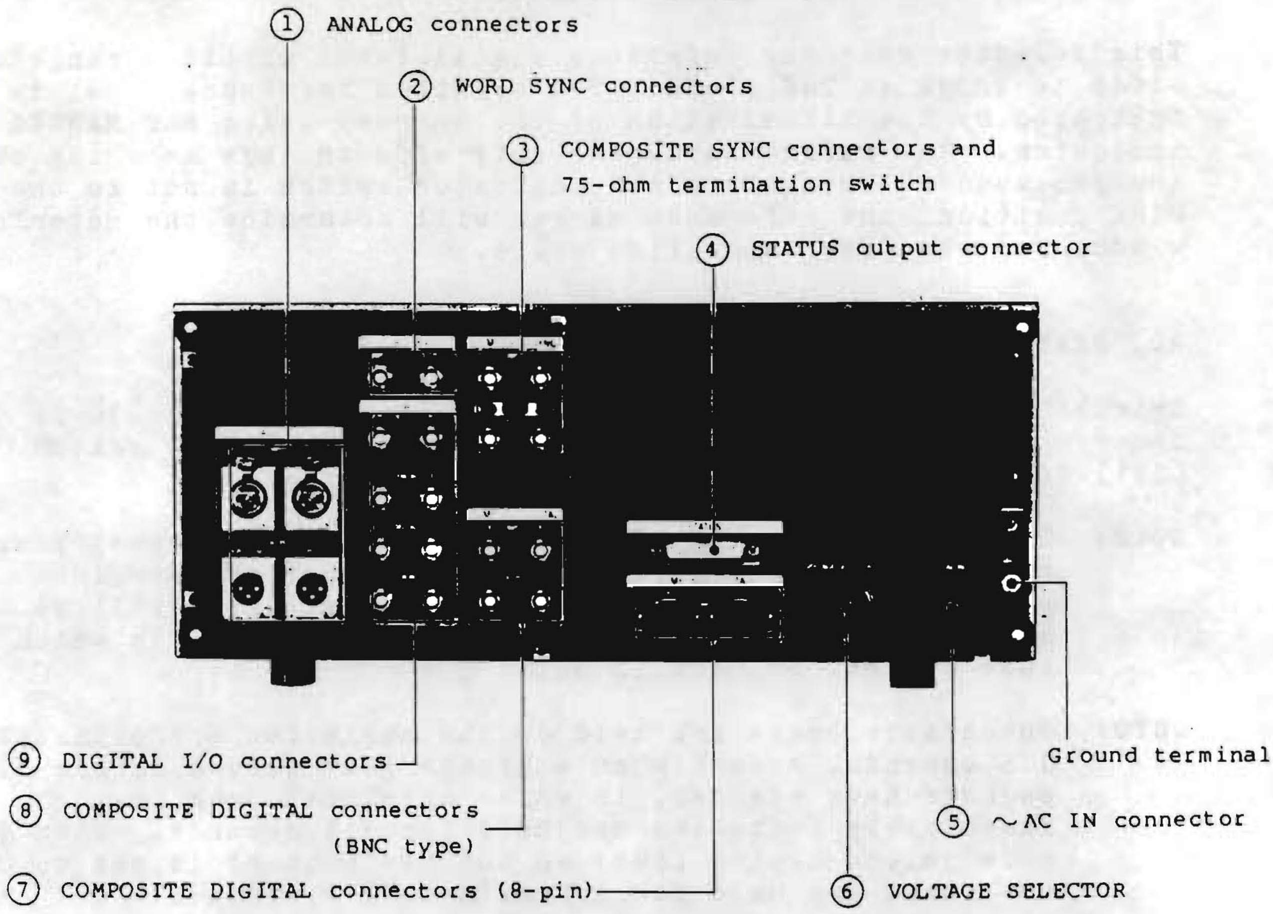


Figure 3-2 PCM-1630 Rear Panel

1. ANALOG Connectors (equivalent to Cannon XLR type)

Analog audio signals are input to or output from these connectors when the standard AD-23 and DA-15 cards are installed.

When optional **DABK-1631** digital I/O boards are installed (instead of using the AD-23 and DA-15 boards) providing the unit with a digital interface which conforms to the AES/EBU standards, supply a digital input signal to the INPUT CH-1 (D-I) connector. The digital output signal from the processor is supplied from the OUTPUT CH-1 (D-O) connector.

2. WORD SYNC connectors (BNC type)

A word sync signal of 44.1kHz or 44.056kHz is input to the WORD SYNC INPUT connector or output from the WORD SYNC OUTPUT connector.

3. **COMPOSITE SYNC Connectors (BNC type) and 75-ohm Termination Switch.**

These connectors are input (COMPOSITE SYNC INPUT 1, 2) and output (COMPOSITE SYNC OUTPUT 1, 2) connectors for a composite sync signal. To terminate the INPUT connectors, set the 75-ohm termination switch to ON. Set the termination switch to OFF to create a looping output (bridge connection).

4. **STATUS Output Connector (25-pin D-sub type)**

Signals containing status information, such as error flags, are output from this connector. These are used by the **DTA-2000** in order to accumulate a listing of the errors on the tape. The connector output circuits except for the RS-422 circuits have open-collector configurations requiring a pull-up to the power supply to work.

PIN ASSIGNMENTS

Pin No.	Signal	Remarks	
1	GND	Ground for $A/\overline{B}$	
2	$A/\overline{B}$	$A/\overline{B}$ select	
3	$\overline{REC}/PB$		
4	FG	Frame ground	
5	$\overline{HLD}$	Hold	
6	GND	Ground for $\overline{HLD}$	
7	GND	Ground for $\overline{PAR}$	
8	---	N. C.	
9	$\overline{AVE}$	Average	
10	GND	Ground for $\overline{AVE}$	
11	$\overline{CRC}$	CRC error	
12	GND	Ground for $\overline{CRC}$	
13	FsID	44.056 kHz: 'H' 44.1 kHz: 'L'	
14	EMP	Emphasis ON: 'H'	
15	GND	Ground for $\overline{MUTE}$	
16	$\overline{MUTE}$	Muting	
17	$\overline{WCLK}$	Word clock	RS-422
18	WCLK		RS-422
19	BCLK	Bit clock	RS-422
20	$\overline{BCLK}$	(25-slot)	RS-422
21	ME CH-1	CH-1 data	RS-422
22	$\overline{ME\ CH\text{-}1}$	(25-slot)	RS-422
23	ME CH-2	CH-2 data	RS-422
24	$\overline{ME\ CH\text{-}2}$	(25-slot)	RS-422
25	$\overline{PAR}$	Parity error	

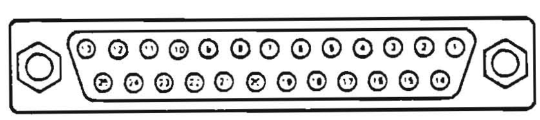


Figure 3-3 Status Connector Pin Assignments

5. **AC IN (input) Connector**

Connect to an AC outlet using the supplied ac power cord.

6. **VOLTAGE SELECTOR**

The operating voltage of the unit can be set to 100, 120, 220, or 240 VAC with this voltage selector. To reset the voltage selector, refer to the **PCM-1630** Operation and Maintenance Manual section 1-4-1.

7. **COMPOSITE DIGITAL (video) Connectors (8-pin multi-connectors)**

COMPOSITE DIGITAL A: Main composite digital input (connected in parallel with the COMPOSITE DIGITAL INPUT A BNC connector 8 inside) and composite digital output.

COMPOSITE DIGITAL B: Auxiliary composite digital input (connected in parallel with the COMPOSITE DIGITAL INPUT B BNC connector 8 inside) and composite digital output.

PIN ASSIGNMENT

Pin No.	Signal	Remarks
1	---	N. C.
2	C. D. IN	Composite digital input
3	GND	Ground for C. D. out
4	C. D. OUT	Composite digital output
5	---	N. C.
6	GND	Ground for C. D. IN
7	$\overline{\text{SEL}}$	Connect to ground
8	---	N. C.

NOTE: SELECT ($\overline{\text{SEL}}$) is a status command line for the **DMR-4000** and **DMR-2000** Digital Master Recorders. This line is held to a level of approximately +10.4VDC (logic high) through a pull-up resistor in the **DMR-2000** and left at a high impedence (floating) state in the **DMR-4000**. When the 8-pin cable is connected to the **PCM-1630**, this line is connected to ground (logic low) which activates the BNC/8-pin disable circuit in the DMR machines. When activated, this circuit will disaconnect the BNC signal path and connect the 8-pin signal path instead by way of relay and semi-conductor analog switching circuitry. This is done so that the inputs will not be active at the same time with the 8-pin inputs having priority when the 8-pin cable is connected at both ends.

Figure 3-4 8-pin Connector Pin-out

8. COMPOSITE DIGITAL (video) Connectors (BNC type)

COMPOSITE DIGITAL INPUT A: Main composite digital input.

COMPOSITE DIGITAL INPUT B: Auxiliary composite digital input.

COMPOSITE DIGITAL OUTPUT 1 and 2: Parallel composite digital outputs.

9. DIGITAL I/O (input/output) Connectors (BNC type)

AD OUT (analog-to-digital output): data from the A/D convertors is output from these connectors.

ENC IN (encoder input): Data for input to the built-in encoder can be supplied to these connectors.

DEC OUT (decoder output): Data from the built-in decoders is output from these connectors.

DA IN (digital-to-analog input): Digital data to be routed to the D/A converters can be input to these connectors.

3.1.3 Internal Switches and Indicators

The printed circuit boards (cards) are installed behind the right front panel. To adjust the controls and switches on the printed circuit boards, take off the right front panel by removing the four screws with a coin or a large screwdriver. Refer to Figure 3-5.

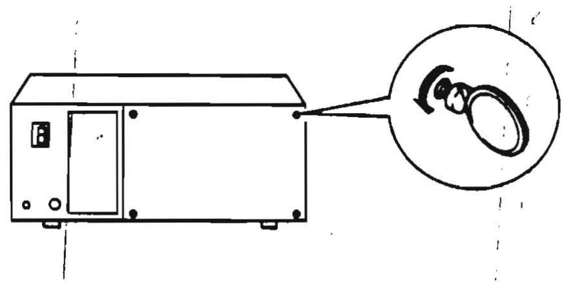


Figure 3-5 Front Panel Latches

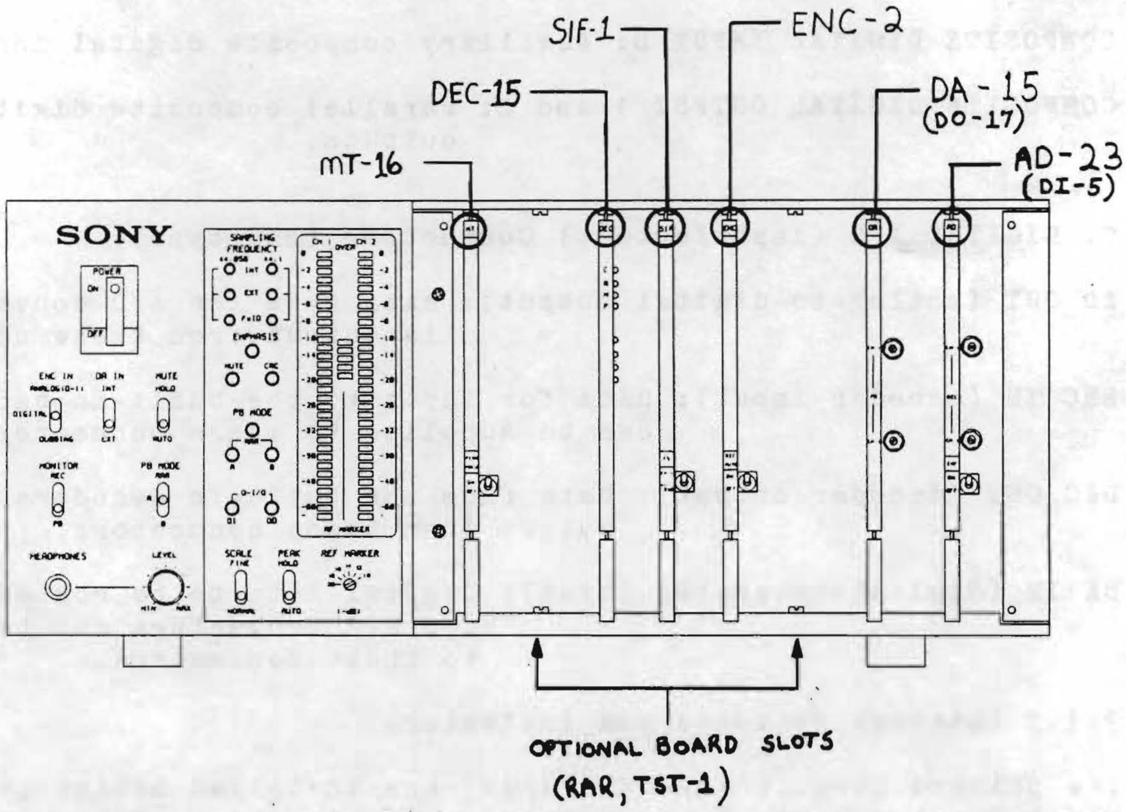


Figure 3-6 Card Rack of the PCM-1630

3.1.4 AD-23 BOARD

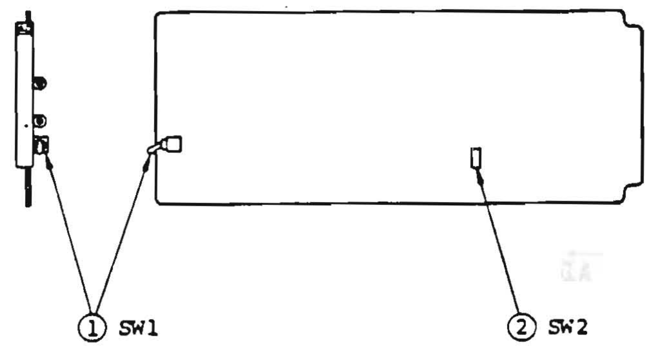


Figure 3-7 AD-23 Switches

3.1.4.1 SW1: EMP (Emphasis) Switch

This switch activates (ON) or deactivates (OFF) the emphasis circuitry during recording.

When this switch is set to ON, the high-frequency response is boosted automatically during recording (pre-emphasis, with a time constant of 50 usec./15 usec.). The high-frequency content of the signal is cut during playback (de-emphasis) to reduce the amount of noise upon reading of the EMPHASIS bit within the digital audio data signal. Subjectively, it has been said that EMPHASIS will improve the quality of the sound and in some cases also improve the signal-to-noise ratio.

When this switch is set to OFF, a recording is made with the flat frequency response and the EMPHASIS bit in the digital audio data is set to off. The EMP switch is factory preset to OFF.

3.1.4.2 SW2: Dither Switch

This switch activates (ON) or deactivates (OFF) the dither generator circuit.

When this switch is set to ON, a low level audio signal (dither) is mixed with the incoming audio signals. This is done in order to randomize audible noise caused by quantization error and therefore minimize the effects of the noise. Although the dither level is set at less than 1 LSB, the overall noise level will be raised somewhat when the switch is set to ON, but the noise will be randomized white noise components which will have less effect on the audible output signals.

This switch is factory preset to OFF.

3.1.4.3 Emphasis Identification Bits

The setting of the EMP switch does not affect the emphasis identification bits during playback mode. The affect of the switch in the output signal data is dependent on the setting of the ENC IN selector on the front panel as shown in the table below. The relationships between the setting of the ENC IN selector and the emphasis identification bits are as follows:

Output signal / ENC IN selector	AD OUT connector	COMPOSITE DIGITAL OUTPUT connector	DEC OUT connector
ANALOG	ON/OFF of the EMP switch on the AD board	ON/OFF of the EMP switch on the AD board	Irrelevant*
DIGITAL	ON/OFF of the EMP switch on the AD board	ON/OFF of the emphasis bits in the digital signal data input to the ENC IN connector	Irrelevant*
DUBBING	ON/OFF of the EMP switch on the AD board	ON/OFF of the emphasis bits in the signal data input to the COMPOSITE DIGITAL INPUT connector	ON/OFF of the emphasis bits in the signal data input to the COMPOSITE DIGITAL INPUT connector

* In the E-to-E or playback mode, the emphasis depends upon the ON/OFF status of the emphasis identification bits in the signal data input to the COMPOSITE DIGITAL INPUT connector(s).

Table 3-1 Emphasis Bits

The de-emphasis circuit for playback is activated (ON) or deactivated (OFF) depending on the EMPHASIS bits in the digital audio data. The source of the data depends upon the setting of the DA IN selector as shown in the table below.

DA IN selector	ON/OFF status of the de-emphasis*
INT	ON/OFF status of the emphasis identification bits in the signal data input to the COMPOSITE DIGITAL INPUT connector
EXT	ON/OFF status of the emphasis identification bits in the signal data input to the DA IN connectors in the DIGITAL I/O connector section

*The EMPHASIS indicator on the front panel lights up or goes off in accordance with the ON/OFF status of the de-emphasis circuit. The emphasis status signal output from the STATUS connector on the rear panel automatically matches the ON/OFF status of the de-emphasis circuit.

Table 3-2 De-emphasis Status

3.1.5 ENC-2 BOARD

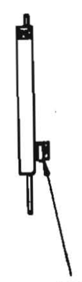


Figure 3-8 ENC-2 Switches

3.1.5.1 SW1: REC MUTE (record muting) Switch

To record a muting signal (all digital audio data bits are set to "0"), set the switch to ON. Signals input to the ANALOG INPUT connectors are ignored, and output signals from the COMPOSITE DIGITAL OUTPUT or COMPOSITE DIGITAL connectors are changed into mute data signals.

During normal operation, be sure to set the switch to OFF.

The switch is factory preset to OFF.

3.1.6 SIF-1 Board

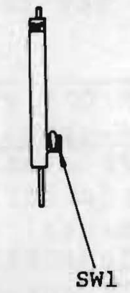


Figure 3-9 SIF-1 Switches

3.1.6.1 SW1: FS (sampling frequency) Selector

This switch selects the sampling frequency when the unit operates in the internal sync mode:

44.1kHz (upper position)
44.056kHz (lower position)

The selected sampling frequency is indicated by the corresponding INT SAMPLING FREQUENCY indicator on the front panel.

When the unit operates in the external sync mode, the sampling frequency is determined by the frequency of the external sync signal input to the unit. Therefore, the setting of this selector has no effect upon the sampling frequency.

This selector is factory preset to 44.1kHz.

3.1.7 DEC-15 Board

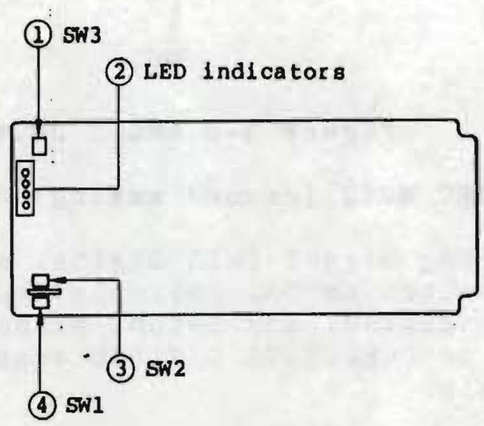


Figure 3-10 DEC-15 Switches and Indicators

3.1.7.1 SW3

This DIP switch is provided as a servicing aid to check the functions of the unit. The switch is factory preset as follows:

Switch No.			
1	2	3	4
ON	ON	OFF	OFF

Do not change the setting of the switches as this will affect the threshold level of the ATC circuit

Table 3-3 SW3 Servicing Switch Normal Operation Settings

3.1.7.2 LED Indicators

The LED indicators indicate the error status of the data being reproduced. The illumination of the indicators shows:

C (green): Correction
A (yellow): Average
H (red): Hold
P (red): Parity error

3.1.7.3 SW2: Muting Time/Muting ON/OFF switch

This DIP switch determines whether the muting circuit activates or not when an error occurs, and sets the muting time of the muting circuit. The muting time determines how long after the mute condition has ceased that the muting circuit will remain active (or the minimum mute time).

Switch No. 4 activates (ON) or deactivates (OFF) the muting circuit. When switch NO. 4 is set to OFF, the muting circuit is inactive and does not mute the audio signals.

The muting time can be set with switches No. 1 to No. 3 as follows. The adjustable range is from 1/60 seconds to approximately 2 seconds as shown in the table below:

Switch No.				Muting time
1	2	3	4	
x	x	x	OFF	Muting OFF
OFF	OFF	OFF	ON	1/60 sec.
ON	OFF	OFF	ON	1/30 sec.
OFF	ON	OFF	ON	1/15 sec.
ON	ON	OFF	ON	About 0.1 sec.
OFF	OFF	ON	ON	About 0.3 sec.
ON	OFF	ON	ON	About 0.5 sec.
OFF	ON	ON	ON	About 1 sec.
ON	ON	ON	ON	About 2 sec.

Table 3-4 Muting Control DIP Switch

3.1.7.4 SW1: M-SENS (Muting Sensitivity) switch

This DIP switch adjusts the sensitivity of the muting circuit, that is, it determines how quickly the muting circuit activates when errors occur during digital audio reproduction from data on tape. When switch No. 1 only is set to ON, the muting circuit activates for the time set by the muting time/muting ON/OFF switch (SW2), if errors occur in succession for a period of approximately 20H (H - horizontal lines). When switch No. 2 only is set to ON, a succession of errors for approximatley 10H activates the muting circuit. Similarly, when switch No. 3 only set to ON and when switch No. 4 only is set to ON, a succession of errors for the times shown below activates the circuit:

SW1

Switch No.				Succession
1	2	3	4	of errors
ON	OFF	OFF	OFF	20 H
OFF	ON	OFF	OFF	10 H
OFF	OFF	ON	OFF	5 H
OFF	OFF	OFF	ON	2 to 3 H

Table 3-5 Muting Sensitivity Control DIP Switch

When any of or all of the switches are set to ON simultaneously, a succession of errors for the total time set with these switches activates the muting circuit. The minimum sensitivity is 32H, the maximum sensitivity is 2 to 3H. The muting sensitivity switch is factory preset to 20H (Switch No. 1 ON, and Switches No. 2, 3, and 4 to OFF).

3.1.8 MT-16 board

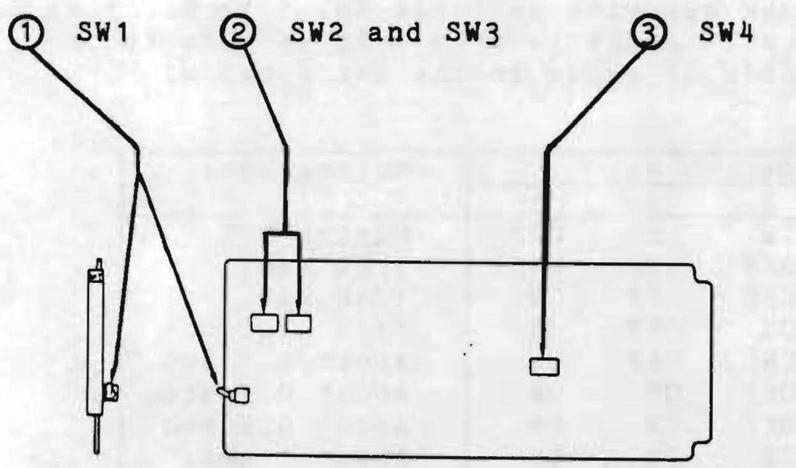


Figure 3-11 MT-16 Switches

3.1.8.1 SW1: PEAK HOLD Switch

This switch selects the function of the level meter; as a peak hold meter or a standard peak level indicator meter.

ON: The level meter functions as a peak hold meter. The level of the highest peak is indicated and held on the scale for approximately 1.5 seconds (can be set to 4 seconds) when the PEAK indication mode selector on the front panel is set to AUTO, or until a higher peak occurs when the PEAK indication mode selector on the front panel is set to HOLD. This switch is factory preset to ON.

OFF: The level meter functions as a peak meter. When this switch is set to OFF, the setting of the PEAK indication mode selector on the front panel has no effect upon the level meter indication, and peak levels are not held on the scale even if the PEAK indication mode selector is set to HOLD.

3.1.8.2 SW2 for Channel 1 and SW3 for Channel 2: Overload indication adjustment switches

These DIP switches set the number of words of full-scale signals (overload signals - all bits used) continuously input to the unit, before the OVER level indicator on the level meter will illuminate. Between 1 to 8 words can be set for each channel with these switches.

SW2 (SW3)

Switch No.								Number of words
1	2	3	4	5	6	7	8	
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	1
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	2
ON	ON	ON	OFF	OFF	OFF	OFF	OFF	3
ON	ON	ON	ON	OFF	OFF	OFF	OFF	4
ON	ON	ON	ON	ON	OFF	OFF	OFF	5
ON	ON	ON	ON	ON	ON	OFF	OFF	6
ON	ON	ON	ON	ON	ON	ON	OFF	7
ON	ON	ON	ON	ON	ON	ON	ON	8

Table 3-6 Overlevel Indicator Sensitivity DIP Switches

These switches are factory preset to 3 words (Nos. 1 to 3 are set to ON, and Nos. 4 to 8 OFF.)

3.1.8.3 SW4: Mode Select Switch

This DIP switch selects the level meter indication modes. It sets the peak hold time and release time, and determines whether the overlevel indication is to be held or not. When overlevel indication is held, the OVER LEDs will illuminate when an overlevel condition occurs (see section 3.1.8.2 for the setting of the sensitivity) and remain illuminated until reset by power down or front panel switch.

SW4

Switch No.	Indication mode	Switch position ON	Switch position OFF
1	Peak hold time	About 4 sec.	About 1.5 sec.
2	Release time	About 100 msec.	About 50 msec.
3	Overlevel level	Not held	Held
4 to 8	Not used		

All the switches are factory preset to OFF.

Figure 3-7 Metering Mode Select DIP Switch

3.1.8.4 Reference Signal Level and Headroom

Headroom describes the difference between the reference signal level and maximum permissible the full-scale level before clipping. In digital audio, the full-scale signal is obtained when all of the bits are used to describe the voltage level of any given sample. The headroom can be adjusted within a range from 20dB to 10 dB in 2-dB steps, which is determined by the adjustable range (about 12dB) of the REC LEVEL ADJUST controls. The adjustable range of the headroom is greatest when the reference signal level is +4dB (0dBm = 0.775Vrms). The maximum input level is +24dB and therefore the headroom is 20dB. Since the REC LEVEL ADJUST controls do not reduce the gain, the headroom will be less than 20dB when the reference signal level is above +4dB, while the headroom will be more than 10dB when the reference signal level is less than +4dB.

The reference signal levels and their corresponding adjustable headroom ranges are shown below:

Reference signal level	Headroom range
-6 dB	20 dB
-4 dB	18 - 20 dB
-2 dB	16 - 20 dB
0 dB	14 - 20 dB
+2 dB	12 - 20 dB
+4 dB	10 - 20 dB
+6 dB	10 - 18 dB
+8 dB	10 - 16 dB
+10 dB	10 - 14 dB
+12 dB	10 - 12 dB
+14 dB	10 dB

(0 dB = 0.775Vrms)

Table 3-8 Reference Level and Headroom Range

3.1.8.5 Level Meter

The level meter indicates the full-scale level of the A/D converted signal as 0dB. For example, when the reference signal level is +4dB, the headroom is 20dB and the maximum signal level is +24dB. The level meter reads "-20dB" for an input signal of +4dB and the "0dB" for an input signal of +24dB.

3.1.8.6 Level Adjustment

While observing the level meter, adjust the signal level as follows. Be sure to set the PEAK indication mode selector to AUTO when adjusting the level.

STEP 1 Set the headroom with the REF MARKER selector. The LED of the REF MARKERs corresponding to the selected headroom will illuminate. For example, to set the headroom to 16dB, set the RED MARKER selector to "16". The REF MARKER LED of -16 dB will illuminate.

NOTE: The REF MARKER selector setting has no effect upon the gain, but only changes the REF MARKER indication.

STEP 2 Input an audio signal at the desired reference level to the unit, and adjust the REC LEVEL ADJUST controls so that the level meter indicators corresponding to the selected desired reference level (equal to the REF MARKER LED) illuminate.

STEP 3 Set the SCALE selector to FINE, and precisely adjust the REC LEVEL ADJUST controls.

The level meter calibration changes to display in 0.2-dB steps above and below the illuminated REF MARKER LED. Only one LED for each channel on the level meter illuminates. Adjust the REC LEVEL ADJUST controls so that the lowest LED on the level meter illuminates. It is recommended to overadjust so that two Llower LEDs illuminate and then back off the adjustment so that only the lowest LED is illuminated.

STEP 4 Set the SCALE selector to back to NORMAL.

3.2 PCM-1610 PCM Processor

The **PCM-1610** PCM Processor is used to encode the digital audio signals for use by the rotary head recorders. It features tranformer balanced analog audio inputs and outputs and is the predecessor to the **PCM-1630**.

3.2.1 PCM-1610 Front Panel

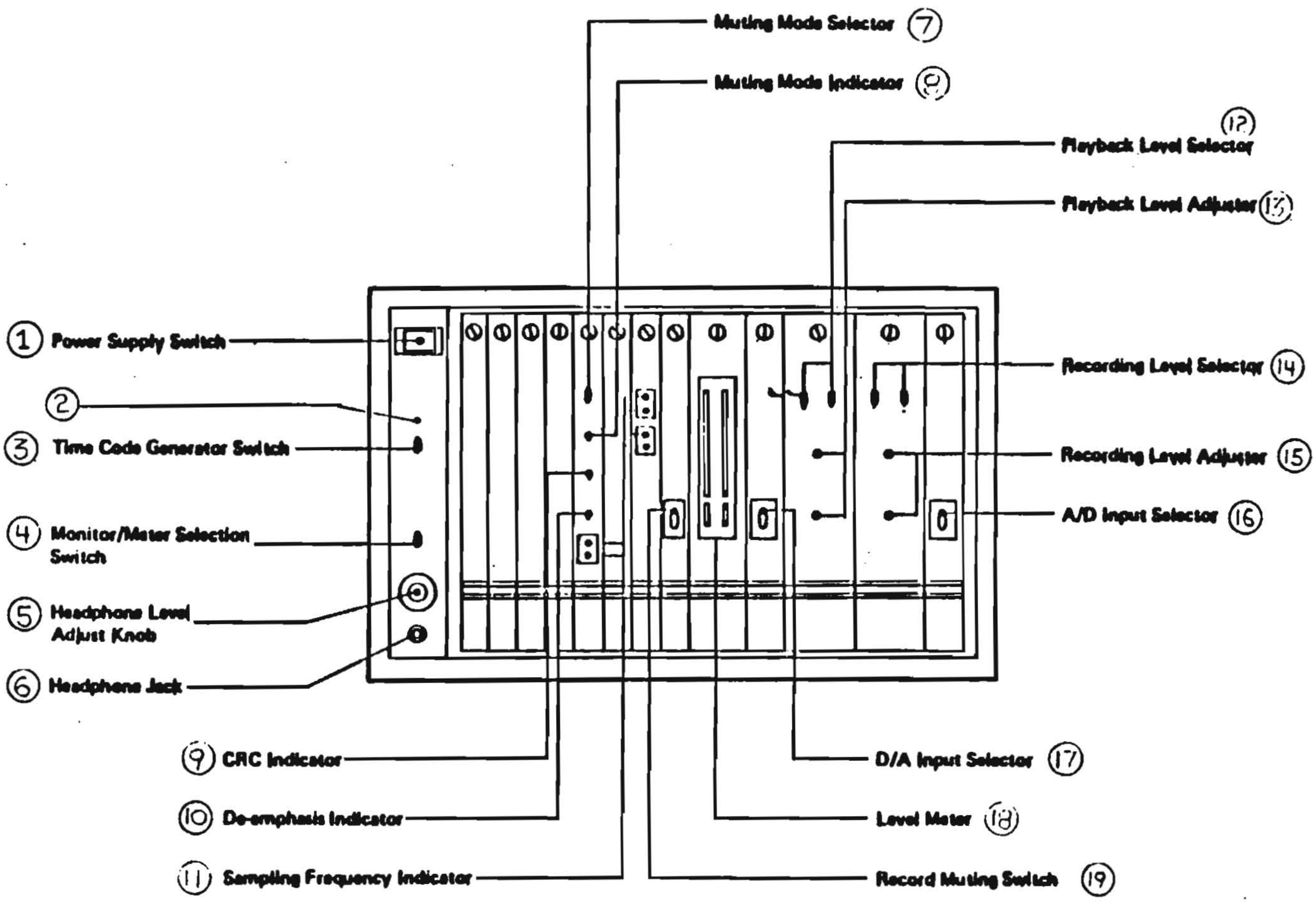


Figure 3-12 PCM-1610 Front Panel

1 Power Supply ON/OFF switch

Switch the line voltage source to the Power Supply ON and OFF.

2 Time Code Generator LED

This indicator has three modes of operation which are relative to the setting of the Time Code Generator switch indicating the mode of operation of the time code generator.

TC Generator switch setting	TC Generator LED condition
RESET	OFF
HOLD	FLASHING
RUN	ON

Table 3-9 Time Code Generator Modes of Operation

3 Time Code Generator switch

This switch selects the mode of operation of the Time Code (TC) Generator.

RESET This setting will set the value of the TC Generator to zero.

HOLD This setting will hold the value of the time code generator at the time that the switch is set.

RUN This setting will place the TC Generator in the RUN mode. This mode will commence at the last value registered in the generator and will not stop the generator until the RUN setting is changed.

4 Monitor/Meter Selection switch

This switch will select the signal output to the monitor system and meter circuitry. The selection is either the PB (pLAYER) or the REC (RECORDER) machine.

5 Headphone Level Adjust knob

This vernier control will adjust the audio signal volume level at the Headphone Jack.

6 Headphone Jack

This female connector supplies audio monitor signals to the headphones. The headphones must have an impedence of 8-ohms or more for the best results.

7 Muting Mode Selector switch

This switch allows selectivity between either a NORMAL or HOLD function. In the NORMAL setting the MUTE mode will react exactly to the error correction/detection circuitry. For example, when the MUTE condition occurs, the MUTE LED will illuminate, and when the MUTE condition is released the LED will extinguish. In the HOLD setting for any (mute condition occurance, the MUTE LED will illuminate and remain illuminated until the Muting Mode selector is returned to the NORMAL position.

8 Muting Mode Indicator LED

This indicator will illuminate when a MUTE condition occurs. It can be set for HOLD mode or NORMAL operation by way of the Muting Mode Selector (see above).

9 CRC Indicator LED

This indicator will illuminate whenever a Cross Redundancy Check (CRC) code error occurs and extinguish when the CRC error ceases.

10 De-emphasis Indicator LED

This indicator will illuminate to indicate that the De-emphasis circuit is active which means that the EMPHASIS bit in the digital audio data is on (pre-emphasis).

11 Sampling Frequency Indicator LED

These indicators illuminate to indicate which Sampling Frequency is being utilized (44.1kHz or 44.056kHz) on the tape.

12 Playback Level Selector switches

These switches (one for each channel) each have two positions (PRESET/VARIABLE).

PRESET The Playback signal level is determined by the internal settings of the PB AUDIO board switches.

VARIABLE The two adjustment screws (one for each channel) located on the front of the PB AUDIO board are selected as Playback Level adjustments. These adjustments are one turn vernier controls that yield a +/-6dB range.

13 Playback Level Adjustment screws

These variable resistors adjust the Playback Level for a maximum adjustment of 12dB (+/- 6 dB) when the Playback Level Selector switches are set for VARIABLE.

14 Record Level Selector switches

These switches (one for each channel) select either the PRESET position or the VARIABLE position.

PRESET The Record Level is determined by the internal settings of the REC AUDIO board.

VARIABLE The two adjustments (Record Level Adjustment screws) located on the front panel of the REC AUDIO board are enabled and are utilized for this adjustment. These allow for an adjustment range of approximately +/-6dB

15 Record Level Adjustment Screws

These one turn variable resistors can adjust the Record Level for a maximum adjustment deviation of 12dB (+/-6dB) from the preset value when the Record Level Selectors are set to the VARIABLE position.

16 A/D Input Selector switch

This switch selects the input type desired, either ANALOG or DIGITAL, to the A/D board.

ANALOG The analog audio signals from the XLR Cannon connectors are routed to the A/D convertors

DIGITAL The digital audio data signals input from the rear panel replace the digital audio data output from the A/D convertors and gets routed to the encoder.

17 D/A Input Selector

This switch selects the input to the D/A board.

INTERNAL Routes data from the A/D board to the D/A convertors.

EXTERNAL Digital audio data connected to the rear panel is routed to the D/A convertors.

18 Level Meter

This meter tracks both channel 1 and 2 with two 24-segment LED bars with a range of -42dB to +20dB. The two 5-segment meters below the main meters are calibrated such that they can be used as a fine adjust around the 0dB point of the main meters

19 Record Muting switch

This momentary switch allows the instantaneous muting of the input signal to the RECORDER (all zeroes in the digital audio data).

3.2.2 PCM-1610 Rear Panel

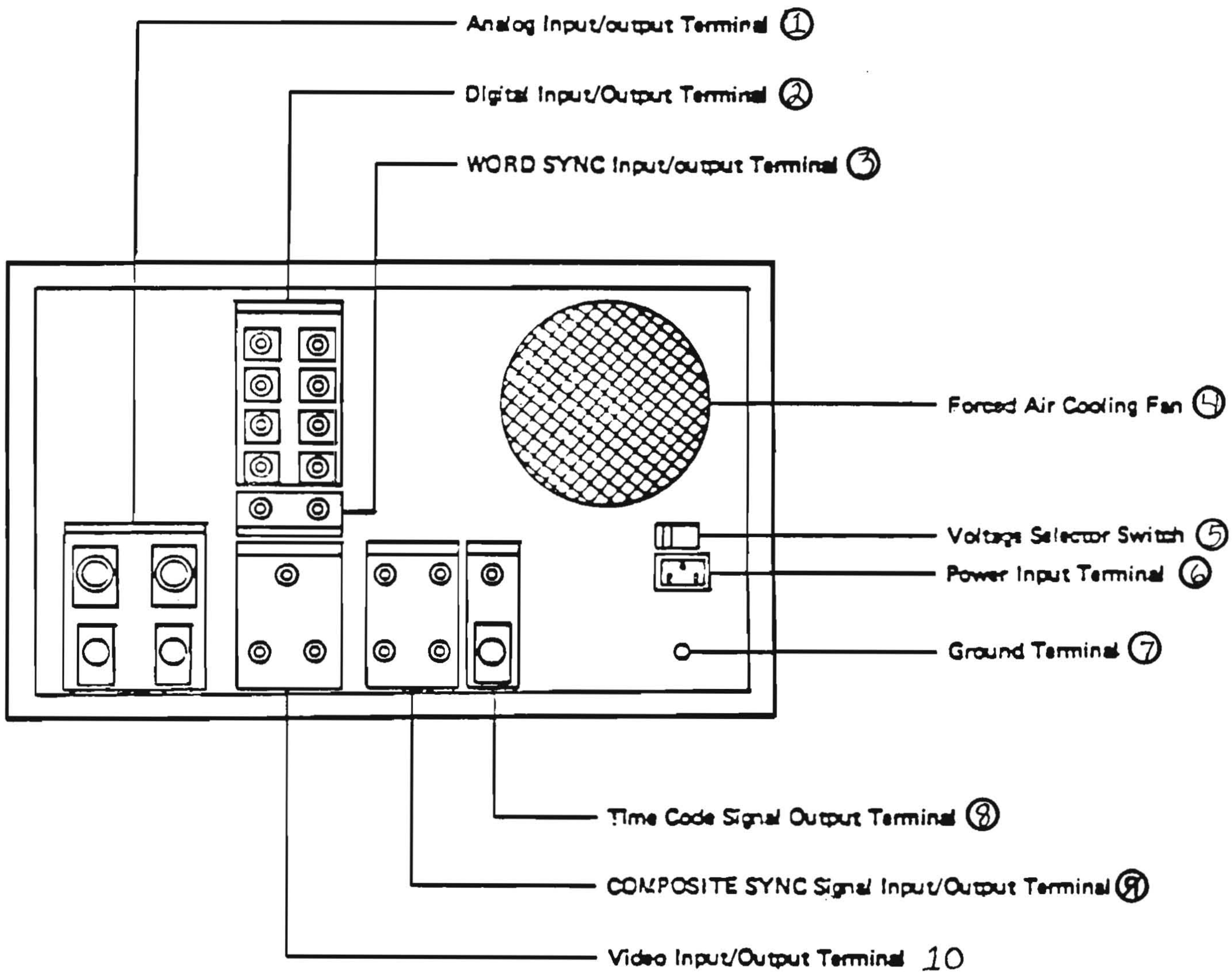


Figure 3-13 PCM-1610 Rear Panel

1. Analog Input/Output Terminals

These terminals provide input of analog audio signals into the PCM-1610 and analog output to the monitor system.

***NOTE:** These XLR type connectors are wired as shown below:

PIN #	ASSIGNMENT
1	SHIELD
2	COLD
3	HOT

Table 3-10 PCM-1610 XLR Connector Wiring

2 Digital Input/Output Terminals

These terminals provide access to the A/D output, D/A input, ENCODER input, and DECODER output.

3 WORD SYNC Input/Output Terminals

These BNC connectors provide for WORD SYNC input and output for synchronization between machines.

4 Forced Air Cooling Fan

This fan provides the necessary cooling for the power supply and all internal electronics of the **PCM-1610**. Be sure to leave adequate ventilation space to avoid overheating of the unit.

5 Voltage Selector switch

This switch alloes for selectability of the input line voltage between two ranges 100v to 120v and 220v to 240v.

WARNING: The Voltage Selector switch must be properly set to the correct line voltage input setting **BEFORE** connecting the **PCM-1610** to line voltage. An improper setting of this switch upon turning on the power can result in catastrophic damage to the unit.

6 Power Input Terminal

This connector is where the standard equipment line cord is mated to supply line voltage to the unit.

7 Ground Terminal

This is a chassis ground connection which can be used for star grounding of the unit in the existing system.

8 Time Code Output Terminal

This terminal provides unbalanced time code signal at the BNC connector and balanced time code signal at the XLR type connector.

9 COMPOSITE SYNC Input/Output Terminal

This terminal provides two BNC unbalanced inputs and two BNC unbalanced outputs for composite sync signals. The 75-ohm termination switch is also located in this section for using bridging, looping, or daisy-chained configurations. When this is done, this switch should be ON (otherwise it should be OFF).

10 Video Input/Output Terminal

This terminal provides a single BNC unbalanced video (composite digital) input and two video (composite digital) outputs.

3.3 DAE-1100/1100A

All the editing controls for the **DAE-1100** series Digital Audio Editors are found on the keyboard. The keyboard is separated into five specific sections, the PLAYER-A controls, PLAYER-B controls, RECORDER controls, SEARCH functions, and the GAIN OFFSET control. The PLAYER and RECORDER sections are basically the same, each controlling a specific machine.

3.3 DAE-1100/1100A Keyboard

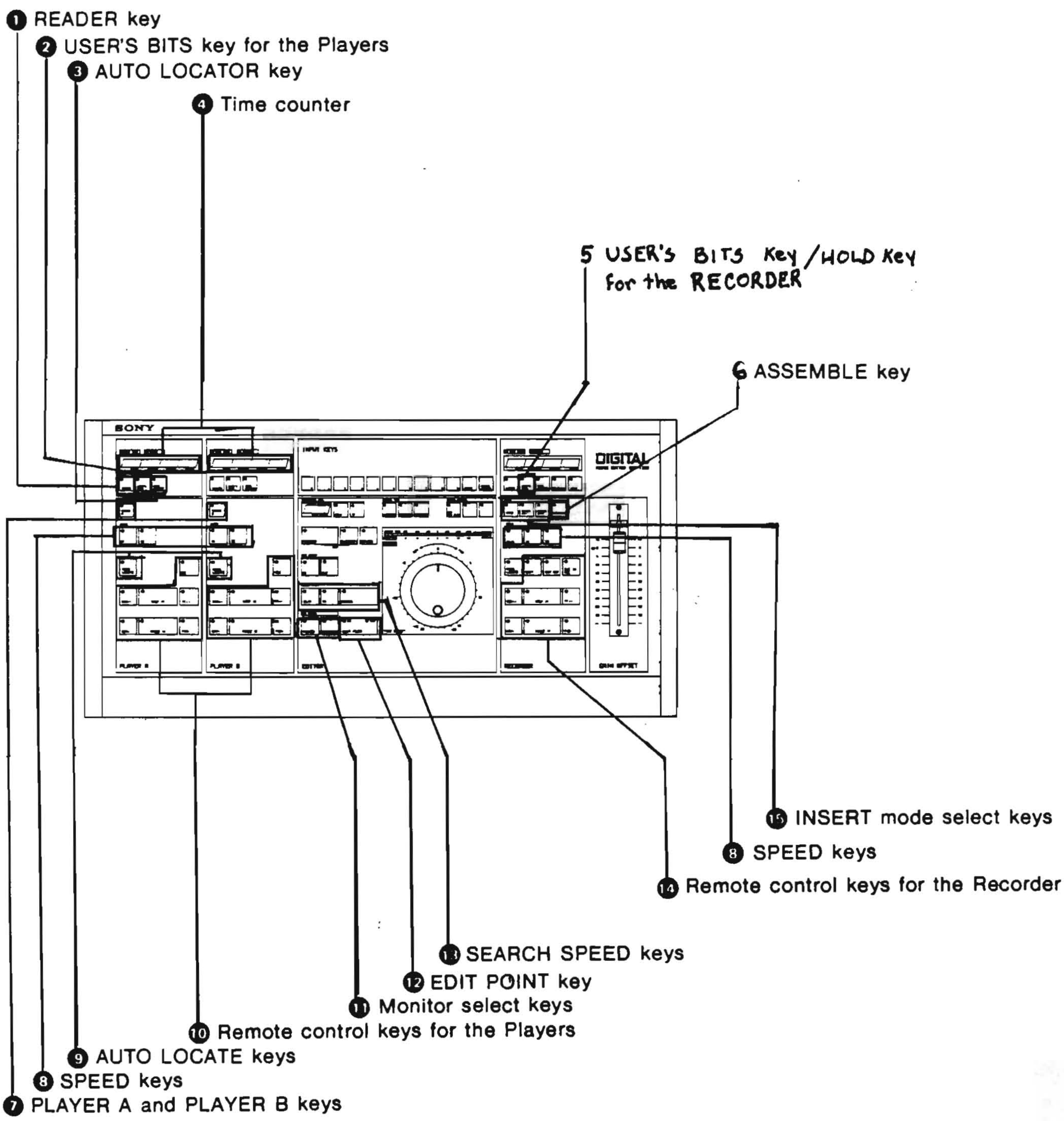


Figure 3-14 DAE-1100 Series Keyboard/Controller

1 READER key

When this key is pressed and the indicator LED on the key illuminates, the time code read by the built-in time code reader for PLAYER-A is displayed on the time counter display just above it. When the unit is turned on, this key is always set to this condition.

2 USER BIT key for the Players

Press to recall the numerical sequence recorded with the time code on the PLAYER-A tape by means of the User Bits function.

3 AUTO LOCATOR key

Press this key and then enter the time code value with the INPUT KEYS (see #20) to memorize the locate point to be accessed with the AUTO LOCATE key (see #9). A flashing lower segment on the display indicates which character is being entered. This value defaults to zero (0) on power-up.

4 TIME COUNTER

The SMPTE time code, users bits, or autolocate value for PLAYER-A is displayed here.

5 USER BIT key and HOLD key for the Recorder

To store a 8-digit sequence in memory (for example, the date), press the USER BITS key, then the HOLD key, and then the appropriate INPUT KEYS. The memorized sequence will be recorded on the tape within the longtitudinal time code signal during a RECORD, INSERT CH-2 RECORD or ASSEMBLE RECORD mode. Pressing the USER BITS key alone displays the recorded sequence in the time counter display. The HOLD key can be used to momentarily stop the time code generator. To restart the time code generator, press HOLD again.

6 ASSEMBLE key

This key places the Recorder in the ASSEMBLE edit mode. In ASSEMBLE mode, all tracks are recorded including digital audio data (composite digital), time code, and control track.

7 PLAYER A and PLAYER B keys

In the editing operation, press one of these keys, depending on which Player is being used for the edit IN point.

8 SPEED keys

Select the tape speed during the forward or reverse mode. The X1/5 key will transport the tape at 1/5 normal speed, the X1 key at normal sped and X2 key at twice normal speed. (With some Recorders/Players the tape may be transported at speeds different from these settings.)

9 AUTO LOCATE keys

Press to automatically locate the time code value stored in the memory by the AUTO LOCATOR key (see #3). When this is pressed, the tape will fast wind so that its time code value becomes the same as the autolocate value.

10 Remote control keys for the Players

These keys control the transport functions of each PLAYER.

11 Monitor select keys

When the PLAYER Key is pressed, the sound of the PLAYER tape can be monitored and the player will be active for selecting an edit point. The PLAYER which is active is indicated by the PLAYER-A and PLAYER-B keys (illuminated). When the RECORDER key is pressed, the sound of the RECORDER tape can be monitored. The edit point selection will be enabled upon pressing EDIT POINT IN/OUT for the machine that is being monitored.

12 EDIT POINT key

When this key is pressed, the edit point for the active VTR will be stored in the memory. The IN lamp lights when the edit point to be located is on the PLAYER tape. The OUT lamp lights when the edit point is on the RECORDER tape. Three seconds after this key is pressed, the unit will go into the search mode enabling 3 seconds before EDIT POINT and 3 seconds after to be stored in SEARCH RAM. SEARCH RAM data can be reproduced by the SEARCH dial or SEARCH SPEED keys.

13 SEARCH SPEED keys

When searching for the edit point within the memorized +/-3 seconds range, the X1/2 key makes the reprodution at 1/2 normal speed and X1 key at normal speed. The MANUAL key activates the editor's manual search mode. In this mode search for the exact edit point using the SEARCH dial (see #28).

14 Remote control keys for the Recorder

These keys control the tranport and front panel editing mode functions of the RECORDER.

15 Insert mode select keys

These keys function in the same way as the INSERT mode select switches of the RECORDER and select the INSERT mode. In the INSERT mode, the CTL track is reproduced, and composite digital signals are recorded in sync with the CTL signal from tape, therefore, a continuous CTL stripe is required when using INSERT mode.

DAE-1100/1100A Keyboard Controller

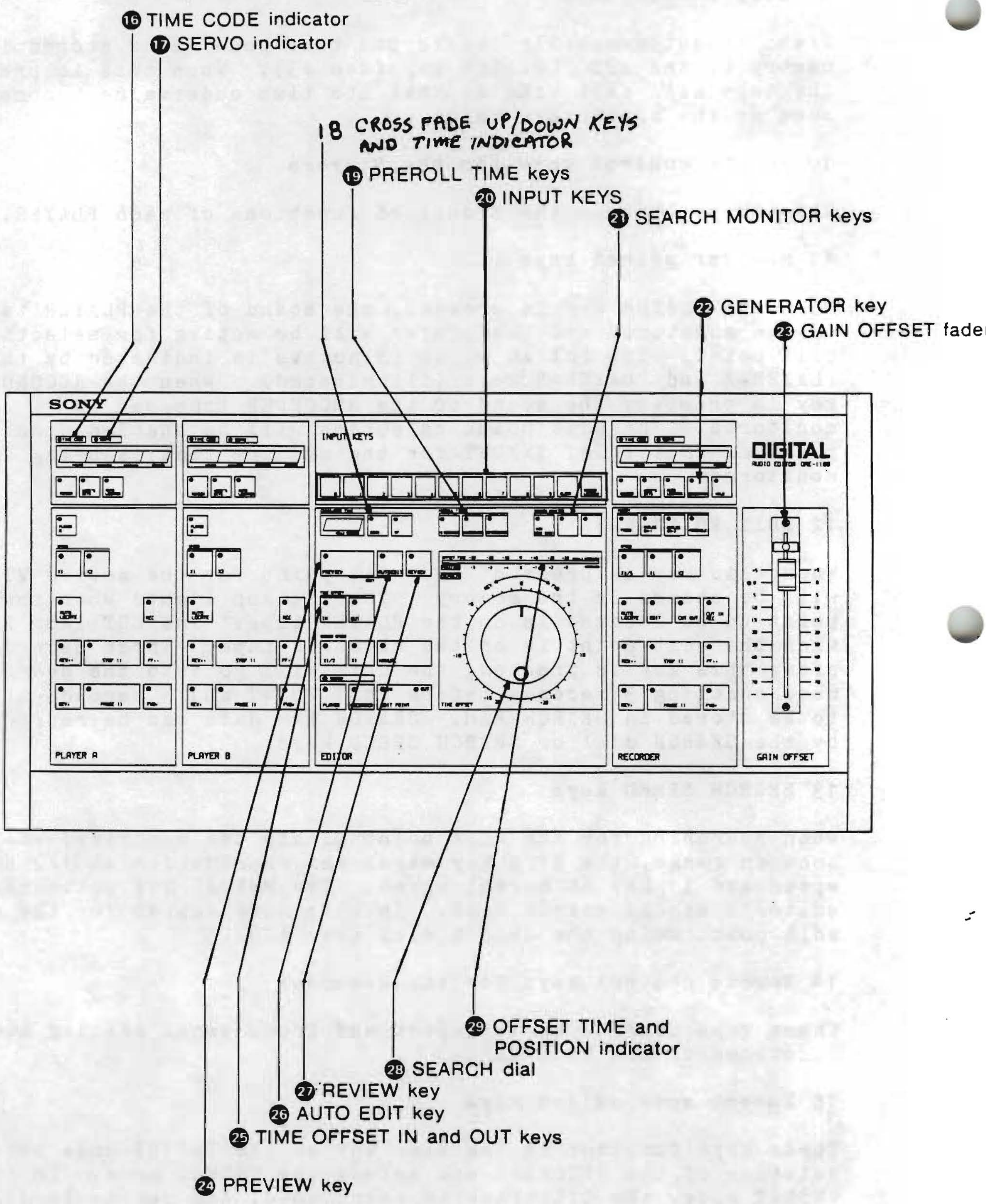


Figure 3-15 DAE-1100 Series Keyboard

16 TIME CODE indicator

This illuminates to indicate that time code is being read by the internal time code reader. It will not illuminate if the wrong type of time code is used, if the signal level is too low, or if the time code is not synchronized with the video signal.

17 SERVO indicator

This illuminates when the VTR drum servo is locked.

18 CROSS-FADE TIME keys and indicator

Select one of the 10 available cross-fade times by pressing the DOWN (to decrease) or the UP key (to increase).

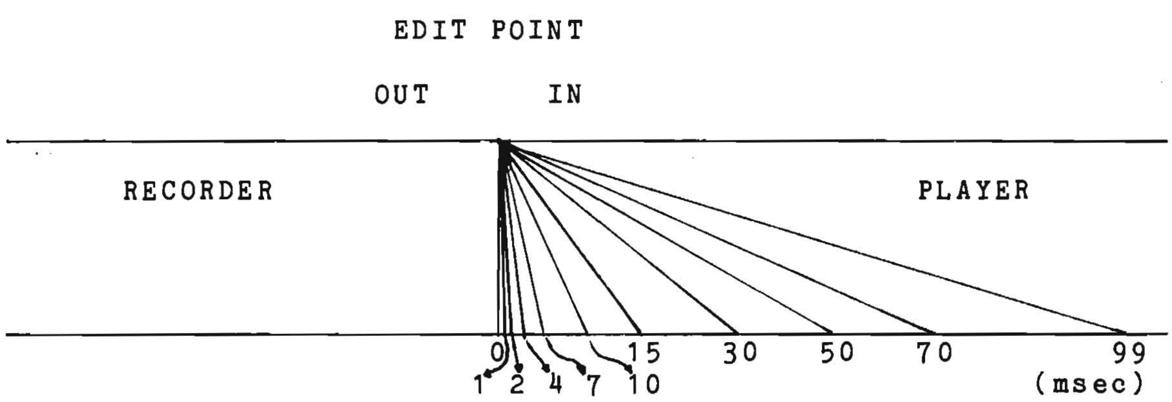


Figure 3-16 Cross-fade Times

19 PREROLL TIME keys

Select the pre-roll point from which the PREVIEW, AUTO-EDIT, or REVIEW will start. Pressing the 5 SECONDS key, for example, will start PREVIEW, AUTO-EDIT, or REVIEW 5 seconds before the edit point.

20 INPUT keys

Use to enter SMPTE time code value used for the time code generator start time, autolocate position, and to enter numerical USER BITS information.

21 SEARCH MONITOR keys

When searching for the edit point using the SEARCH dial, monitoring the mono sum of both channels, CH1, or CH2 (individually) can be achieved by pressing the appropriate key. The key must be pressed before the unit enters the SEARCH mode.

22 GENERATOR key

Press to display the SMPTE time code generated by the built-in time code generator (displayed in the RECORDER section display).

23 GAIN OFFSET CONTROL

This controls the output level of the PLAYER as an attenuator in the digital domain. A stop is placed so that the uppermost position of the fader is 0dB or +5dB (gain). When this is set to 0dB, the indicator LED illuminates.

24 PREVIEW key

Press to check the edit point selection without recording (PREVIEW). This operation will initiate electronic editing when used with the AUTO EDIT key.

25 TIME OFFSET IN and OUT keys

To adjust the edit-in or edit-out point, keep the IN or OUT key pressed and turn the SEARCH dial. Shift the edit point anywhere within a range of +/-1 minutes, each full turn of the SEARCH dial corresponds to 1 time code frame (see silkscreened segments for sub-frame positioning).

26 AUTO EDIT key

Press this key together with the PREVIEW key to start automatic editing. When pressed alone, this key does nothing.

27 REVIEW key

Press to check the completed edit. When pressed, the RECORDER rewinds to the pre-roll point and plays through the recorded edit (used for confidence listening).

28 SEARCH dial

In the manual SEARCH mode, turn this dial and monitor the sound to locate the exact edit point (similar to rocking the reels of an analog tape machine). Also used to set the offset time.

29 OFFSET TIME and POSITION indicator

The lower scale (POSITION) is for edit point location giving a visual indication of the edit point during a SEARCH operation, and the upper scale (OFFSET TIME) indicates the offset time used when offsetting the IN or OUT points using the SEARCH dial.

3.9 DAE-1100A REAR PANEL

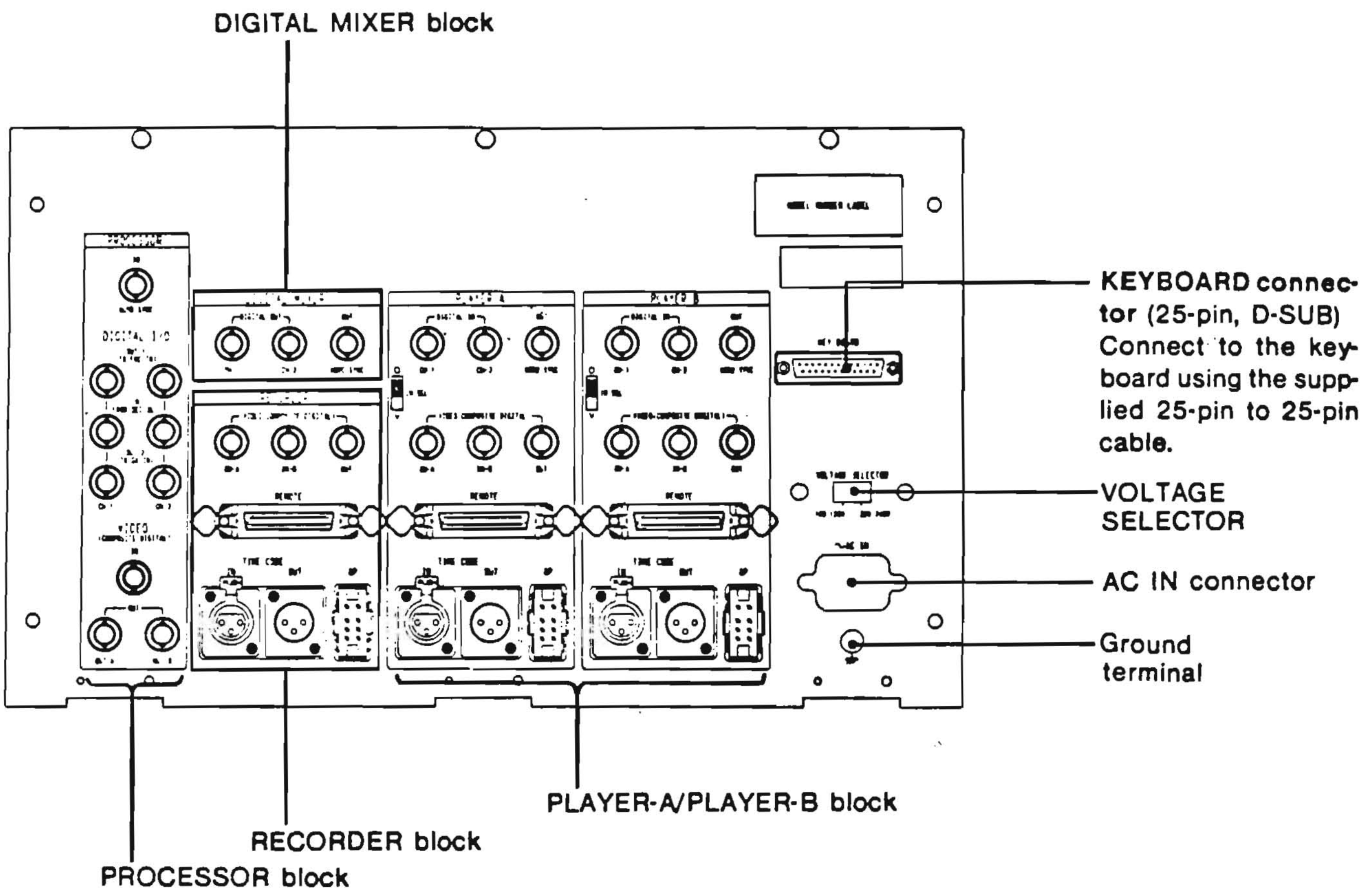


Figure 3-17 DAE-1100A Processor Rear Panel

3.9.1 PROCESSOR BLOCK

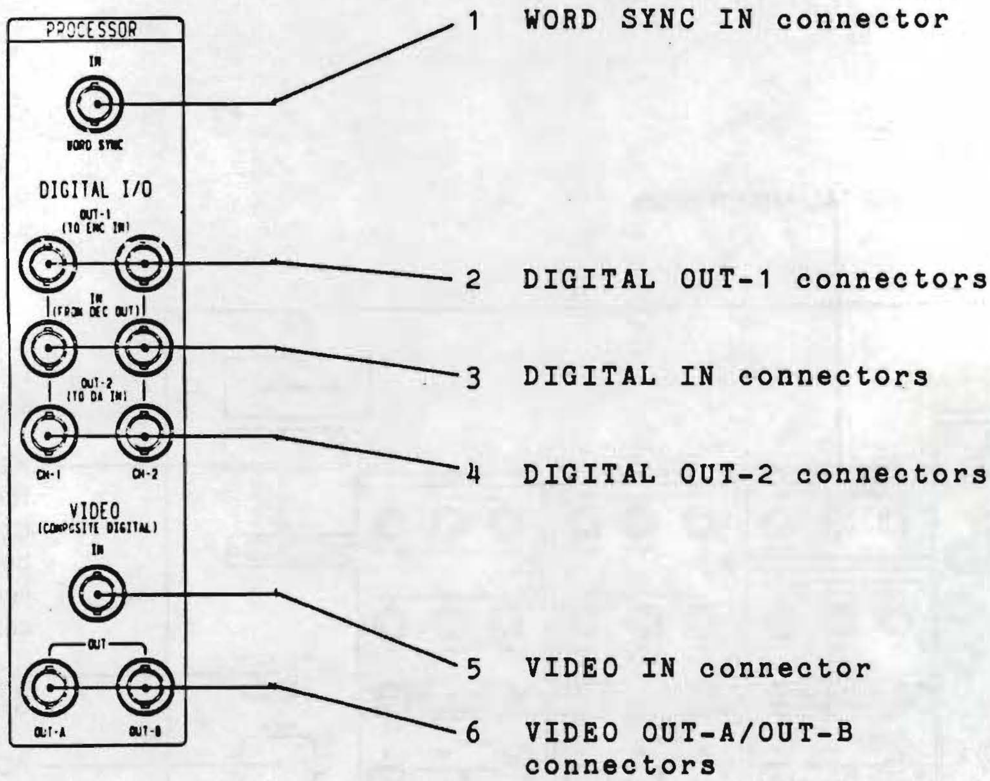


Figure 3-18 DAE-1100 Rear Panel Processor Block

1 WORD SYNC IN connector (BNC type)

Accepts the word sync signal from the PCM Processor. The word sync signal input here is buffered and output from the WORD SYNC OUT connectors of DIGITAL MIXER, PLAYER-A, and PLAYER-B blocks.

2 DIGITAL OUT-1 connectors (BNC type)

Connects to the ENC IN connector of the PCM processor. These connectors supply the digital output signals from the editor to the PCM processor.

3 DIGITAL IN connectors (BNC type)

This is an input to the editor which accepts the digital output signals from the DEC OUT connectors of the PCM Processor.

4 DIGITAL OUT-2 connectors (BNC type)

Connect this output from the editor to the DA IN connectors of the PCM processor. These connectors supply the digital output signals from the editor to be used for monitoring.

5 VIDEO IN connectors (BNC type)

Connect this input of the editor to the composite digital (video) output of the PCM processor.

6 VIDEO OUT-A/OUT-B connectors (BNC type)

Connect this output from the editor to the composite digital (video) input A or B of the PCM processor to supply composite digital output signals. The signal is selected from the composite digital signal supplied to the VIDEO IN connector of the RECORDER, PLAYER-A, or PLAYER-B block depending on the **DAE-1100A** keyboard setting and mode of operation.

3.9.2 DIGITAL MIXER Block

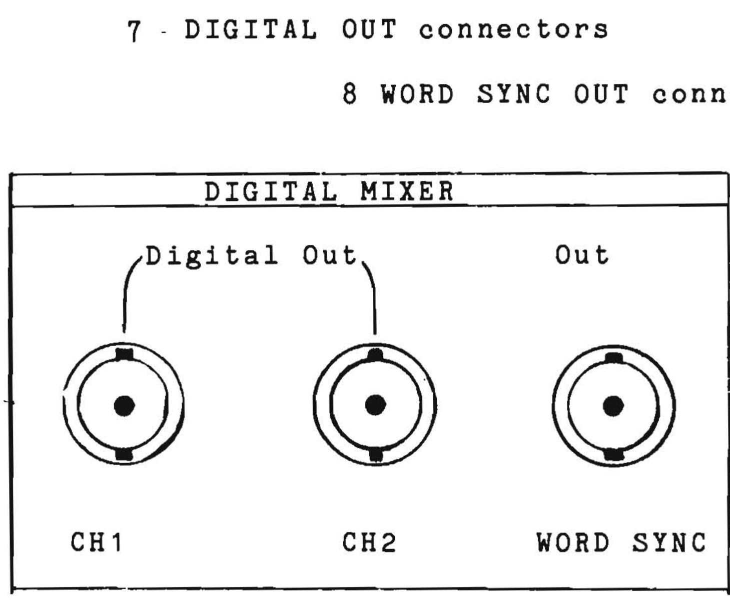


Figure 3-19 DAE-1100 Rear Panel DIGITAL MIXER Block

7 DIGITAL OUT connectors (BNC type)

The digital signals supplied from the PCM processor to the DIGITAL IN connectors (see #3) are buffered and output from these connectors to the digital mixer.

8 WORD SYNC OUT connector (BNC type)

The buffered word sync signal supplied from the PCM processor to the WORD SYNC IN connector (see #1) is buffered and output from this connector to the digital mixer.

3.9.3 RECORDER BLOCK

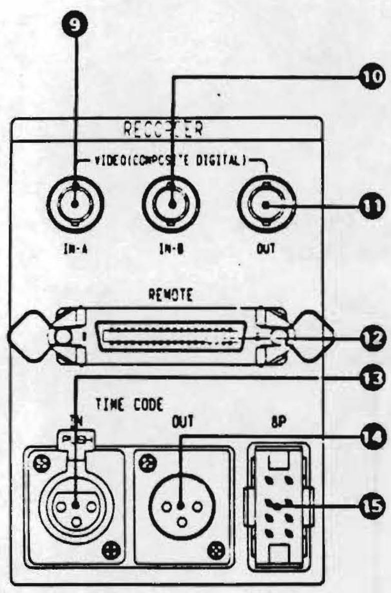
9 VIDEO IN-A connector

10 VIDEO IN-B connector

RECORDER BLOCK

VIDEO (COMPOSITE DIGITAL)

11 VIDEO OUT connector



12 REMOTE connector

13 TIME CODE IN connector

14 TIME CODE OUT connector

15 8P connector

Figure 3-20 DAE-1100 Rear Panel RECORDER Block

9 VIDEO IN-A connector (BNC type)

Accepts the composite digital (video) signal from the VTR. This input signal is output from the VIDEO OUT-A connector (see #6) of the PROCESSOR block.

10 VIDEO IN-B connector (BNC type)

This is the second composite digital (video) input to the editor used when editing with the RAR mode utilizing the **PCM-1630** and the **DMR-4000**. It connects to the SUB (B) COMPOSITE DIGITAL OUT-1 or OUT-2 connector of the **DMR-4000**. The input signal is output from the VIDEO OUT-B connector (see #6) of the PROCESSOR block.

11 VIDEO OUT connector (BNC type)

The composite digital signal supplied to the VIDEO IN connector (see #5) of the PROCESSOR block is output directly from this connector. This signal must be terminated by way of a 75-ohm termination switch at the input of the VTR.

12 REMOTE connector (36-pin)

Input/output connector for the RECORDER remote control. Connect directly to the **BVU-800DA/DB** or **DMR-4000**, connect to the **IF-5850DA** when using the **DMR-2000**.

13 TIME CODE IN connector (Cannon XLR-3-31)

Input connector for the built-in SMPTE time code reader.

14 TIME CODE OUT connector (Cannon XLR-3-32)

Output connector from the built-in SMPTE time code generator.

15 8P connector (8-pin)

Input/output connector pin for signals equivalent to those of the VIDEO IN-A, VIDEO OUT, and TIME CODE IN/OUT connectors of the RECORDER block. This can be used in place of the BNC connectors by using a VTR equipped with an 8-pin connector using the 8-pin multi-cable.

3.9.4 PLAYER A/PLAYER B Block

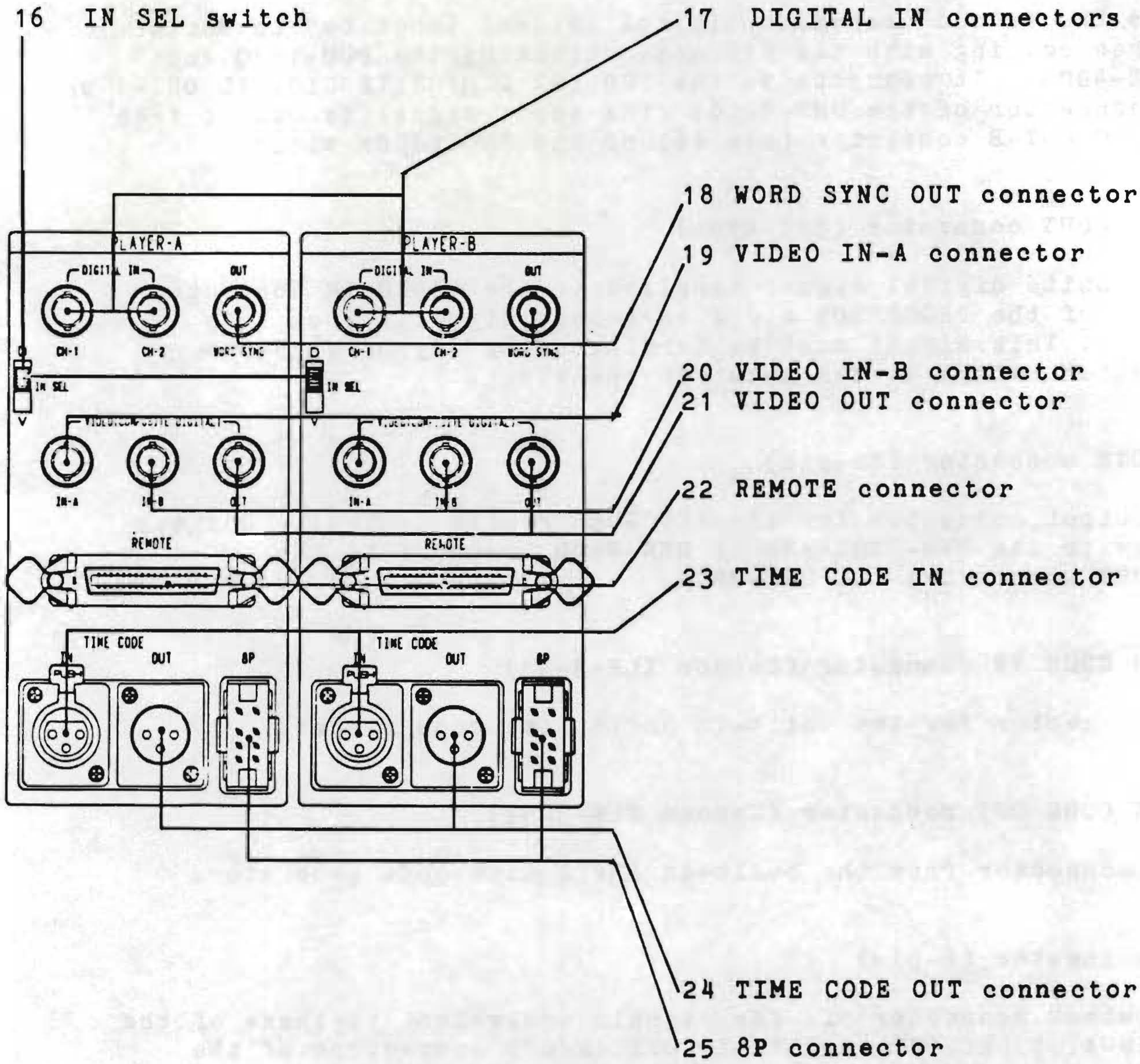


Figure 3-21 DAE-1100 Rear Panel PLAYER Blocks

16 IN SEL (input select) switch

Selects the input signal source as follows:

D: The digital input signal.
V: The composite digital input signal.

17 DIGITAL IN connectors (BNC type)

Inputs used when utilizing the **PCM-3102/3202** as PLAYER A or B the DIGITAL IN connectors of the corresponding block (PLAYER-A or B) causing the editor to accept the digital output signal from the **PCM-3102/3202**. Also used when utilising the digital mixer, connecting the output of the mixer to these connectors of the corresponding block.

18 WORD SYNC OUT connector (BNC type)

The buffered word sync signal supplied to the WORD SYNC IN connector 1 from the PCM processor is output from this connector. When using the **PCM-3102/3202** as the player, connect to the **PCM-3102/3202** to synchronize it with the **PCM-1610/1630** using the same sampling frequency of the word sync signal.

19 VIDEO IN-A connector (BNC type)

The composite digital (video) signal supplied from the PLAYER A/B is input to this connector. The signal input here is output from the VIDEO OUT-A connector 6 of the PROCESSOR block.

20 VIDEO IN-B connector (BNC type)

When editing the RAR mode using the **PCM-1630** and the **DMR-4000**, connect to the SUB (B) COMPOSITE DIGITAL OUT connector of the **DMR-4000** for playback. The signal input here is output from the VIDEO OUT-B connector 6 of the PROCESSOR block.

21 VIDEO OUT connector (BNC type)

Output connector for the composite digital (video) signal used to synchronize PLAYER A/B with the PCM processor. Connect to the composite digital input connector of the PLAYER A/B VTR.

22 REMOTE connector (36-pin)

Input/output connector for the remote control signals of the PLAYER A/B. Connect directly to the **BVU-800DA/DB** or **DMR-4000**, to the **IF5850DA** when using the **DMR-2000**, or to the **IF-3000** interface box when using the **PCM-3102/3202** Series DASH machines.

23 TIME CODE IN connectors (Cannon XLR-3-31)

Input connector for the built-in SMPTE time code reader.

24 TIME CODE OUT connectors (Cannon XLR-3-32)

Output connector for the built-in SMPTE time code generator. Utilized when using the **PCM-3102/3202** as a player for phase synchronization with **PCM-1610/1630** via the time code frame.

25 8P connector (8-pin)

Input/output connector for signals equivalent to those of the VIDEO IN-A, VIDEO OUT, and the TIME CODE IN connectors of the PLAYER A/B blocks. This can be used as the only connection to a VTR equipped with an 8-pin connector using an 8-pin multi-cable.

SECTION 5

PCM-1610 CIRCUIT DESCRIPTIONS

PCM-1610 CIRCUIT DESCRIPTION

5.1 GENERAL BLOCK DIAGRAM THEORY

The following is a descriptive analysis of the overall signal flow of the **PCM-1610**. Refer to Fig. 5-1.

The basic block consists of 4 sections: 1. Record Section, 2. Clock Generator Section, 3. Meter/Monitor Section, and 4. Playback Section. Each will be discussed individually.

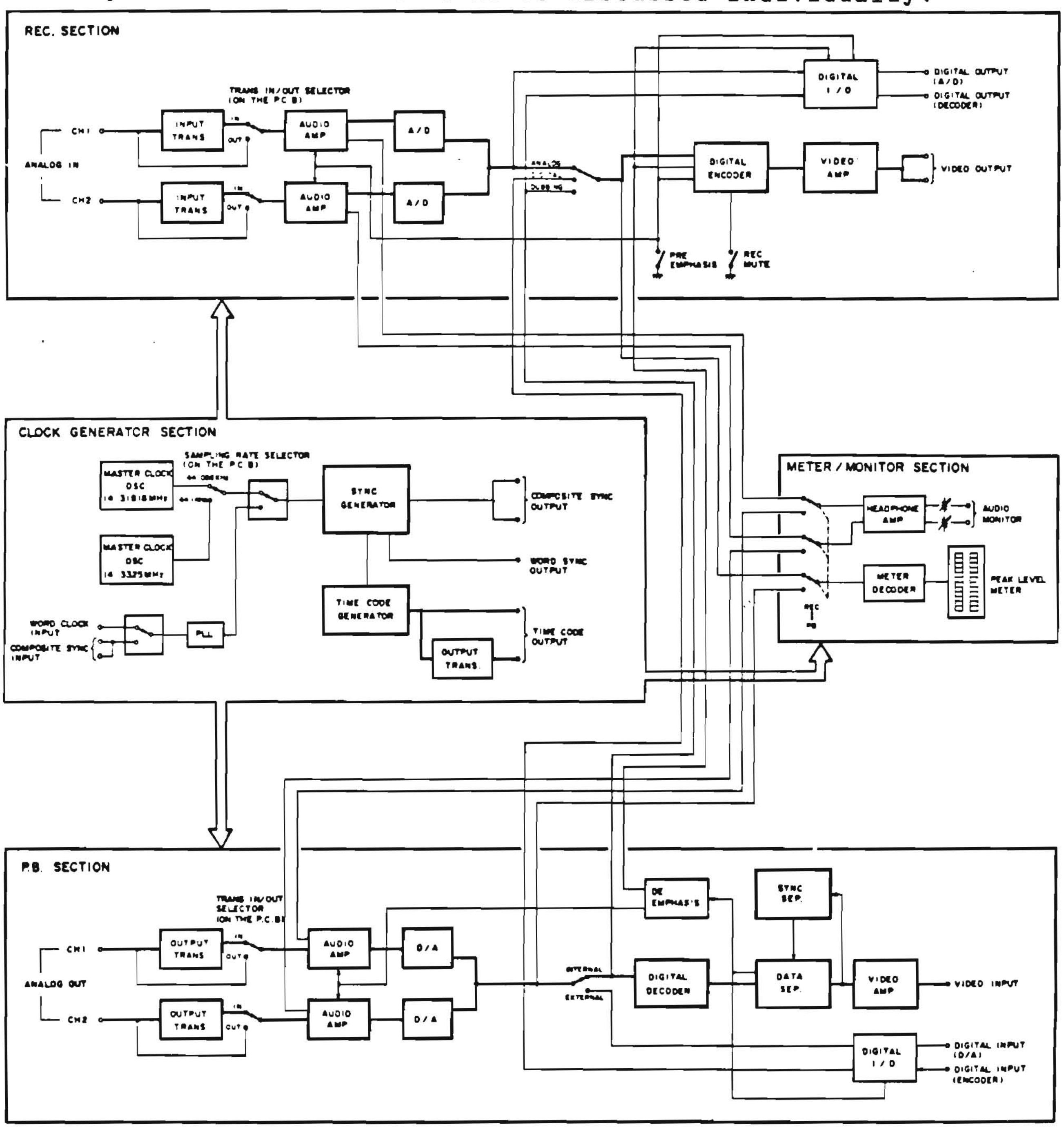


Figure 5-1 PCM-1610 Overall Block Diagram

5.1.1 Record Section

The RECORD section consists of the analog input stages which route the analog inputs to the analog-to-digital converters. The digital outputs of the A/D converters is routed to the encoder for adding error correction and encoding to composite digital (video) format. Also included in this section is the digital I/O. The major blocks are described below.

Rec Amp: Referring to Figure 5-1, analog signals are input via the record board. The signals can be transformer or direct coupled and is then sent through a low pass filter (L.P.F.) to limit the maximum signal frequency to 20kHz. This is used to attenuate and eliminate alias frequency components (frequencies greater than the Nyquist frequency) entering the analog-to-digital converter (A/D) stage. From there, the signals are impedence (Z) converted and level adjusted in the filter amp. The signals are then sent to the A/D board.

A/D: The signals from the REC board enter the A/D where the signals are first sampled by the sample-and hold (S/H). The S/H stores the analog information for a brief time to to allow the A/D converter to make a conversion without the input voltage changing during the coversion period. The parallel A/D data signals are then sent to the parallel-to-serial converter and output from the board in a serial format.

Encoder: The data from the A/D is routed to various boards, one of which is the encoder board. The encoding of the data consists of the following steps:

1. Word interleaving and adding of error correction and detection bits
2. Time-division/multiplexing of the 2 channels
3. Time-compression of the data stream
4. Adding the skew bits for identification of the sampling frequency (FsID) and emphasis (EMP) information.

Video Out: Encoded data from the encoder board is then mixed with video sync signals from the video out board. The video board, in addition to generating the video signal, also generates the sampling clocks which can be locked internally by crystal or locked externally by word clock or composite sync input. The internal or external master clock is used for producing all the reference clock signals for the other boards.

Data I/O: The data routed from the A/D is also routed to the digital I/O. The I/O contains 2 decoder outputs and 2 A/D outputs. The digital I/O is used to interface the PCM processor to other compatible devices.

5.1.2 Meter/Monitor Section

The monitor/meter section contains the meter decoder, the headphone amplifier, and the monitor switching circuitry.

Meter: 2 sets of 16-bit data signals are fed to the meter board circuitry. One set is from the A/D, the other is from the signal input to the D/A. The meter system can monitor either the Record or Playback signals.

Monitor: Since the switch for the meter and headphone monitor are ganged, monitoring and metering will be the same.

5.1.3 Clock Generator Section

The clock generator section contains the system timing oscillators as well as the sync and time code generators.

Video: The master clock generates timing references for the **PCM-1610**. Two oscillators select the sampling rates of 44.056 or 44.1kHZ. Using a PLL circuit, the clock generator can be externally locked by composite sync or word sync. In this case, the **PCM-1610** can be operated in a master/salve application

In addition, the generator section produces NTSC compatible sync signals such that the final psuedo video signals are compatible with VTR standards.

Time Code: Generator The Time Code Generator generates time code in D.F. or N.D.F. and is derived from the clock generator section. Hour and minute digits can be pre-set. The main purpose for this is to allow time code to be recorded on the analog tracks at the same time digital audio data is recorded in the ASSEMBLE mode. The time code and also be recorded at a different time (independently) using INSERT RECORD.

5.1.4 Playback Section

The playback section includes the decoder for separating the data from the composite digital (video) siganl, de-multiplexing, separation of error codes from the digital audio data, digital-to-analog conversion and the analog output sections. Eack block is described in the following paragraphs.

Video Out: Upon playback from a VTR, video information is input into the video board where sampling frequency and mode of sync is determined. The muting circuit in the video board supplies a muting signal to the decoder to prevent distortions associated with interruptions in the sync source.

Sync Sep: The Sync Separator board receives digital audio data signals super-imposed on the video signals via the back panel connectors. Digital audio and sync data are separated and the digital audio data is sent to the Data Separator board. The sync data is used to decode the encoded data.

Data Sep: Data from the SYNC SEP board is input into the Data Sep board. The data board discriminates the emphasis signal from the data, checks the data for correctability and sends the cleared data to the decoder. It also supplies muting signals to the decoder output when the data state is continuously N.G. The muting window as well as the muting time can be varied. Also, incoming data can be delayed to optimize the performance of the processor to match the VTR.

Dec A: The CRC of the data from the Data separator is sent to the DEC A board. Syndrome error signals relating to the decoded data are then determined and sent to the DEC B as either a correction, average, or holding signal. The DEC A board also generates the clock signals necessary for data correction.

Dec B: Parallel data and error information from DEC A are then routed into DEC B which corrects or conceals the data, and sends the corrected data to the D/A board.

D/A: The corrected data is routed to the D/A whereby the digital pulse streams are transformed from digital information to analog waveform signals. Devices within the board minimize distortion and create the aperture time needed for the D/A converter to convert the data to analog signals. Data from the D/A is sent to the PB board. The playback signals are routed through passive de-emphasis circuits which can be switched out manually or enabled automatically upon playback of emphasized material. In addition, the PB board houses the headphone amplifier for monitoring. The outputs are balanced or un-balanced and the level can be adjusted +/-6dB.

Digital I/O: In addition, the **PCM-1610** contains a digital I/O so that digital audio data can be transferred to other devices in the digital domain. The digital I/O consists of two blocks, the digital input and output blocks. The digital input block extracts external data, converts it into a form compatible to the internal data format, and sends the data to the encoder or D/A circuits. The digital output block converts data from the A/D out or decoder out, into a standardized I/O format to send to other digital devices.

5.2 ANALOG SECTION

Refer to Figure 5-2. Analog signals are input to the REC Audio board where level adjustments and pre-emphasis operations are performed. After passing through a low pass filter to remove signals above 20kHz, the signal enters the A/D stage where the analog signals are sampled and converted to digital audio data which is sent out as a serial bit stream. Monitoring of record or playback signals is accomplished by the REC/PB switch select located on the front panel. Digital information from the PCM processor is input externally from the I/O and routed to the D/A where the digital audio data is converted to analog signals. These analog signals are then processed by the Playback board where level and de-emphasis operations are performed, and routed to the final differential stage where it is output as an analog signal.

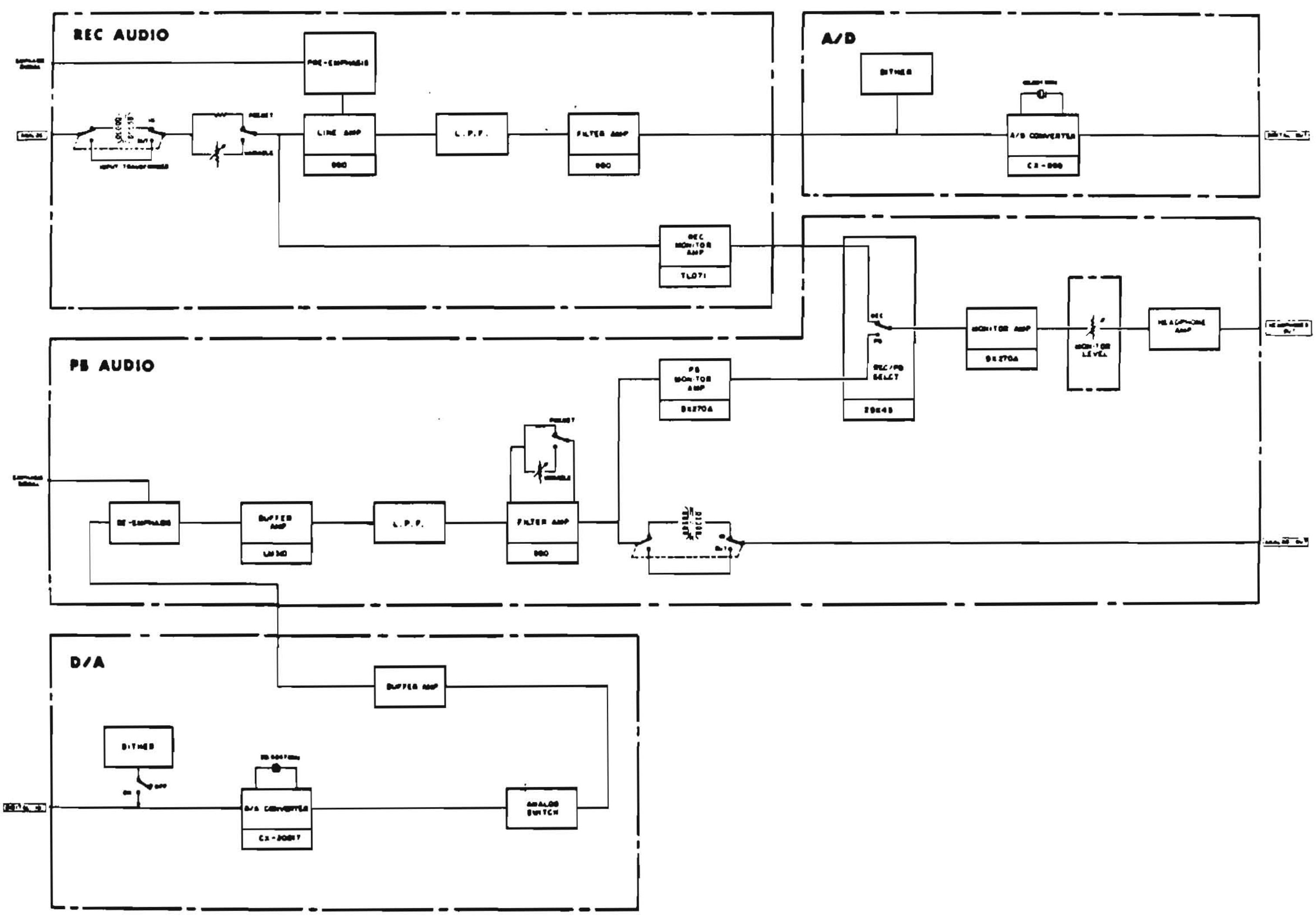


Figure 5-2 Analog Section Block Diagram

5.2.1 Record Audio Board

5.2.1.1 Outline and General Description

Audio signals at the analog input connectors are processed by the REC Audio Board. The board performs the following functions:

1. Bandwidth limiting
2. Transformer input/output switching
3. Adjusting the input/output level +/-6dB
4. Pre-emphasis function

5.2.1.2 Block Diagram and Schematic Analysis

Refer to the block diagram (Figure 5-2). Input signals are selected on the REC board by either transformer or direct coupled. These are then routed through the pre-set/variable select switch whereby the input level adjustment is determined. The level is adjusted in the line amp, incorporating a negative feedback pre-emphasis circuit. From the line amp, the signals are routed through the L.P.F. to limit the bandwidth to 20kHz. Finally, the signals are impedance converted and level adjusted in filter amp and brought out to the A/D.

Refer to the schematic diagram (Figure 5-3). Since both channels are identical, channel 1 will be used as reference. With the transformer switched in the balanced mode the input impedance is approximately 80k-ohm and 10k-ohm in the unbalanced mode. VR5 (2k-ohm) is used to obtain equal input level between the high (hot) and low (cold) signal lines regardless of the transformer in/out switch.

$$AV = \frac{R5 + R6 + R7}{R4} = \frac{33k + 2.4k + 100}{15k} = \frac{35.5k}{15k} = 2.367$$

$$Av\ (dB) = 20 \log Av = 20 \log 2.367 = 20 \times (0.3741) = 7.48dB$$

Table 5-1 Input Stage Gain Formula

For pre-emphasis:

$$T_1 = \left[2\pi \left(R8 + \frac{R5 \times (R6 + R7)}{R5 + (R6 = R7)} \right) C6 \right]^{-1} = 3192Hz$$

$$T_2 = \left[2\pi \quad R8C6 \right]^{-1} = 10,610\ Hz$$

Table 5-2 Pre-Emphasis Frequency Formula

The relay is controlled by Q1 and Q2 with R87, C7 used to cope with large drop-outs.

After passing through the L.P.F. which is a 13 pole Tchebyshev type filter, the signal is then impedance matched and level adjusted by the filter amp OP202.

$$AV = \frac{R15\ (13k) + VR4\ (0-\ 5k)}{R4\ (3.3k)} = 3.939 \text{ to } 5.454$$

$$AV\ (dB) = 20 \text{ Log } Av = 20 \text{ Log } 3.939 = 11.91 \text{ dB}$$
$$20 \text{ Log } 5.454 = 14.73 \text{ dB}$$

Table 5-3 Post-LPF Gain Stage Formula

IC1 and IC51 are used as a monitor amplifier to send signals to the PB board. The output level can be matched to the PB monitor amp with RV6.

Decoupling for the +/-24V and +/-15V power supply rails is also provided by means of capacitor/inductor circuits shown at the lower left corner of the schematic diagram (Figure 5-3).

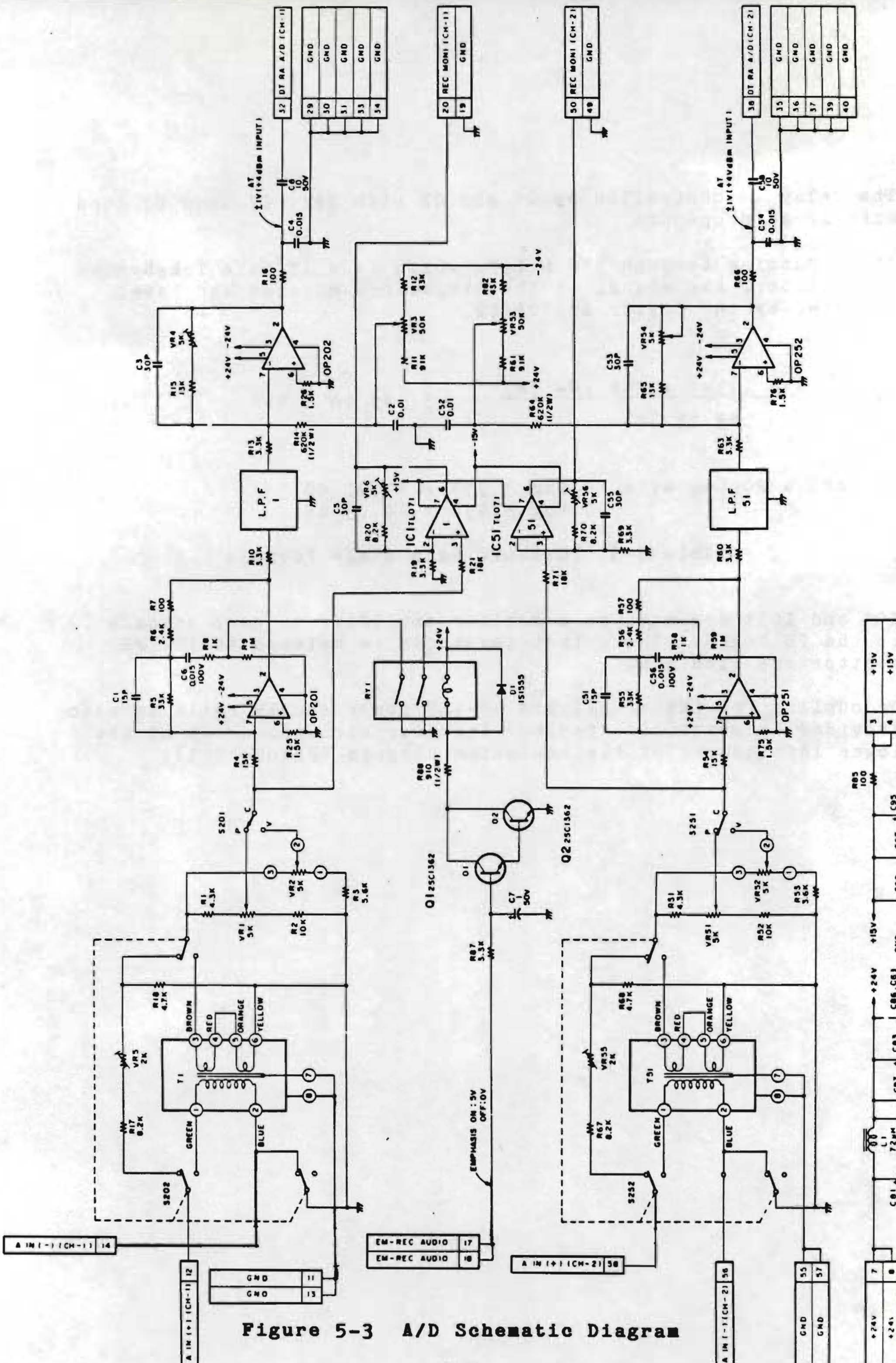


Figure 5-3 A/D Schematic Diagram

5.2.2 A/D Board

The A/D board performs the following:

1. Performs a S/H function on the analog signal for A/D input
2. Converts the analog signals to parallel digital data
3. Performs a parallel to serial data conversion.

Referring to the schematic diagram (Figure 5-3), analog input signals (DTRA A/D) are converted to digital audio data outputs (A/D out). The BUSY signal is produced during the conversion period. WDCK and BIT CK are input control signals for the board. The encoder input signals are switched by the combination of Analog/Digital/Dubbing switch and the Encoder and Digital I/O boards.

Refering to the timing diagram (Figure 5-4) and the schematic diagram (Figure 5-3), WDCK A/D is input to the mono-stable multivibrator IC-A5 to derive a pulse to be supplied to CONTROL IN on the S/H at which time the S/H remains in the sample mode. When the pulse ends, the S/H returns to the HOLD mode. With the delayed pulse from IC-A4-13, and A/D command pulse is output by Q of IC-A4-12. This pulse command is sent to the TRIGGER IN on the A/D at which time the A/D starts converting. The conversion time is set so that a 16-bit conversion is completed before the next WDCK A/D input.

With the trailing edge of the $\overline{\text{WDCK}}$ A/D pulse, the parallel output of the A/D is loaded into the P/S shift registers IC-A2, 3-A7, A8. This parallel data is then converted to a serial bit stream as A/D out and clocked by the BIT CK A/D signal. The BUSY signal is used to set the conversion time fo the A/D by VR103, 4.

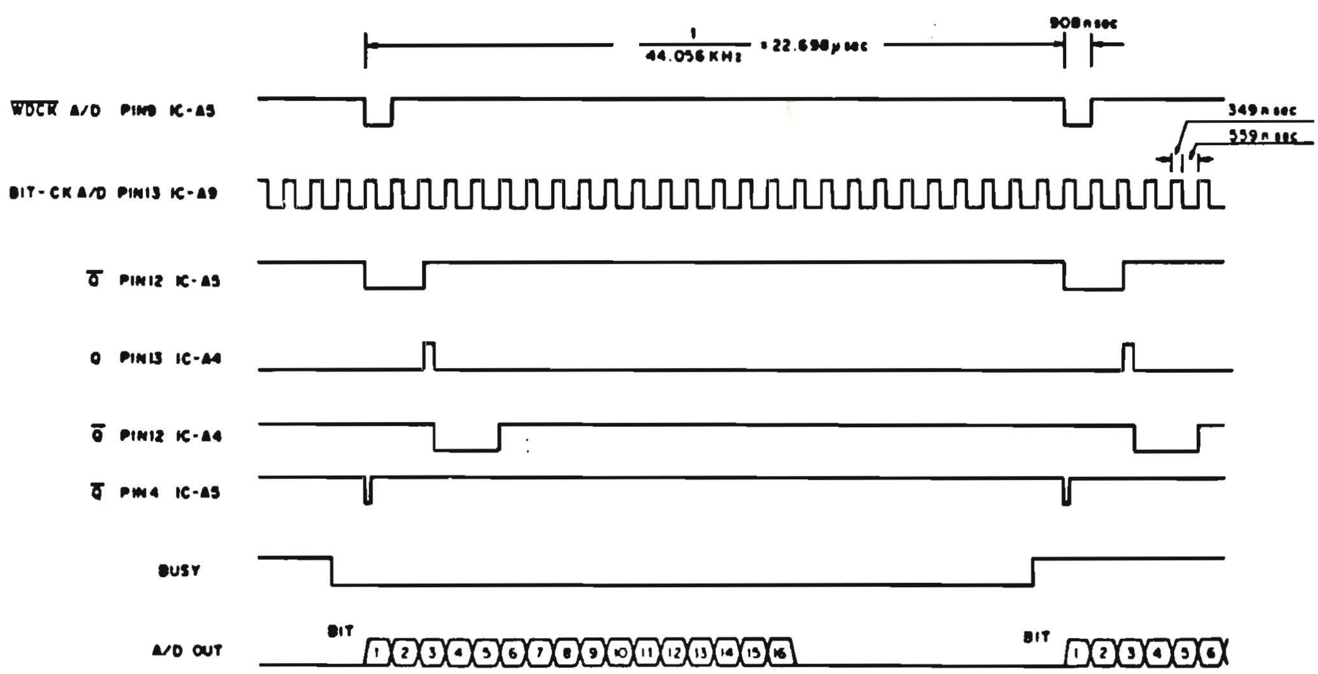


Figure 5-4 A/D Timing Diagram

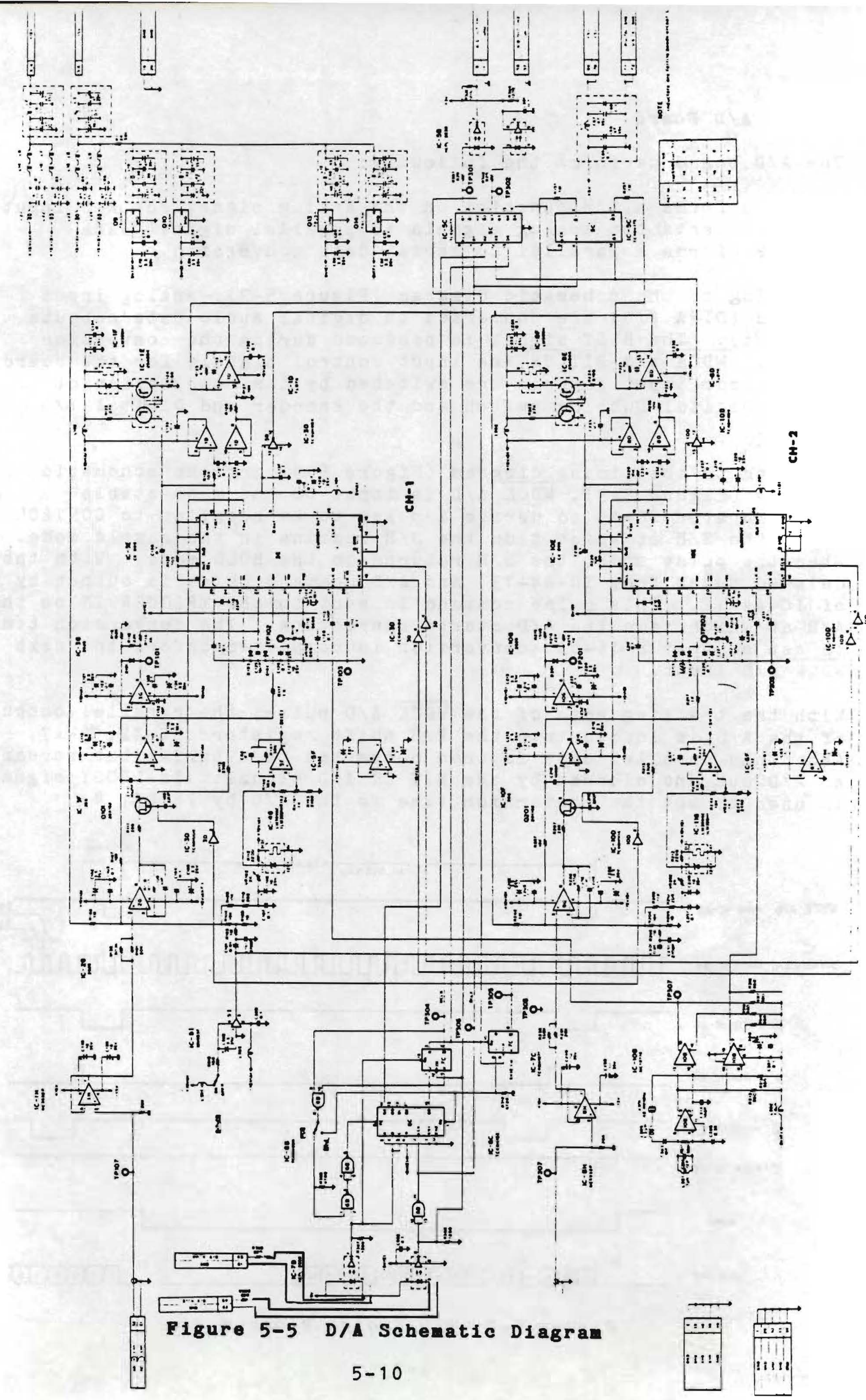


Figure 5-5 D/A Schematic Diagram

5.2.3 D/A Board

The D/A board performs the following functions:

1. Serial to parallel data conversion
2. Digital-to-Analog conversion
3. De-glitching and aperture time correction.

Referring to the schematic diagram (Figure 5-5) serial data (DT D/A ME) is fed into the shift registers and then latched into the D/A converter by $\overline{\text{WDCK}}$ D/A signal. The D/A converter generates an equivalent output current to the analog switch (IC-A4) and is converted to an output voltage (DT D/A PA) by the current-to-voltage converter.

Refer to timing diagram (Figure 5-6) and the schematic diagram (Figure 5-5). 16-bit data (DT D/A ME) is input to the S/P shift registers IC-D1 and IC-C4 for channel-1, and for channel-2 IC-B12 and IC-C7. The serial to parallel conversion of each word takes 16 clock pulses. The parallel data is latched into IC-C2, C3, and C4 with the trailing edge of $\overline{\text{WDCK}}$ D/A and is supplied to the D/A converter input. The output of the D/A converter is an analog current and is input to the buffer amp IC-B4 and led to the analog switch IC-A4. The analog switch operates as a sample and hold circuit which has the following functions:

1. Acts as a de-glitcher
2. To optimize the aperture time

The analog switch IC-A4 sends an output current to IC-A3, when aperture time (APCM) is high. IC-A3 acts as an I -> V converter and derives the analog (DT D/A PA) output. This sample and hold circuit is used to hold voltages between conversion periods and to reduce the effects of quantization noikse providing a more stable output signal with less artifacts of the sampling rate.

Inductor 13 is used as a frequency limiter to prevent slew rate limiting of the input current to IC-A3. This minimizes the generation of distortion.

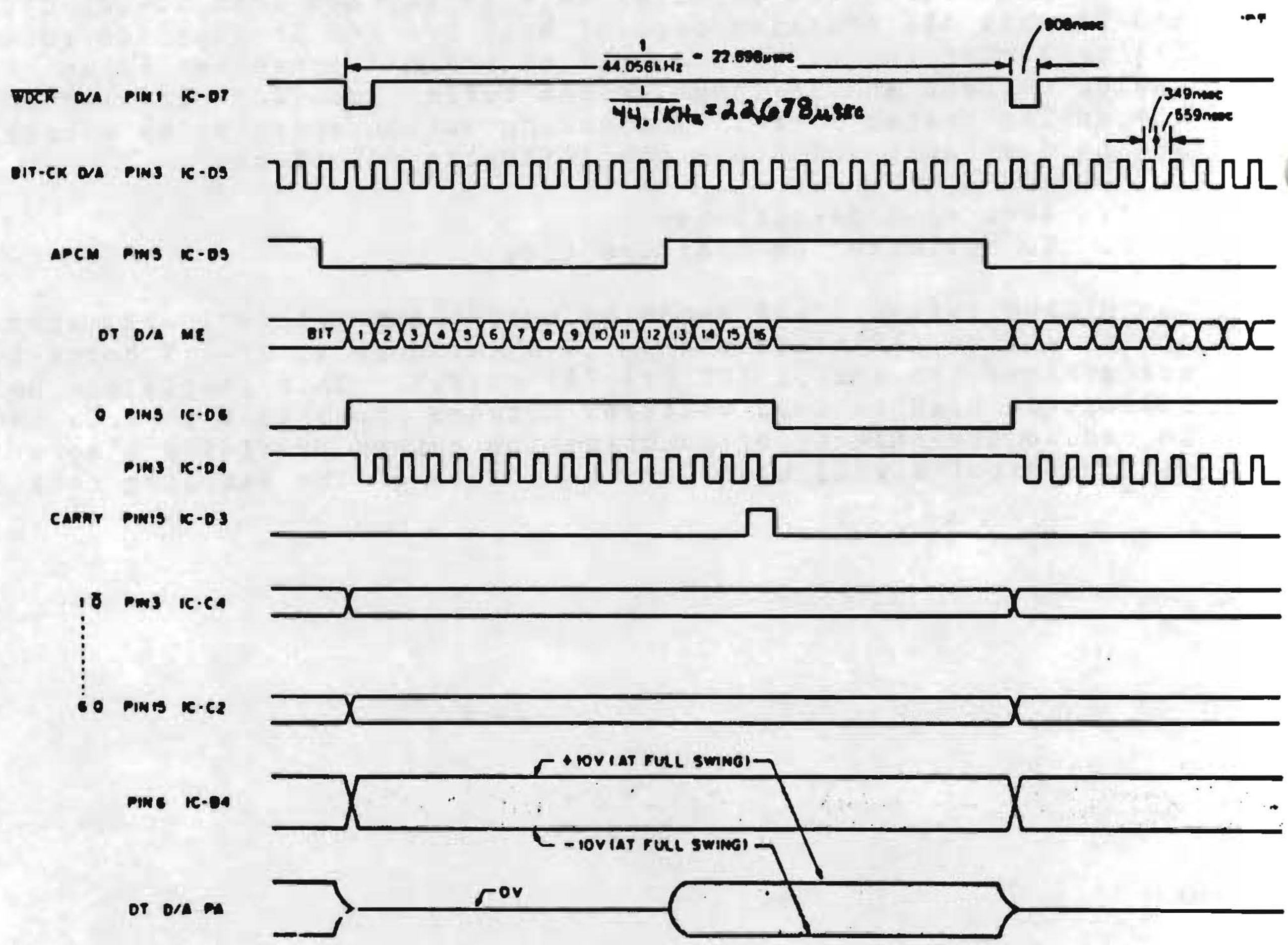


Figure 5-6 D/A Timing Diagram

5.2.4 Playback Board

Analog signal output from the D/A converter is buffered, level adjusted, de-emphasized, low pass filtered, and balanced returning it to the same representation as the original analog input waveform in the PB board. The PB board comprises the following functions:

1. De-empahsis
2. Adjusting the output level +/-6dB
3. Transformer In/Out
4. Headphone signal switching
5. Elimination of quantization noise

Refer to Figure 5-7. The D/A converter output signals are routed to the de-emphasis circuit which is activated according to the EMPHASIS bit in the data stream. From here the signals are routed to the input buffer amp IC1. The output of the buffer amp is connected to the low pass filter which will limit the output bandwidth eliminating the effects of quantization noise. The signals are then sent to the filter amp level adjusted. The signals are connected both to the output transformer and the headphone monitor amp. After passing the switching network, that switches between input/output sections, they are fed to the headphone amp and out to the headphone jack.

Signal input to the PB board is input to the De-emphasis circuit.

$$FCL = \left[2\pi \ (R1 + R2 + R3)\ C1 \right]^{-1} = 3{,}179\text{Hz}$$

$$FCH = \left[2\pi \ R3\ C1 \right]^{-1} = 10{,}638\text{Hz}$$

Table 5-4 De-Emphasis Circuit Formula

The emphasis signal from the Encoder turns on the relay emphasis network. Q9, Q10, R19, and C18 are encorporated to provide a long time constant to keep the relay enabled during a long dropout.

From the de-emphasis network, the signal is buffered and then sent through an L.P.F. because output signals from the D/A contain many high frequency components (quantization noise), aside from the basic signal. These are due to the switching of the D/A converter between samples. Some of these effects are removed by the aperature circuit, however, the aperature circuit can not remove all of these effects therefore the L.P.F. then limits the bandwidth to eliminate quantization components which are at a frequncy which is directly related to the sampling rate.

After passing through the L.P.F., the signal is processed by the filter amp OP1. The amp matches the load impedance of the filter and controls gain to the output.

$$\frac{1}{ZO_{vr}} = \frac{1}{R6} + \frac{1}{R7 + R8} = 3.33\text{k-ohm}$$

Table 5-5 Filter Amp Formula

The circuit gain of OP1 (filter amp) is adjustable by +/-12dB. The minimum gain Gmin is determined by R10 (20k-ohm), R7, and R8. The maximum gain Gmax is determined by R7, R8, VR2, R11, R12 and VR1.

$$Gmin = 20\ Log_{10} \frac{R10}{R7 + R8} = 13.4dB$$

$$Gmax = 20\ Log_{10} \frac{R10 + \dfrac{VR2\ (R11 + R12 + VR1)}{VR2 + R11 + R12 + VR1}}{R7 + R8} = 26.8dB$$

Table 5-6 Output Gain Structure Formula

VR1 (10k-ohm) is used to set the preset output level.

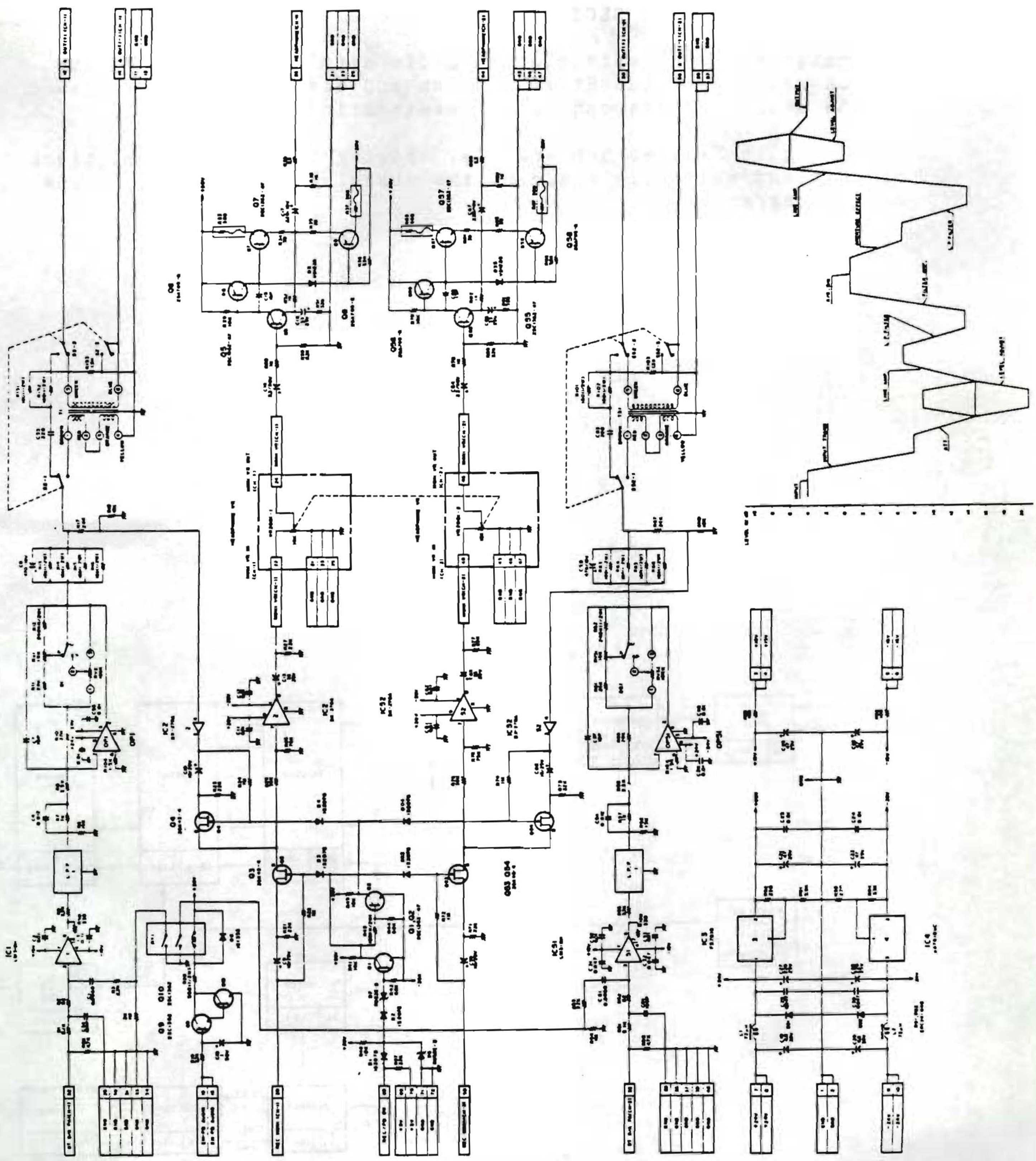


Figure 5-7 Playback Schematic Diagram

5.3 METER/MONITOR SECTION

The meter board accepts digital audio data depending upon the switch setting of the REC/PB switch and displays the data level on the meter corrresponding to readings in terms of dB.

Referring to Figures 5-8 and 5-9, showing the Meter board block diagram and schematic diagram, the description is given in the next paragraphs.

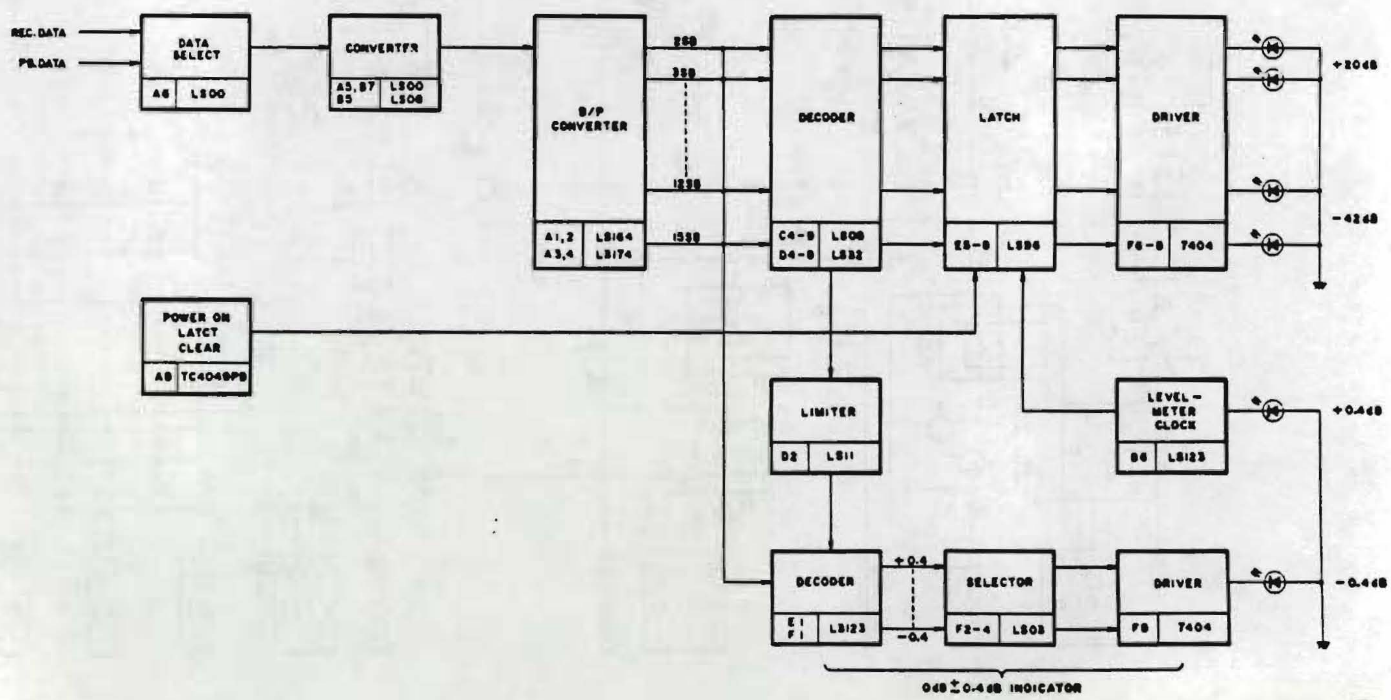


Figure 5-8 Meter/Monitor Block Diagram

Two sets of 16-bit digital audio data (DTME) which is the signal before encoding, and the input data to the D/A converter (DT D/A ME), are input to the board. The data selector (IC-A6, B8, B9) selects either the Record or Playback data and presents the appropriate data signals to the absolute value circuit comprising of IC-C1, A5, B5, B7. The absolute value circuit examines the MSB of the 16-bit data. If the MSB is 0, the data is positive and is retained. If the MSB is a 1, this represents negative data and all 16-bits are inverted.

The 3 LSBs are not used as their information weight is too small. The MSB designates magnitude response and is therefore not used. The serial data is then converted to a 12-bit parallel word by the S/P converter comprising of A1 through A4, and is then decoded by the AND-OR logic array of IC-C4 through C9 and D4 through D9. The decoder logic is arranged so that all LEDs from -42dB to +20dB are lit when enabled and the LED corresponding to +0.4dB to -0.4dB are lit individually, only when the level of data is within +/-0.4dB of 0dB.

The dynamic ballistics of the meter circuitry are controlled by the latch combination IC-E5 through E9 and the clock pulse from IC-B6. The meter will follow momentary increasing surges in input level and will decrease by 1 LED per clock pulse if the input level drops so that the decay time from +20 to -00 is approximately 1.2 seconds.

The latched data is then presented to the drivers which are IC-F5 through F9 and output to their corresponding LEDs. ICA9 and B9 make up a Power Up latch clear circuit, so that upon power up, all LEDs are turned off.

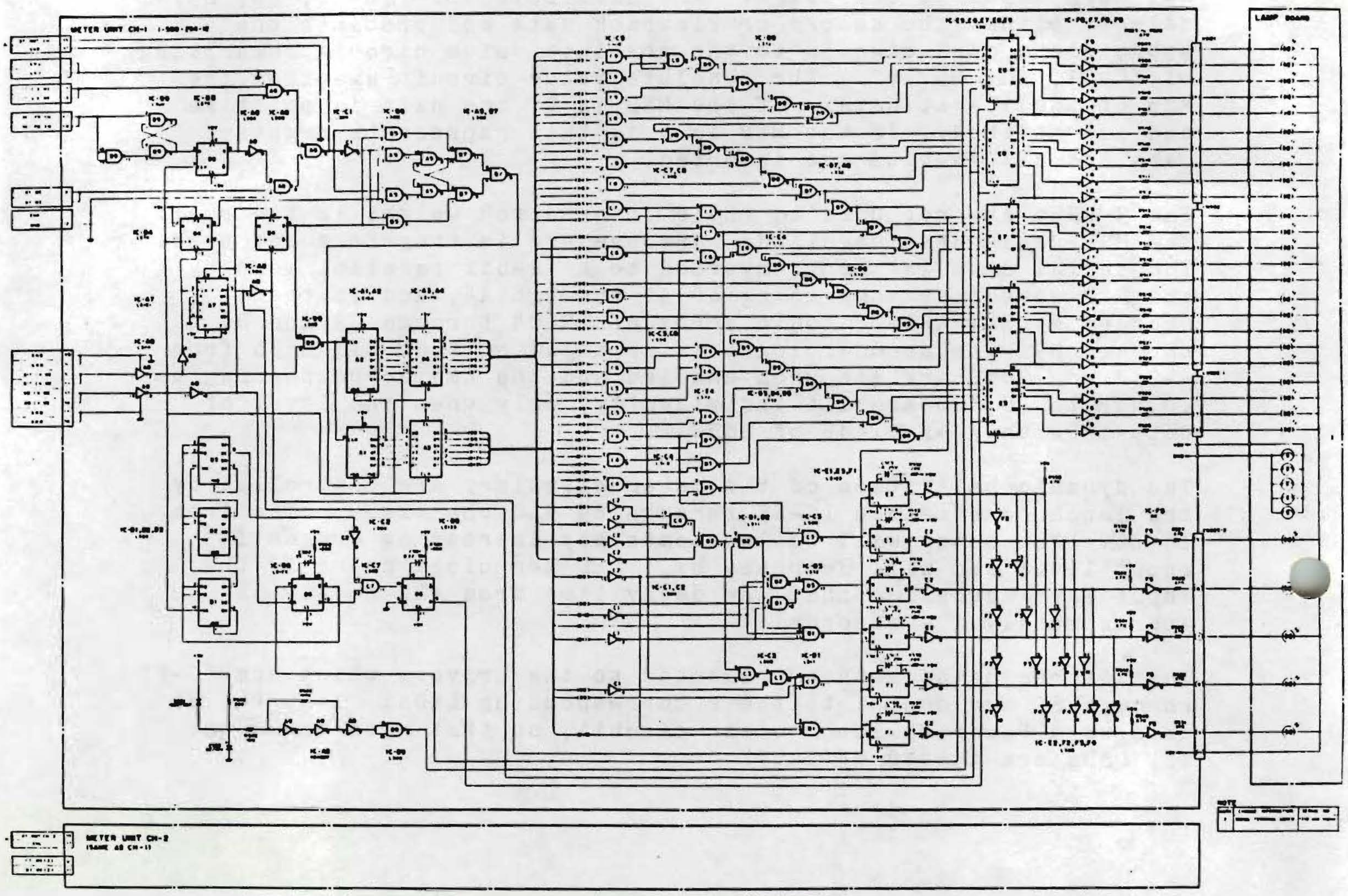


Figure 5-9 Meter/Monitor Schematic Diagram

5.4 COMPOSITE DIGITAL (VIDEO) SECTION

5.4.1 Encoder Board

The digital audio data from the A/D or digital input signals from the Digital I/O are processed by the Encoder Board and output as an NTSC compatible composite digital (video) signal via the Video Out Board. The Encoder performs the following functions:

1. Word interleaving
2. Addition of error correction and detection bits
3. Time division/multiplexing of the two stereo channels
4. Time compression of the data stream
5. Addition of skew bits for the identification of emphasis and sampling frequency.

Referring to block diagram (Figure 5-10), the data selector comprising of IC-A3 and A4 selects digital audio data from the A/D converter, the Digital I/O, or the Decoder (in the case of dubbing). Data selection depends upon the switch settings on the A/D and D/A boards.

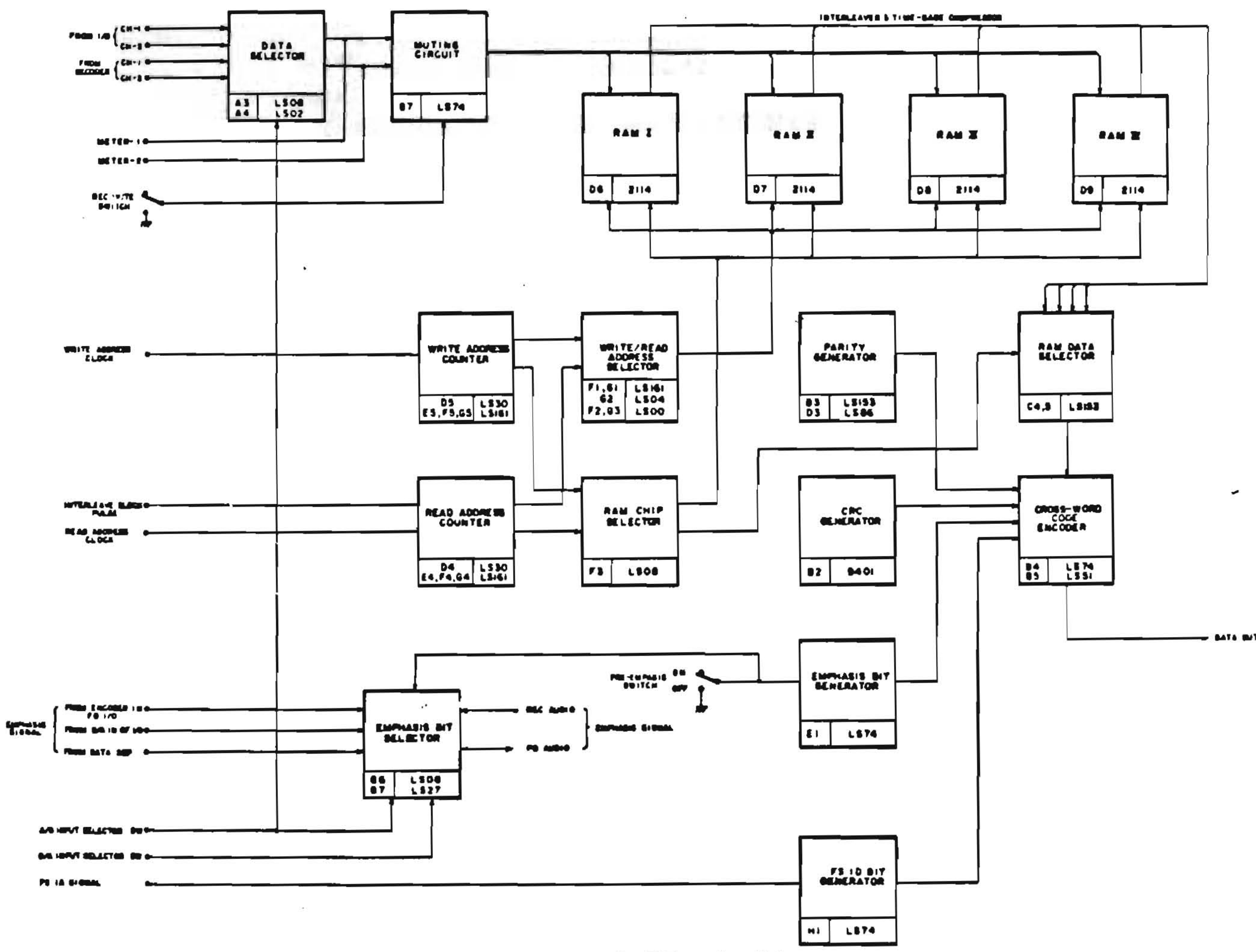


Figure 5-10 Encoder Board Block Diagram

The muting circuit enabled by the REC MUTE switch on the front panel, inhibits data flow (all zeroes) to prevent oscillation during A/D selection or if a blank interval is to be recorded. The data is then written and read by control signals from the read/write address counter, read/write address selector and RAM chip selector. The data is then interleaved and compressed by the RAM Memory where each RAM is 1k x 4 bit. At the same time, parity, CRC, emphasis and sampling frequency ID bits are added to the data format by the crossword code encoder. The final interleaved data is sent to the Video Out Board.

5.4.1.1 Encoding and Interleave Structure

The delayed left (L) and right (R) digital audio data consisting of 2 parallel 16-bit data words are written into RAMs I-IV as shown in Figure 5-11. Since the RAMS are 1k x 4, Figure 5-13 shows the correct addressing of data for the L and R channels. Two words of data (32 bits) are written in the RAMs in the order of RAM I, II, III, IV. Each RAM will contain 210 words comprising of 105 words each for the L and R channels per RAM. Figure 5-12 shows the format in which data is written and read from RAM, i.e., when data is written into RAM I, it is simultaneously read from RAM III. In the same manner, when data is written into RAM II, it is simultaneously read from RAM IV. The reading speed is three times faster that the writing speed and the data is sequentially read from line 1 to obtain the configuration shown in Figure 5-13. Figure 5-13 shows the relationship of the data words, parity, which is the exclusive, or of the Ln and Rn channels and CRCC which is check which is a check code used to detect errors in the data path. Interleaving of data is performed by sequentially reading from line 1 in Figure 5-13 to the format shown in Figure 5-14. Each horizontal line contains 193 bits consisting of 9 data words (16 bits), 3 CRC words (16 bits) and 1 skew bit for the identification of emphasis and sampling frequency. The left and right channels are arranged such that the time difference between odd and even numbered data words are 23.33H (210/9) apart. In so doing, errors in data are correctable since the error word is dispersed by virtue of interleaving.

Since each interleave block is equal to 35H (horizontal lines) and there are 7 interleave blocks/1 video field. Then there are 7x35 = 245H/field. And there are 105 w/block x 2 ch x 7 blocks/field = 1470 words/field.

Referring to Figure 5-15, the skew bit information is inserted on the 129th bit of each H line. The detection of emphasis and sampling frequency is such that if the skew bit on the 1st H line of each interleave block is low emphasis is enabled. Sampling frequency of 44.1kHz is used when the skew bit on the 2nd H line of each interleave is low.

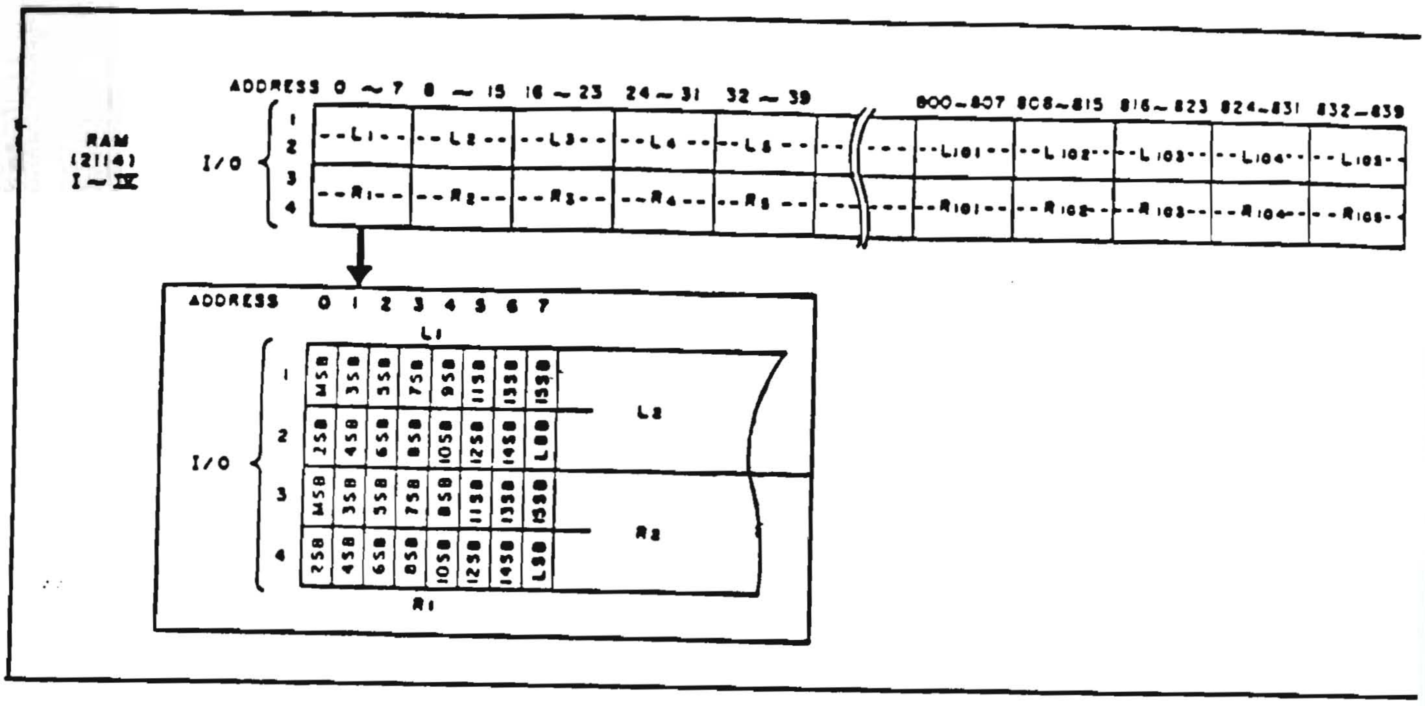


Figure 5-11 Addressing of RAMs

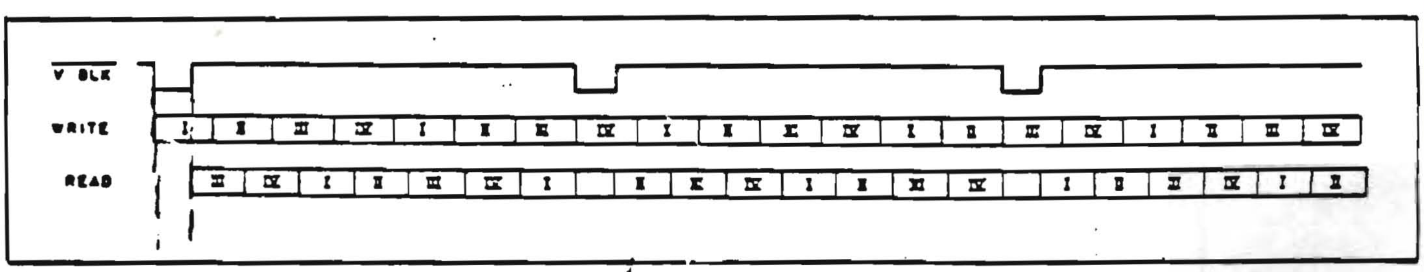


Figure 5-12 Data Read/Write Format

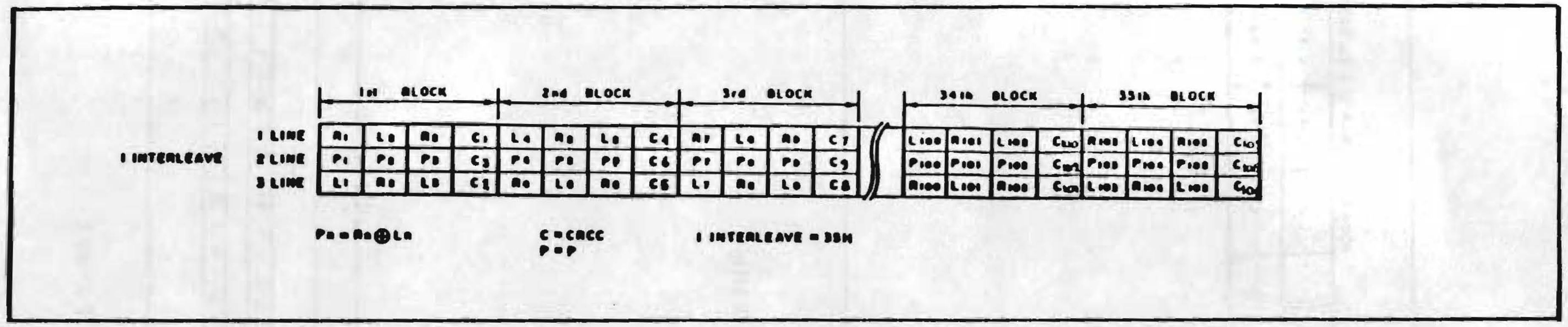


Figure 5-13 Interleave Data

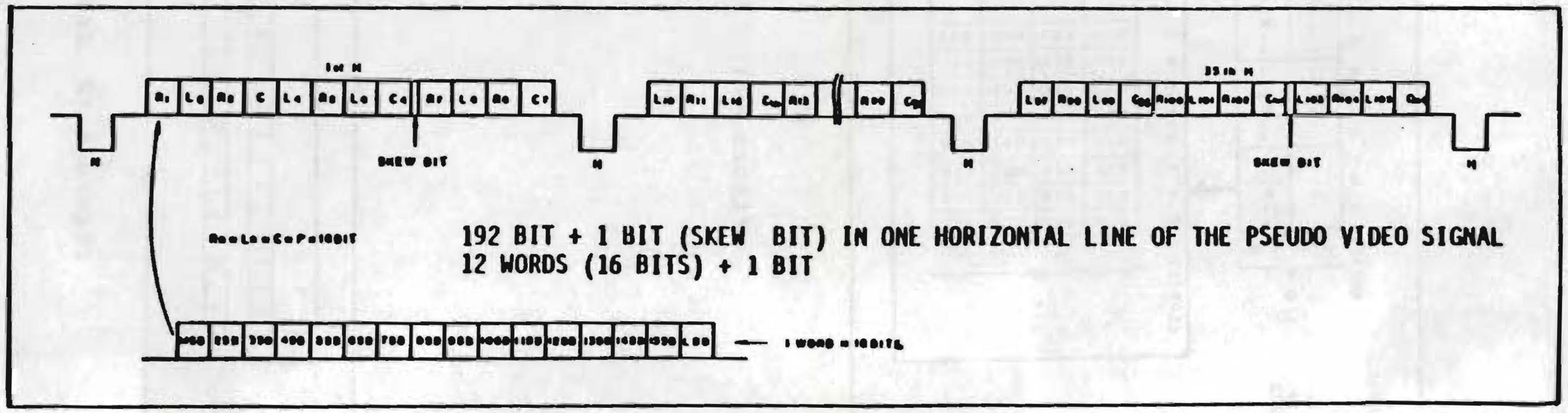


Figure 5-14 One Horizontal Line of Composite Digital (Video)

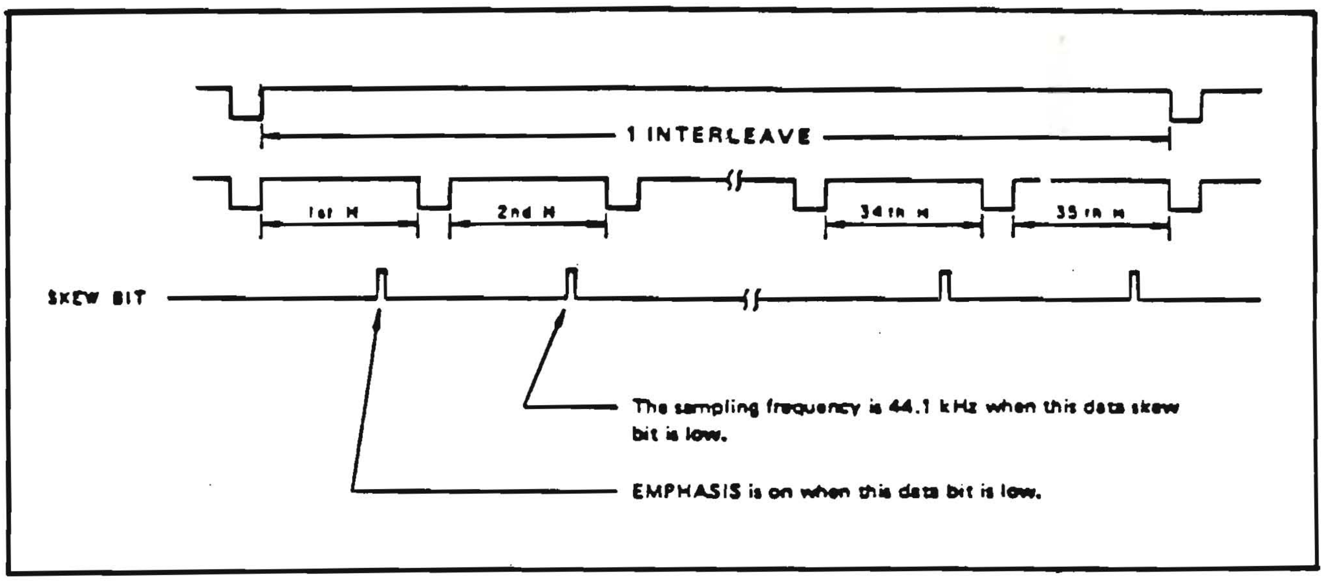


Figure 5-15 Skew Bit Information

Referring to the Encoder schematic (Figure 5-16) and block diagram (Figure 5-10), the data selector (IC-A2, A3, and B6) selects between A/D converter output data and the data signals from the Decoder Board. When the dubbing mode is enabled, Pin 41 goes low thus switching to the data from CH1-2 out. Since the selection of modes is by manual operation, IC-B6 in conjunction with the clock supplied by IC-D6 switches the data in an interval where data is not present, thus allowing the switching of signals without abrupt transients.

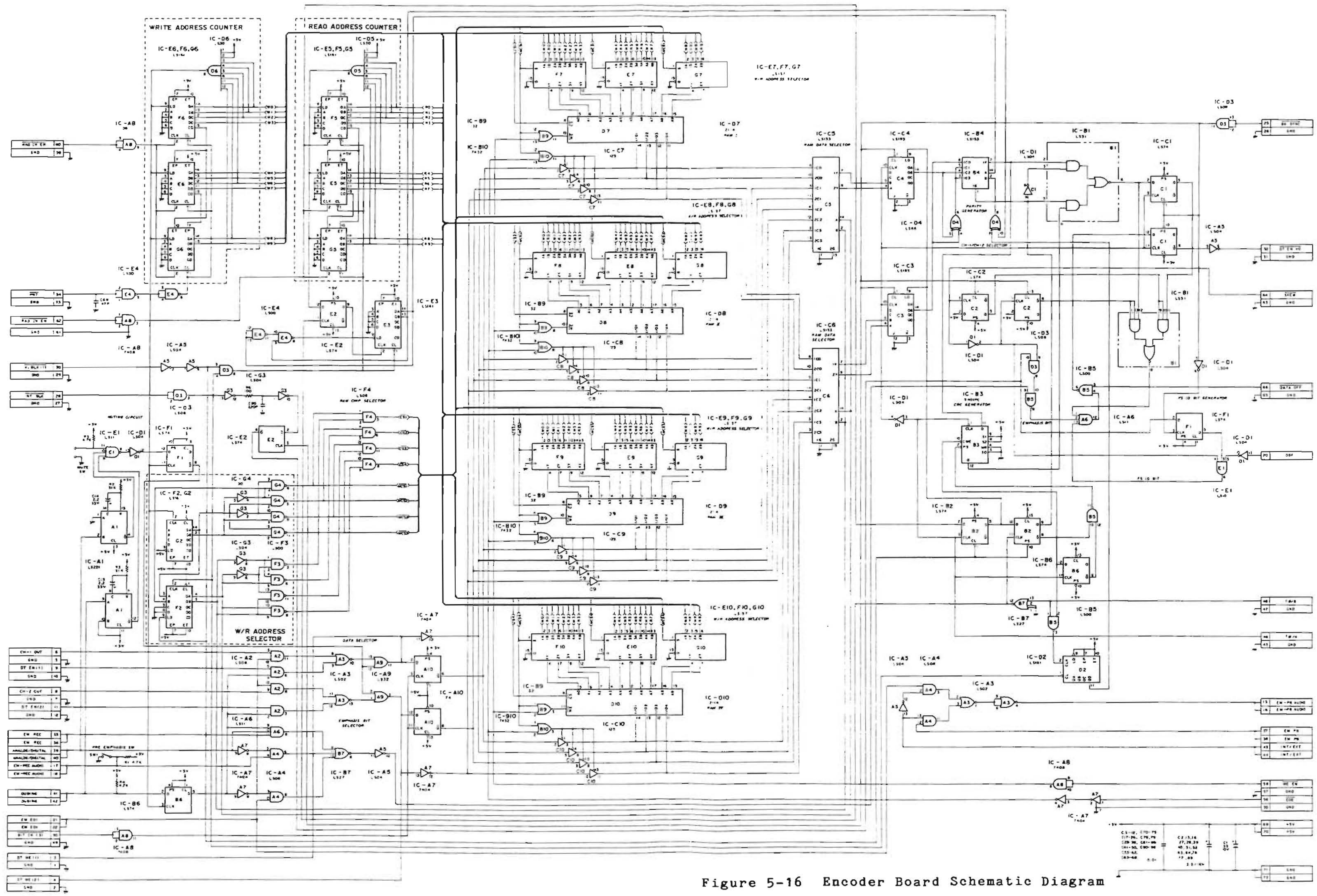


Figure 5-16 Encoder Board Schematic Diagram

ENCODER BOARD

5.4.1.2 **Muting Circuit**
(IC-A1, D1, E1, F1, and A9)

The mute circuit is used to prevent a loop when the processor is in E-E mode; when the audio input and output is looped. A 78msec mute signal (all zero data) is produced using the ANALOG/DIGITAL signals (pins 39 and 40) and dubbing signals (pins 41 and 42) with the mono multivibrator (M.M.V.) IC-A1 "ANDED" with the signals from the momentary REC MUTE switch. This produces a logic high on pins 3 and 8 of IC-A9 via IC-F1 when MUTE is enabled.

5.4.1.3 **S/P Converter**
(IC-A10 and A7)

Data converted into 2 lines of data after passing through the muting circuit. Data signals are formed into data with a delay of 17usec by IC-A10 which uses BIT CK (3) as a clock, thus becoming parallel signals of 2 lines per channel. The output pairs are from pins 10 and 12 of IC-A7 and pins 6 and 8 of IC-A10.

5.4.1.4 **Write Address Counter**
(IC-F6, E6, G6, and D6)

The Word Clock Enable (Pin 60) signal is used to clock the write address counter. IC-E6, F6, G6, and D6 form an 840 count ring counter. Pin 8 of IC-D6 produces a clock dividing 1 field into 7 parts. The data is 2 line parallel signals. Since 1 word comprises of 8 addresses, 840 counts divided by 8 addresses/word is equal to 105 words and 105 x 2 = 210 words after combining CH1 and 2 data into one RAM.

5.4.1.5 **Read Address Counter**
(IC-F5, E5, G5, and D5)

The Read Address Counter performs the same function as the Write Address Counter, that is 840 counts are performed to re-arrange the data in the format shown in Figure 2-9. The counter is clocked by RAD CK EN: 62, which consists of a 24 pulse clock per cycle, such that 1H = 3 blocks where 1 block = 24 clocks = 1 word = 8 clocks.

5.4.1.6 **W/R Address Selector**
(IC-G2-G4, G7-G10, F2-3, F7-10, and E7-10)

Clocked by pin 8 of IC-D6, IC-G2 and F2 produce timing for the Write and Read clocks, respectively. Clocked by IC-G2, and F2, the inverter, NAND logic consisting of IC-G3 and G4 then produce the appropriate Write and Read timing using the data selectors IC-F7, E7, G7, F8, E8, G8, etc. for the four RAM chips.

5.4.1.7 RAM Selector
(IC-F4)

RAM Chip Selection of RAMs I through IV accomplished by ANDing IC-G4 and F3 signals to IC-F4 which then selects each RAM at the appropriate time.

5.4.1.8 RAM Data Selector, P/S Converter
(IC-C5 and C6) (IC-C3 and C4)

Output data from RAMS I through RAM IV are made available to the RAM Data Selectors IC-C5 and C6 which are 4-to-1 line decoders. Output data is selected by timing signals from IC-F2 (QA and QB) such that the MSB and all odd bits of CH-1 are input to pin 5 of IC-C4 and the 2SB and all even numbered bits of CH-1 are input to pin 4 of IC-C4. Similarly, all odd data bits of CH-2 are input into pin 5 of IC-C3 and even numbered bits into pin 4 of IC-C3. IC-C4 and C3 convert the parallel data for each channel into a serial bit stream.

5.4.1.9 Parity Generator, CH-1/CH-2 Parity Selector
(IC-C4) (IC-B4)

The outputs of IC-C5 and C6 are used to derive the parity data by clocking the CH1 and CH2 data words through IC-D4 which is an exclusive OR gate. The output of pin 6 of IC-D4 in conjunction with outputs of IC-C4 and C3 then decided the parity bit pattern output by the parity generator.

5.4.1.10 CRC Generator, Skew Bit Addition Circuit
(IC-B1 and B3) (IC-B1, C1, C2, and D1)

Clock signals from pins 46 and 48 which are f0/4, f0/8 in conjunction with the output of the parity generator produce corresponding CRCCs calculated by the CRC generator chip IC-B3 and are added to the data stream via IC-B1. The output of IC-B1 is delayed by IC-C1 by one bit so that the combination of IC-C2 and D1 can determine the bit interval to insert the skew bit. These two inputs are then latched into IC-B1 so that the skew bit is inserted in the 129th bit position.

5.4.1.11 Emphasis Circuit
(IC-G3, E2, D3, B5, A3, A4, A5, A6, and B7)

Refer to the block diagram (Figure 5-10) and the schematic diagram (Figure 5-16). Emphasis selection is decided by the Encoder Board switch position and the A/D input switch selection. The determined output is a combination of IC-A3, A4, A5, A6, and B7 gate circuits. If emphasis is selected to be encoded, pin 8 of IC-B5 outputs a low going pulse.

5.4.1.11 Emphasis Circuit continued
(IC-G3, E2, D3, B5, A3, A4, A5, A6, and B7)

The INT BLK: 28 signal delayed by R6 and C80 is input to IC-E2 Pin 2 and is clocked by BK SYNC (IC-E2 Pin 3). The output of pin 6 of E2 is the clock for the 1st H Line of each interleave.

5.4.1.12 FsID Bit Generator
(IC-D1, E1, and F1)

Sampling frequency information is input to the DOF:20 input which goes high in the Drop Frame mode. Clock by BK SYNC:25, IC-F1 Pin 2 utilizes the output of IC-E2 Pin 6 of the Emphasis circuit to produce the second H sync window of each interleave.

5.4.2 Video Out Board

The principal functions of this board are to produce Master Clock signals for all boards, to synchronize the PCM to external composite sync or word sync, and to mix data interleaved by the Encoder board with NTSC sync signals to produce appropriate composite digital (pseudo video) signals to be recorded.

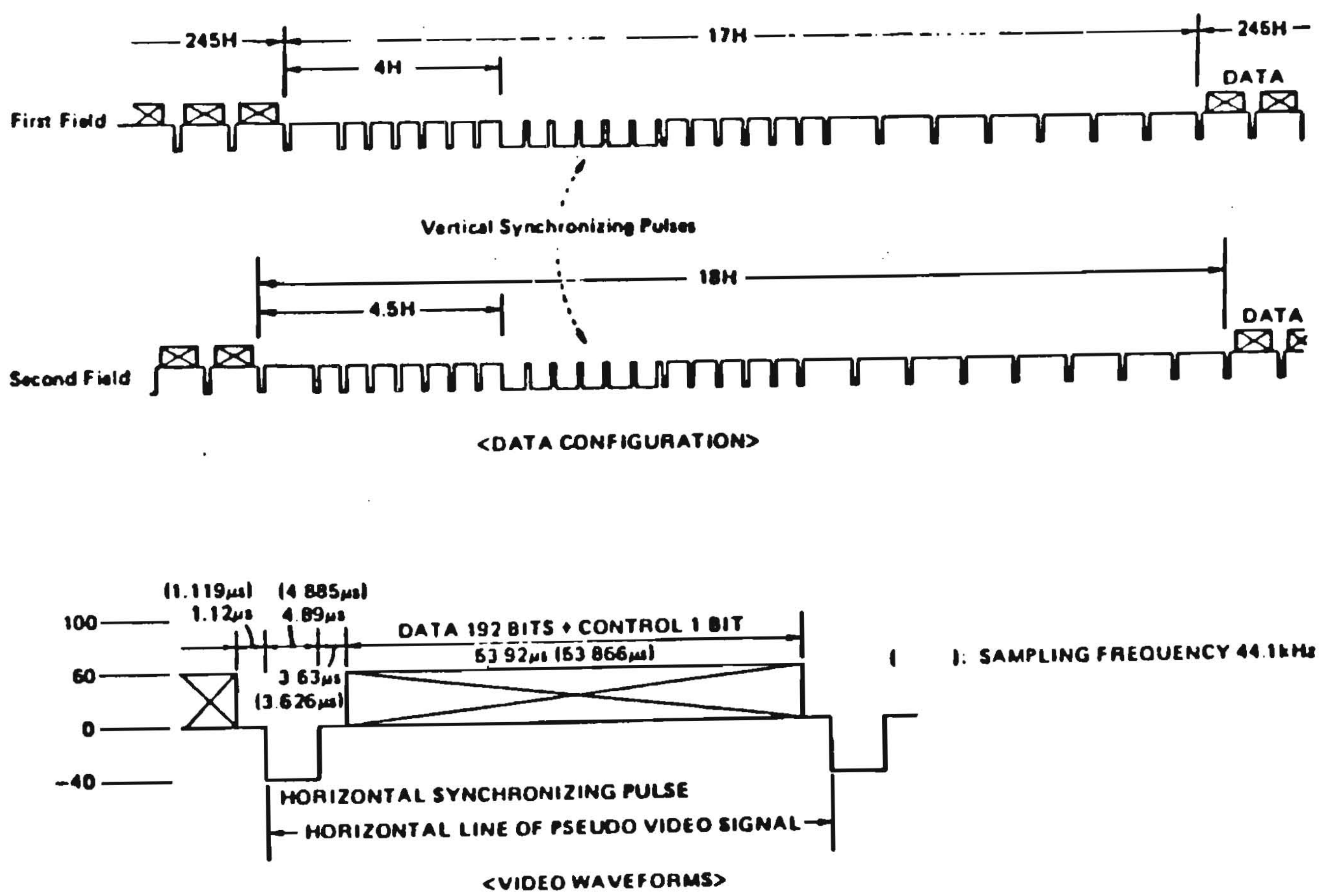


Figure 5-17 Composite Digital (Video) Signal Diagram

5.4.2.1 Video In/Out Format

Referring to Figure 5-17, the PCM processor produces an NTSC compatible comosite diigtal (video) signal for use by the modified VTR machines. Of the 525 lines per video frame, 490H are used for data and 35H are used for synchronization. The odd field has 245 data lines and 17 synchronization lines. Each H line stores 192 bits of data and 1 skew bit. Since the recording density output is related to the video signal and master clock frequency, they are easily derived.

1. Packing Density

$$= [\text{Data interval/H} \div \text{Bits/H}]^{-1}$$

$$= [53.9175\text{us}/193]^{-1} = 3.579545 \times 10^{6} \text{ Bits/s or Hz}$$

Master Clock

$$= \text{P.D.} \times 4 = 14.31818\text{MHz for } 44.056\text{kHZ}$$

2. Packing Density

$$= [53.86358\text{us}/193]^{-1} = 3.583125 \times 10^{6} \text{ Bits/s}$$

Master Clock

$$= \text{P.D.} \times 4 = 14.3325\text{MHz for } 44.1\text{kHZ}$$

Table 5-7 Packing Density

5.4.2.2 Analysis

Composite sync is input to the diode clamping network and Q7 which reduces the sync level to TTL level, and input to IC-G7. IC-G7 removes the equalization pulses and vertical sync and outputs H sync. WDCK in passes through the receiver IC-G4 and is fed to the switch combination IC-D13 as well as the H sync output. When both signals are input simultaneously, IC-D13 is switched by the output of the re-triggerable M.M.V. IC-E14 such that composite sync has priority.

The selected output as selected by IC-D13, is input to IC-E3 Pin 1 of the phase comparator utilizing a PLL circuit. When Comp. sync is selected, the output of IC-F1 VCO/PLL circuit is divided by 910 in the programmable counter comprising of IC-E11-13 and selected by the output signal from IC-D14 which is input to IC-E3 Pin 3; compared and phase locked.

In the same manner, when WDCK is input, the output of the VCO will be divided (de-multiplied) by 325 on the decoder board which is the division factor to derive the master clock rates.

The two internal VCO's comprising the PLL circuit have frequencies of 14.3325 MHz and 14.31818 MHz. This is due to the fact that the two external sync signals have frequencies of: WDCK = 44.1kHz or 44.056kHz and 15.75kHz and 15.734kHz for composite sync.

When sync is applied externally, the VCO output of the PLL becomes the Master clock. However, when no external sync is supplied, the master clock is derived by the internal clock oscillators of IC-H8 or 11 which is selected manually.

The external and internal clocks are switched by IC-F8. External sync detector IC-F11 controls IC-F8 to give preference to external sync such that the priority is: 1. Composite sync, 2. WDCK, 3. Internal sync. The resultant clock signal is supplied to the TV sync generator IC-F7, which produces composite sync, vertical and horizontal drive, and even and odd fields.

The composite sync output from the sync generator IC-B7 is then fed to sync amplifier of Q8-10 and output as composite sync out.

The master clock selected by IC-F8 is also fed to IC-B7, B10 where the Write Address Clock RAM control pulse for the encoder baord is produced. This clock is also sent to IC-C12-14 where the Read Address Clock RAM control pulse for the encoder board is produced.

The $\overline{\text{DT EN VO}}$ signal which is the encoded output signal from the Encoder is level adjusted by VR2 and mixed with composite sync from the sync generator through R8. This psuedo video signal is amplified by IC-C2 (video amp) and the level adjusted by VR1 and output through the buffer stage comprising of Q1 and Q2 as Video Out.

5.4.2.3 Sampling Frequency Discrimination Circuit

This circuit decides upon the priority of clock signals input and switches the PLL/VCO circuit so that external sync can be applied appropriately. The work clock or comp. sync is sampled individually and divided to a lower frequency. Since the difference between 44.1 and 44.056kHz is 0.1%, and is hard to discriminate, the master clock is used as a reference. The master clock is counted with a programmable counter with a threshold value to discriminate the difference between the two clocks and a decision is made based on the output. A detailed analysis is as follows:

Word Clock (WD CK) or Composite Sync is selected by IC-D13 and is supplied to the clock input of pin 2 of IC-E9. This counter divides the word clock by 14 and composite sync by 5 and the carry (CRY) output being the same frequency (IC-E9 pin 15). The division value is changed by the output Q of the Comp. sync detector IC-E14 such that a high is output for comp. sync and low for WDCK. Depending upon the switch selection of S1 which determines the internal sampling frequency used, the QD output of counter IC-G10 will output a high or low signal depending upon the external sync conditions. The CRY (IC-E9 pin 15) is divided by 4 at a 50% duty cycle by IC-E10 and output to 2Q. Referring to the previous discussion, this means that WD CK has been divided by 14X4 (56), and Comp sync by 15X4 (20). The NAND output of IC-F8 pin 11 consists of the latched 2Q output of IC-E10 pin 9 and of IC-F10 pin 8 which uses the internal master clock as a reference. The output of IC-F8 pin 11 outputs an LD pulse to the programmable counter comprising of IC-G11-13. The NAND output of IC-G8 pin 6 is used as EP pulses. The counter (IC-G11-13) therefore counts the number of internal master clocks with the LD and EP pulses as control and the discrimination signal is latched by the QD output of counter IC-G10 by the Q output of IC-F10 pin 5 by means of IC-F9.

5.4.2.4 Muting Circuit

The muting circuit supplies a muting signal to the Decoder board to prevent the generation of noises when the sync is disturbed when the PCM is driven externally. There are two conditions:

1. When WDCK is applied and is in perfect sync, the rising edge of the pulse on IC-D12 pin 6 will be within the range of "low" of the Sample/Latch signal and pin 9 of IC-D12 will output a "low". When out of sync, the rising edge of pin 6; IC-D12 will be out of range and pin 9 outputs a high to IC-D11, causing IC-A6 to output a mute signal.

2. When Comp. sync is applied and is in perfect sync, the rising edge of IC-D10, pin 11 will be in the range of "high" of the <u>CRY</u> pulse of IC-D10 pin 12 which is derived from IC-E11 and 13. In turn, IC-D10 pin 8 will become low. Similarly, IC-D10 pin 8 will become high if a muting condition occurs. The muting signal is selected by IC-D11, depending on whether WDCK or Composite sync is input. IC-C5 is a re-triggerable M.M.V. with a period of 0.45XCR and is supplied to IC-A6 where the signal is synced to the S/L signal and output to the Decoder.

5.4.3 Sync SEP Board

The Sync Sep Board Figure 5-18 receives the composite digital (pseudo video) signal from the (Video In) connector on the rear panel, separates the data and sync, and sends the data signal to the data separator circuit. The sync information is used to process the encoded data.

Video input at video in is terminated by R901 (75-ohm) and fed to the pedestal clamp generation circuit IC903 and data and sync sampling circuit IC902. Video signals input on IC903 Pin 3 are amplified by 7dB and DC clamped by diodes D901, 2. This is to reduce DC variations in the video signal. The signals are then sent to comparator IC906 (LM311) for sync and comparator IC907 (LM311) for data. IC906 separates the sync information from the video. The threshold DC level is set by RV903. IC907 separates data in the same manner with RV904 setting the threshold level. The sync output of IC906 is inverted by IC-E5 and fed to the M.M.V. IC-E2 which reduces the pulse widths to approximately 45usec. The output is then fed to the second M.M.V. IC-E2 Pin 9 to reduce the sync pulse widths to approximately 2.5usec. and fed to IC-D6.

The clock to IC-D6 is formed by the sync separated earlier and the MM pulse (50usec) of IC-F2. IC-G3 Pin 3 output is H sync. The Q and $\overline{Q}$ outputs of IC-D6 are latched by the CLR (Pin 1) input. The resultant output of IC-D6 (pin 8) are pedestal-clamp pulses to clamp the video level through Q901 and IC-901 after passing through Q906. The reason for this is so the video level has less DC variations so that Sync and Data can be extracted accurately.

IC-E1 forms a clamp pulse generator aux. circuit to prevent DC variations in video-in. IC-G3 is used to improve the recovery time fo the next signal when an interruption occurs, as in a long dropout.

Input video to IC-902 is amplified 7dB to reduce DC variations and data is extracted by IC-905 and supplied to the Data Sep board via terminal 42.

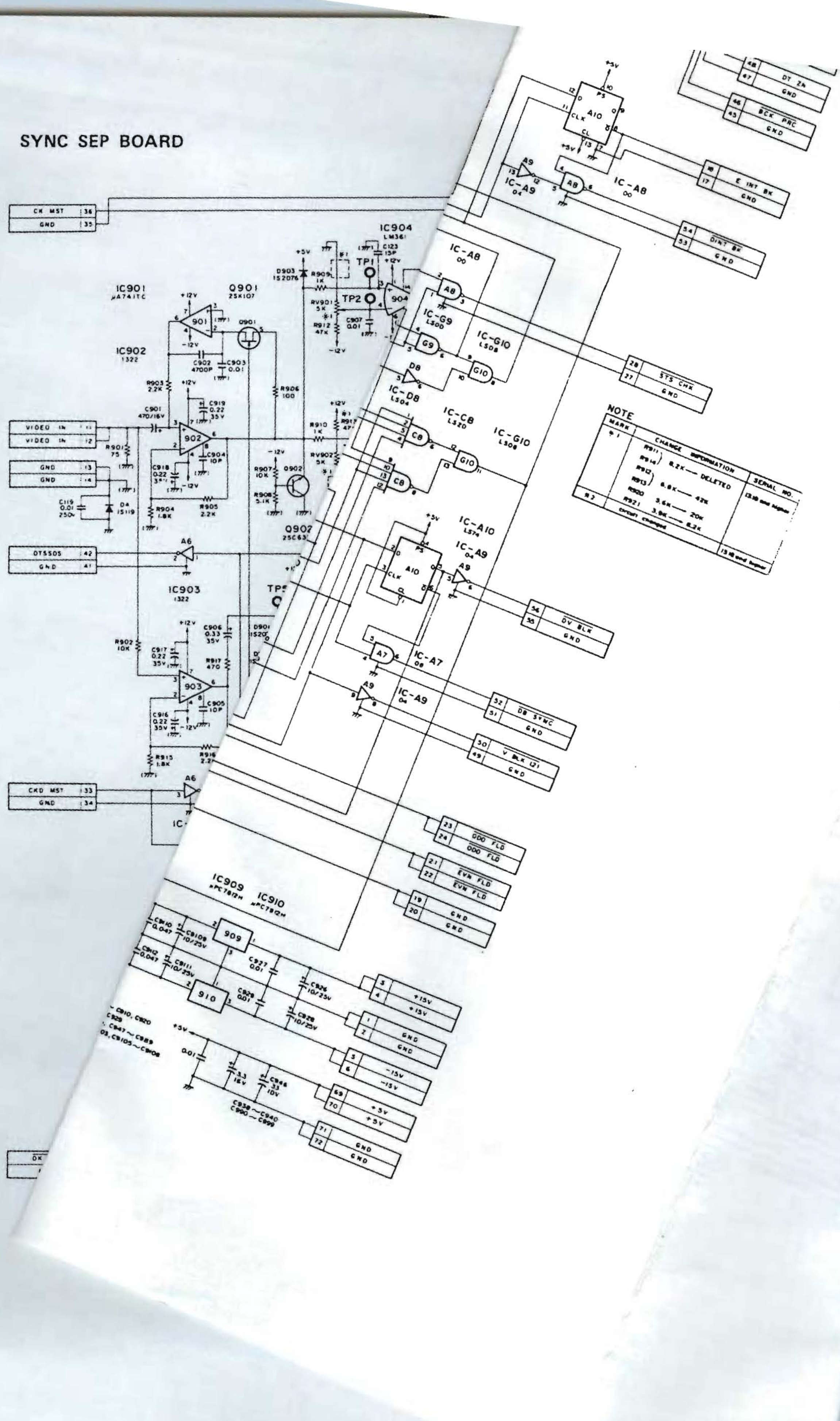
Sync Information is extracted by IC-904 and fed to the integrator circuit. Extraction of V-sync pulses are done by integrator R924 and C911 discharging through R925 and R926. This inverted sync is supplied to the integrator R928-931, C912, and C913 through Q905 which outputs a pulse to confirm the presence of V-sync. IC-E4 pin 2 accepts the inverted pulse from Q904 and gated with VD (vert. drive) from the Video Out, outputs the signal to the V-sync detector, IC-G5 which is an M.M.V. which produces a pulse of approximately 90usec During this interval, IC-G2 counts, and if there

are more than 4 sync pulses, the signal will be taken as V-sync and supplied to IC-C6 pin 15 via pin 11 of NAND gate IC-G9,. when pin 13 goes high.

H sync is confirmed by IC-B8 pin 9 which produces a load pulse in IC-B6, 7 if counting exceeds 54 counts (approx 3.78usec since the sync pulse width is 4.89usec). IC-A8 pin 8 produces a skew bit position pulse to show the position where data should be.

The H sync phase error detect (IC-C7) corrects the counters (IC-E6, E7, F6) by determining the shift in H-sync in 1 H period (as a slippage in data zone) by IC-D7 and returns it to IC-C7 pin 9. IC-B10 pin 5 outputs a pulse during vertical blanking on the EVEN and ODD fields. IC-G10 pin 3 outputs a CLR pulse in conjunction with the CLK supplied by IC-E8 pin 12 to the counters IC-D9, E9, F9 which produce decoding timing signals for the playback section. IC-C9 is used to detect errors in the time axis (V-sync); V period errors are detected by latching IC-C9 with the OK SYND on pin 2.

SYNC SEP BOARD



BOARD

Figure 5-18 Sync

SYNC SEP BOARD

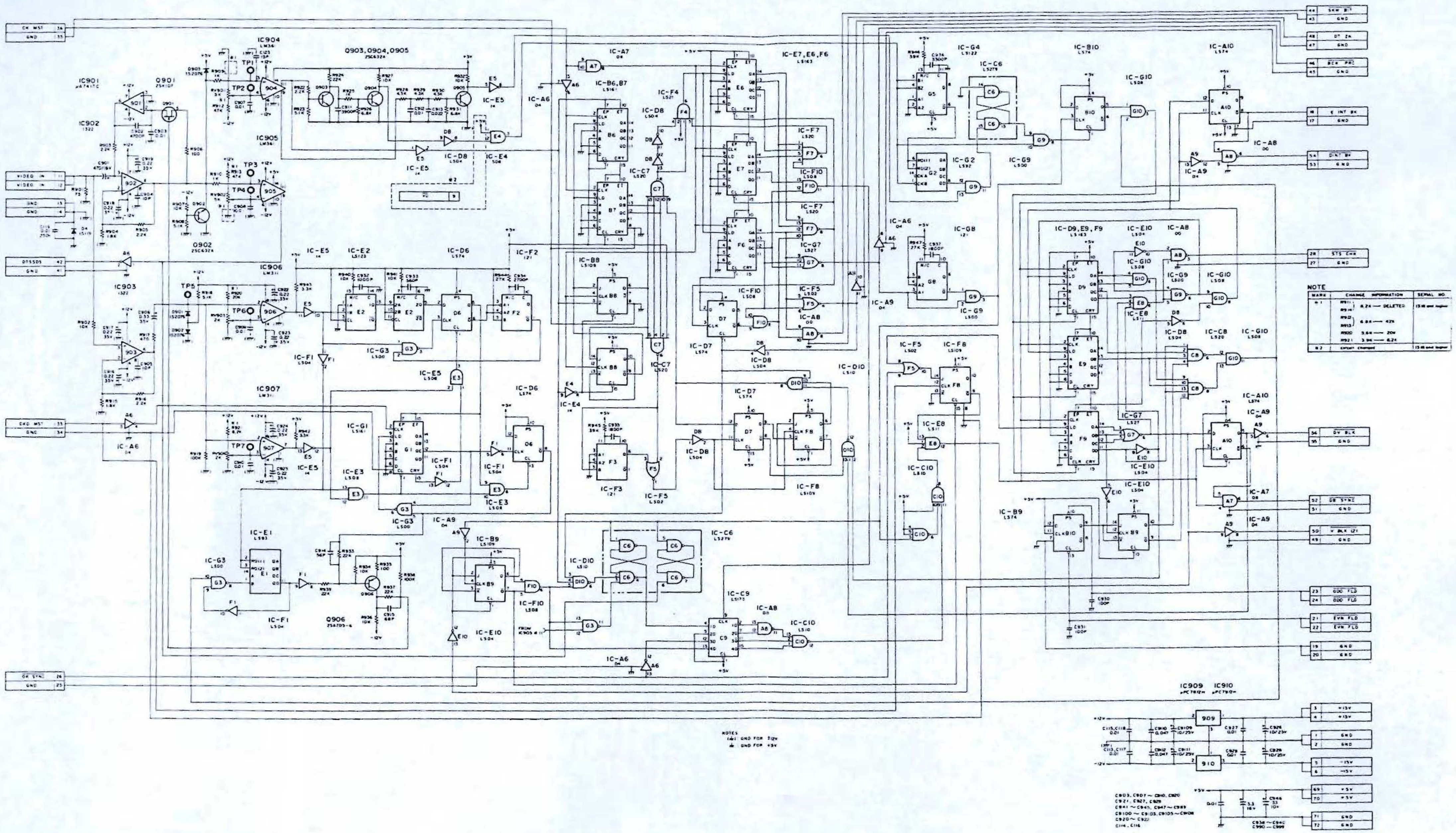


Figure 5-18 Sync Sep Board Schematic Diagram

DATA SEP BOARD

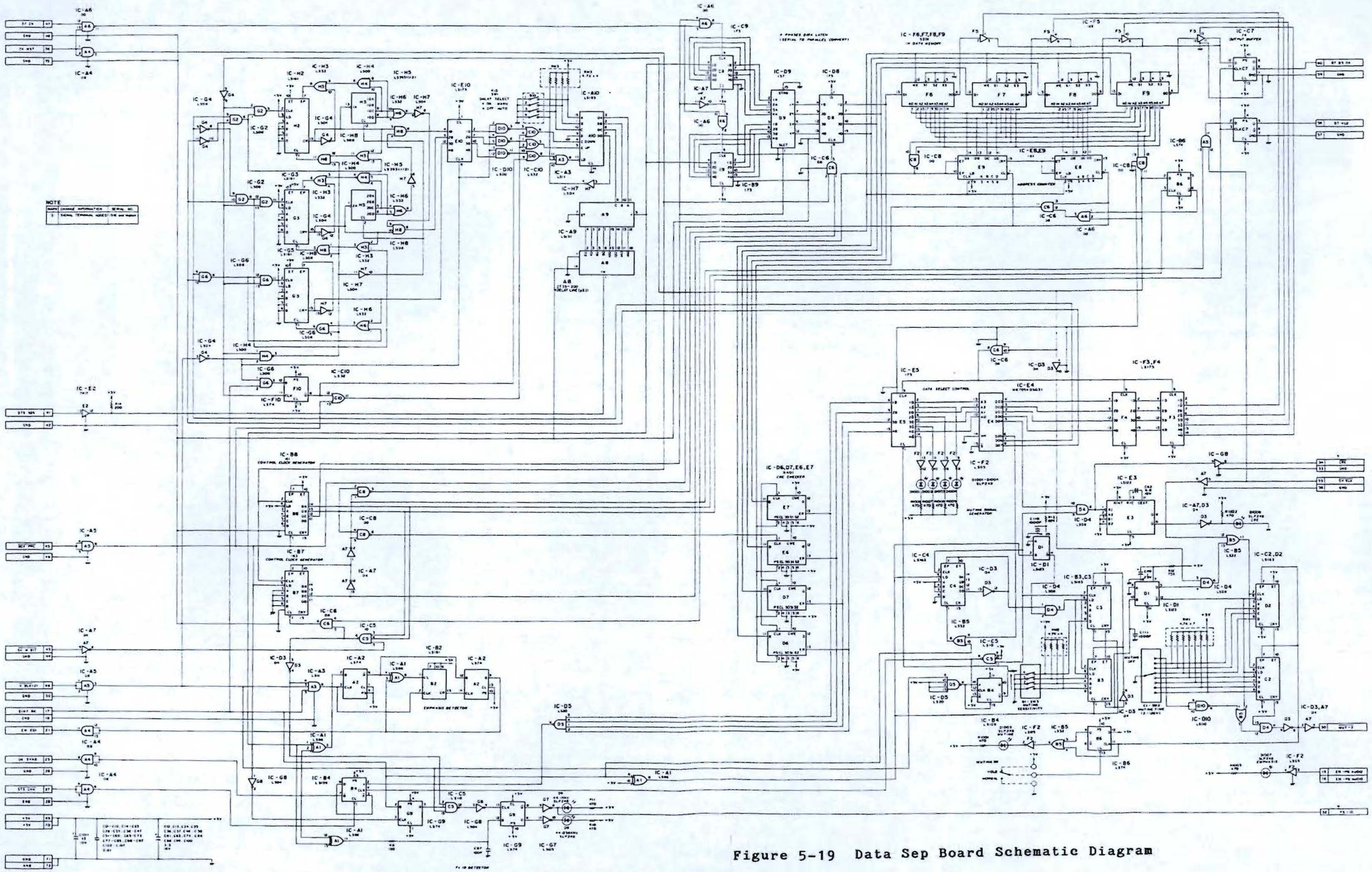


Figure 5-19 Data Sep Board Schematic Diagram

5.4.4 Data SEP Board

The DATA SEP board, Figure 5-19, uses the CRC to check the data; and the skew bits containing the emphasis and sampling frequency information are isolated from the PCM data. Muting signals are output to the decoder when the data is continuously defective.

5.4.4.1 Analysis

Output data from the sync separator is applied to A9-SW1 which delays the data via IC-A8 and is sent to IC-F6-F9. One data bit is divided into 4 block signals by IC-C9, B9 and stored in IC F6-F9 (1H memory). The same data is sent to IC-E7, E6, D7, D6 for checking by the CRC polynominal ($X^{16} + X^{12} + X^{5} + 1$). The 1H memory and the CRC checker are sequentially matched. the results of CRC checking will be latched by IC-E5 and input to the Rom IC-E4. The ROM IC-E4 checks input data with a pre-assigned truth table. When a decision is made, the ROM output is latched by IC-F3 and F4, and the data and phase stored previously are sent to IC-C7 and supplied to the decoder.

5.4.4.2 Emphasis Discrimination Circuit

Emphasis data is inserted on the 129th bit of the first H of each interleave. This circuit decides if emphasis is applied or not. Input signals, $\overline{\text{SKW BIT}}$, $\overline{\text{VBLK}}$(2) and EINT BK are clocked into IC-A2 pin 3 via AND gate IC-A3. IC-A2 pin 6 goes high when the D input is high. When the paired input of the EX.OR gate IC-A1 pin 1, 2 goes low, the Q output goes high with the next clock, thus causing the CLR of IC-B2 pin 1 to go high. Counting then starts and the "CRY" output, after 15 counts, becomes the clock for IC-A2 pin 11. This causes the Q output to go high which signifies the emphasis off condition. When the D input of IC-A2 is low, the Q output (IC-A2 pin 6) becomes "low" which causes the CLR terminal of IC-B2 to become high. The EM EDI signal becomes low signifying emphasis on.

5.4.4.3 Sampling Frequency Discriminators

IC-G9 and the nearby gates make up the Fs discrimination circuit. It tests the logic state of the 129th bit of the 2nd H in each interleave. The logic state is a high for 44.056kHz and low for 44.1kHz. The data is supplied to IC-G9 pin 12 and is output from Q and $\overline{Q}$ through IC-G7 to drive the LEDs.

In the muting circuit, SW2 selects the muting time between 2 and 128 TV vertical intervals or from 33ms to 2.13 sec. SW3 selects the length of mute intervals allowed. When mute occurs, pin 5 (DO5) of IC-E4 (ROM) goes low thus causing IC-B3 to always clear due to a low state on pin 1 CCLs.

As a result, IC-C3 pin 9 and C4 pin 9 go high. By counting the quantity decided by SW3, CRY of IC-C4 outputs a pulse which triggers the monostable M.V. IC-D1. The output pulse of IC-D1 loads the counters IC-D2 and C2 by the amount decided by SW2 (muting time), during which time muting is applied.

5.4.5 Decoder A Board

The decoder A board, Figure 5-20, processes the information sent from the Data Sep board and through CRCC, outputs correction signals to the Decoder B board according to each error. In addition, a buffer storage circuit is included such that a continuous signal with sync is output even in the event that a disruption occurs in the sync portion of the signal.

The video signal is separated in the Sync Sep board into sync and data. The CRC of the data is analyzed in the Data Sep board and output to the Dec. A. This data, whose timing relationship equals that of the video signal, is interleaved and sent as a serial bit stream to the S/P converter IC-F3. The converted 8 bit parallel data, latched by IC-F4, is sent to RAM (IC-K6-7, J6-7, H6-7, F6-7). During this time, IC-D6 goes high, which results in the 16th bit of CRC data being sent to RAM going high.

The bit clock is produced by IC-B6 which divides the clock signal from terminal pin 37 and 38 (OM) by 13. The converted carry output, called BIT SYNC, is sent to the Video Out board, where BIT SYNC receives PRT and the phase locked to the video signal. IC-B5 D4 divides the bit clock signal by 25 and sub-divides by 3, by IC-B5. The QA to QD outputs are sent to ROM IC-B3 and latched by IC-A3 to produce clock signals: 16f, S/L, Pfs, WDCK, and APCM. The ROM output of IC-B3 is sent to IC-E2 (BCD Decimal counter) and latched with the bit clock IC-E1. The decoder data is sent to the Dec. B board as each channel and parity data. Finally, parallel data is applied to IC-H1-2, J1-2, K1-2 when Inhibit and LD goes low. The data is converted to serial data when INH goes low.

The CH1 and CH2 data read into Dec. A has no time compression and is 35H wide which corresponds to 1 interleave block. For this purpose, a 35H memory consisting of IC-K6-7, J6-7, H6-7, F6-7 are provided. Write addressing is controlled by counters IC-E4, 5, 8-10 and ROMS IC-E6, 7 which make up a 35H counter. The read address counters consist of IC-C8-10, D9-10. The count sequence repeats every 279 counts.

Clock enable signals output from the W/R address counters are sent to IC-K8-10, J8-10, H8-10, F8-10 to the RAMS (2114). The CH1, 2 or parity data is selected by selectors IC-K3, J3, H3, and F2. The outputs are then supplied to IC-H1-2, J1-2, K1-2, as 16 bit selected parallel data, converted to serial and sent to the Dec B board at the WD CK frequency.

5.4.6 Decoder B Board (Figure 5-21)

In general, audio signals are interleaved and formatted onto video sync with CRC and parity information. The data and sync components are separated by the Sync Sep board and converted into CH1, CH2 data and parity information in parallel mode at the Dec. A. This data is then sent to the Dec. B board in the order of LSB - MSB and no audio data is inserted in the 17th to 25th bits of the 25 bit clock period. If an error was found on the Dec. A, its error syndrome (S21, 22, 23) is sent to the Dec. B inparallel with the data. Depending upon the syndrome information, the Dec. B corrects errors by: correction, average or hold methods, and outputs the corrected signal to the D/A board.

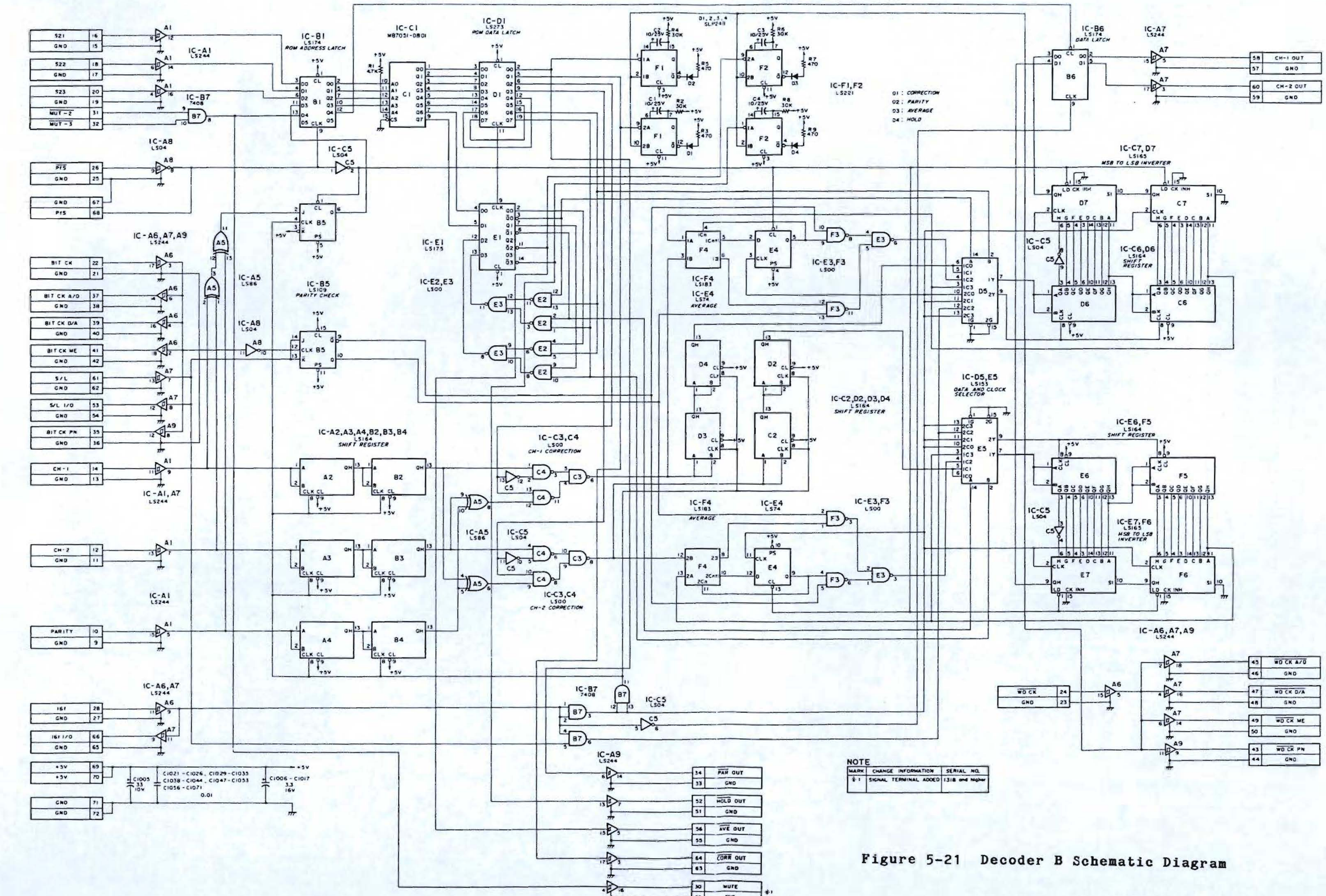
Refer to Figure 5-22 for example of error correction. The 3 column data consisting of L7-9, R8-9 are used. Correction is executed when one of the three data words - say L8 is incorrect. L-8 is corrected by R8 & P because the parity P has been made through an EX. OR between R8 & L8.

When 2 column data or R8 and P are incorrect, average is employed where R8 equals the average value of R7 and R9. When all three values are wrong - R8, L8 and P, HOLD is employed where R8 = R7.

The above analysis is simplified and is used as a model only. True correction of data is handled in blocks for data correction and each block has a set of syndrome information (S21, 22, 22). Each syndrome refers to a specific row. For example: R7, L8, R9 and L7, R8, LO are referred for data correction. When (R7, L8, R9) is in error, S22 goes high. Similarly, when (PPP) is incorrect, S23 goes high. This information (Sn) is supplied to Dec B and synchronized with the re-arranged data.

Referring to the schematic, a parity check (S1) by (EX. OR) operation is carried out for each bit CH1, 2 and parity data by IC-A5 pin 11. If an error occurs in the 16 bit data, IC-B5 pin 6 goes high, S21, S22 S23 are applied to the ROM IC-B1 and based upon the given syndromes, the ROM selects either the correction, average or hold modes. Correction is applied between (11.7H to 23.3H (36 to 70 blocks) and HOLD to errors above 23.3H.

DECODER B BOARD



NOTE

MARK	CHANGE INFORMATION	SERIAL NO.
①-1	SIGNAL TERMINAL ADDED	131B and higher

Figure 5-21 Decoder B Schematic Diagram

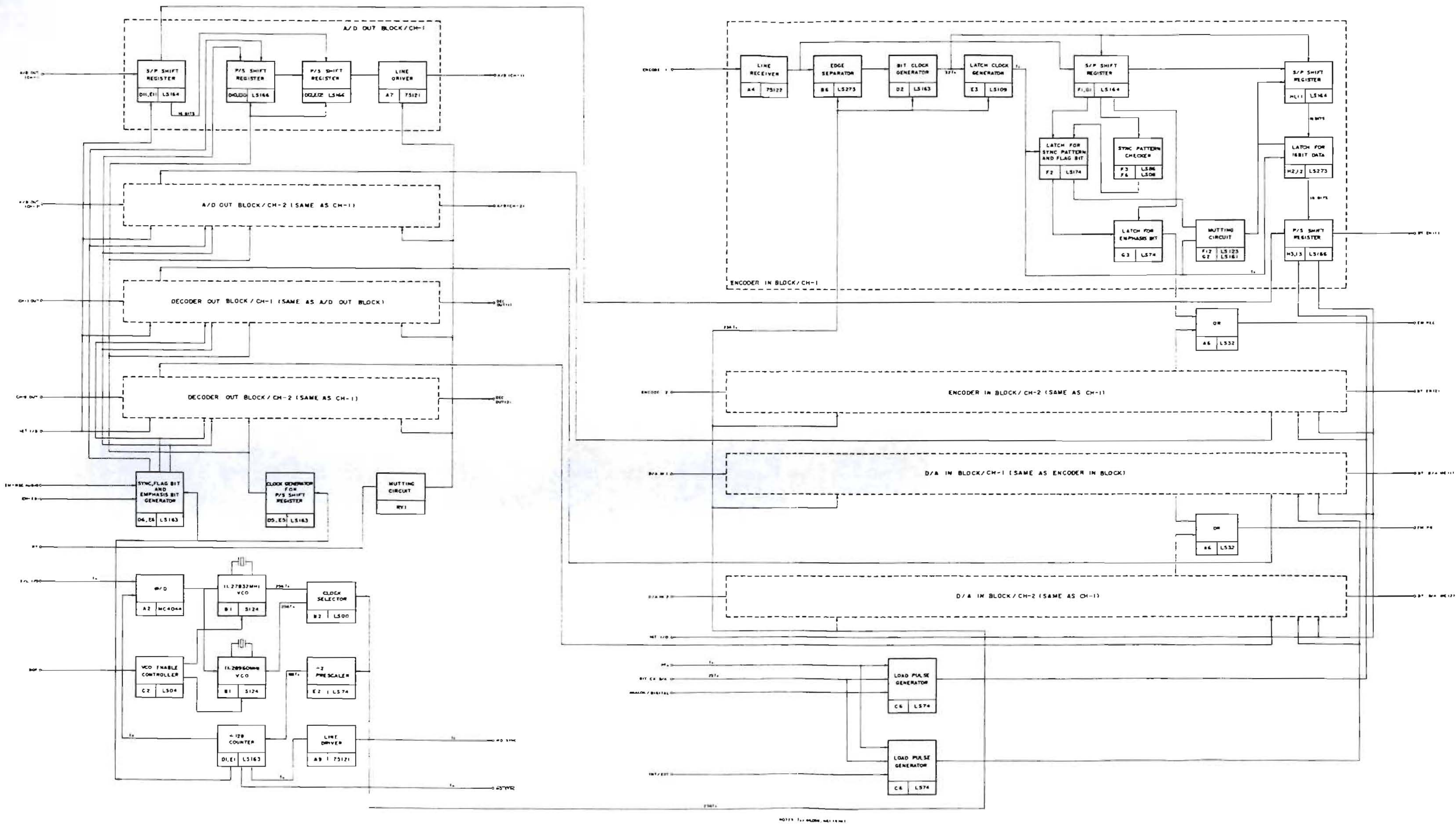


Figure 5-24 Digital I/O Block Diagram

DIGITAL I/C BOARD BLOCK DIAGRAM

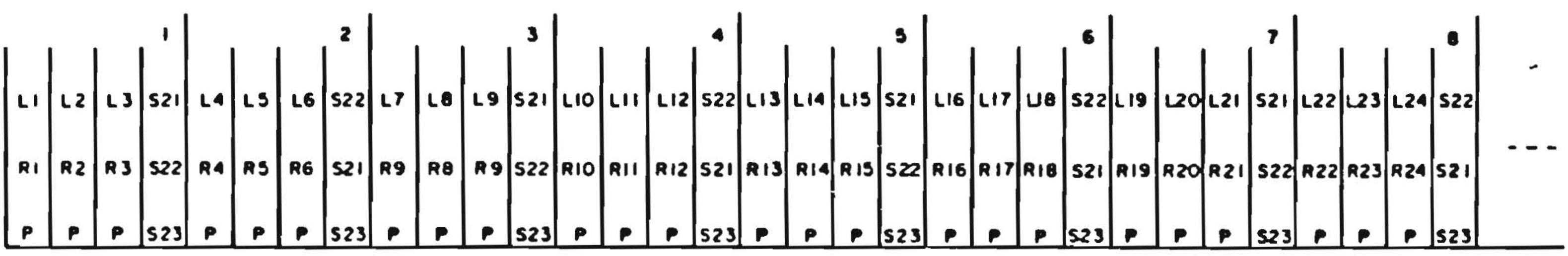
5.4.6.1 Error Correction

If an error occurs in CH-1 and correction mode is applied, Q2 (pin 6) of IC-D1 goes high. This results in IC-C4 pin 13 going high. The corrected data, which is given through an EX. OR between CH-2 and parity data, is sent from IC-A5 pin 8 to the next shift register. IC-D1 pin 9 (Q3) goes high when the CH-2 data is found in error and the corrected data is sent from the EX. OR gate IC-A5 pin 6.

5.4.6.2 Average and Hold Error

If the data is to be averaged, the data from QH pin 13 of IC-C6 is sent to IC-F4 pin 1 (Dual adders). Subsequent data is applied to 1B pin 3 of IC-F4. The E output pin 6, determined by the carry data CN (pin 4), is sent out along with the previous carry data and synchronized with the average clock S/L to pin 4 of IC-D5 (4-1 line multiplexor). The averaged data is sent out when A (pin 14) is low and B (pin 2) is high. IC-D7, C7 and E6, F5 inverts the data stream and is latched to shift registers IC-D6, C6 and E7, F6 for CH-1 and 2 data respectively. The output (parallel) is fed to IC-B6 data latch and buffered by IC-A7 and sent to the D/A board.

For the HOLD Mode, referring only to CH-1, data is sent from IC-D5 pin 7 to the shift registers of IC-D6, C6. Output data from QH (pin 13) of IC-C6 is sent back to C3 (pin 3) of IC-D5. When A (pin 14) and (B) pin 2 are high on selector IC-D5, HOLD data is sent out.



S21, S22, S23 } = Syndrome

Figure 5-22 Syndromes in the Data Stream

Figure 5-23 shows the ROM decision table. Referring to the schematic in Figure 5-21, the addresses for the ROM (MB7051) are supplied by the Syndrome inputs S21, S22, S23 and the Parity check S1. A4 (in Figure 5-23) is the result of an AND function applied to the MUT-2 and MUT-3 inputs.

		S_1	S_{23}	S_{22}	S_{21}	A: CH2	A: CH1	B: CH2	B: CH1	CH2C	CH1C	CORR	PARI
	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	1	0	0	0	0	1	1					1	1
1	1				1	1	1				1		1
2	1			1		1	1			1			1
3	1			1	1			1	1			1	1
4	1		1			1	1					1	1
5	1		1		1	1			1			1	1
6	1		1	1			1	1				1	1
7	1		1	1	1			1	1			1	1
8	1	1						1	1			1	
9	1	1			1	1	1				1		1
A	1	1		1		1	1			1			1
B	1	1		1	1			1	1			1	1
C	1	1	1			1	1					1	1
D	1	1	1		1	1			1			1	1
E	1	1	1	1			1	1				1	1
F	1	1	1	1	1			1	1			1	1
		PARITY CHECK	(1) = NG			(1) = OK		(0) = OK		(1) CORR		FOR LED (0) LIGHT	

Figure 5-23 ROM Decision Chart

5.5 DIGITAL I/O BOARD

The Digital I/O board is employed to interface the **PCM-1610** to other digital audio devices in an all digital system. The input section has two ENCODER inputs (CH-1, CH-2) and two D/A inputs. The output section has two DECODER outputs and two A/D outputs. (Refer to Figure 5-24).

Figure 5-25 illustrates the digital I/O data format with relation to the WORK CLOCK. Also the Block Configuration of the data, and Control Signal Block structure.

5.5.1 Digital Input Circuitry

The digital input section contains the circuits for:

- WORD SYNC extraction
- CONTROL BIT extraction
- PCM DATA extraction
- MUTING circuit

Refer to Figure 5-26 for Digital Input Circuitry (this schematic can be found in the Operation and Maintenance Manual pages 5A-43 and 5A-44).

DIGITAL I/O BOARD BLOCK DIAGRAM

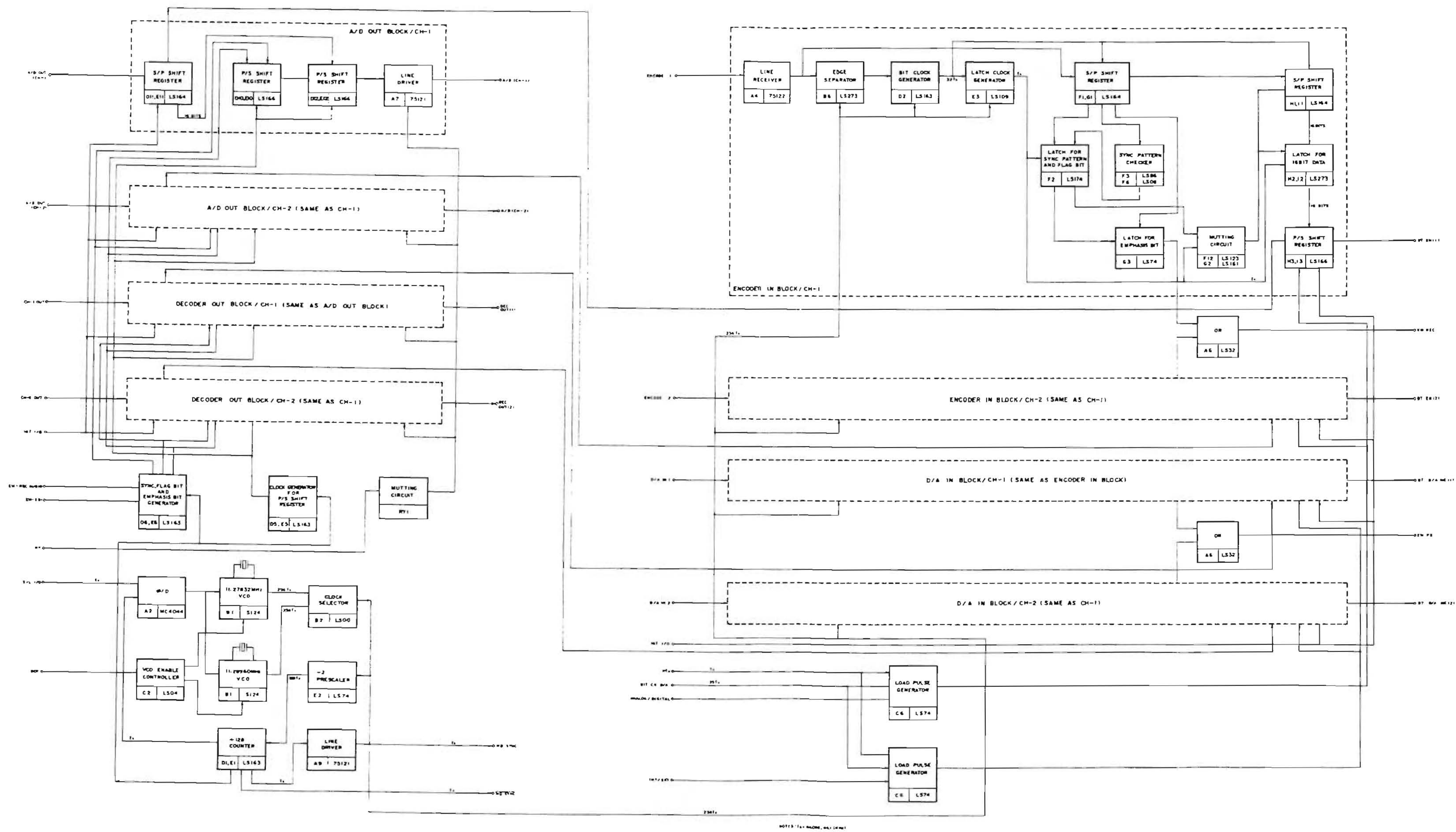
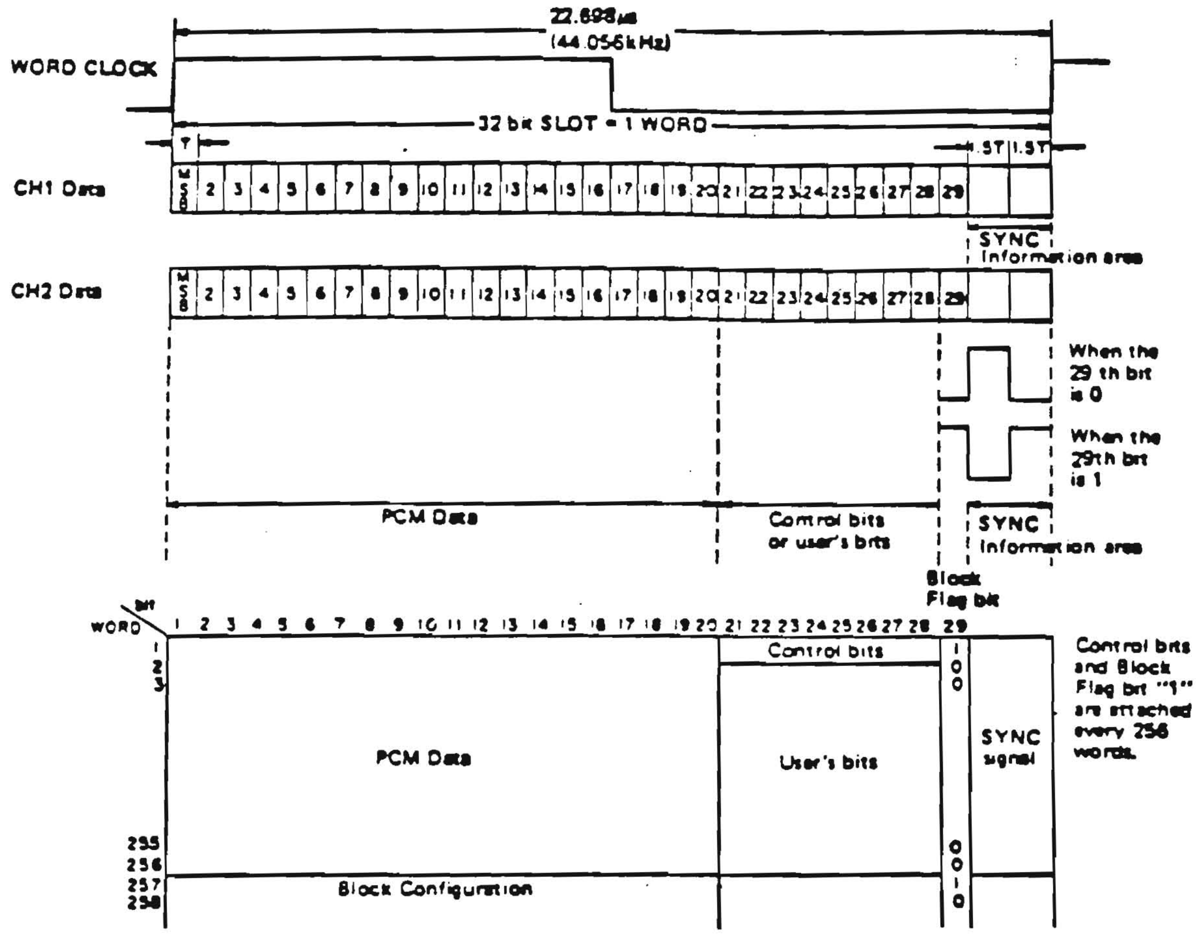
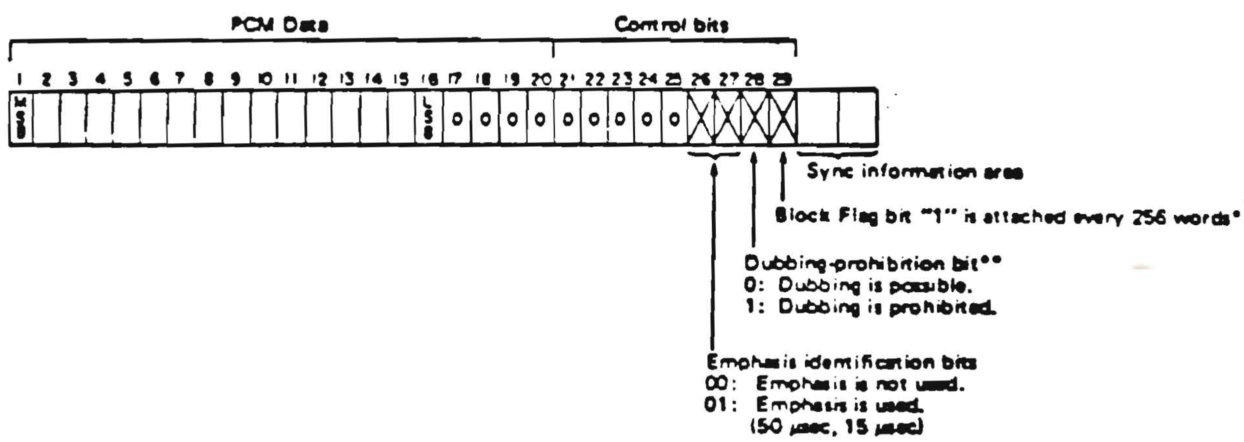


Figure 5-24 Digital I/O Block Diagram

Digital input/output format



Control signal block structure



* When Block Flag bit is "0", Dubbing-prohibition bits and Emphasis identification bits are also "0".

** In the case of PCM-1610, Dubbing-prohibition bit is always "0".

Figure 5-25 Digital I/O Format

5.5.2 WORD SYNC Extractor

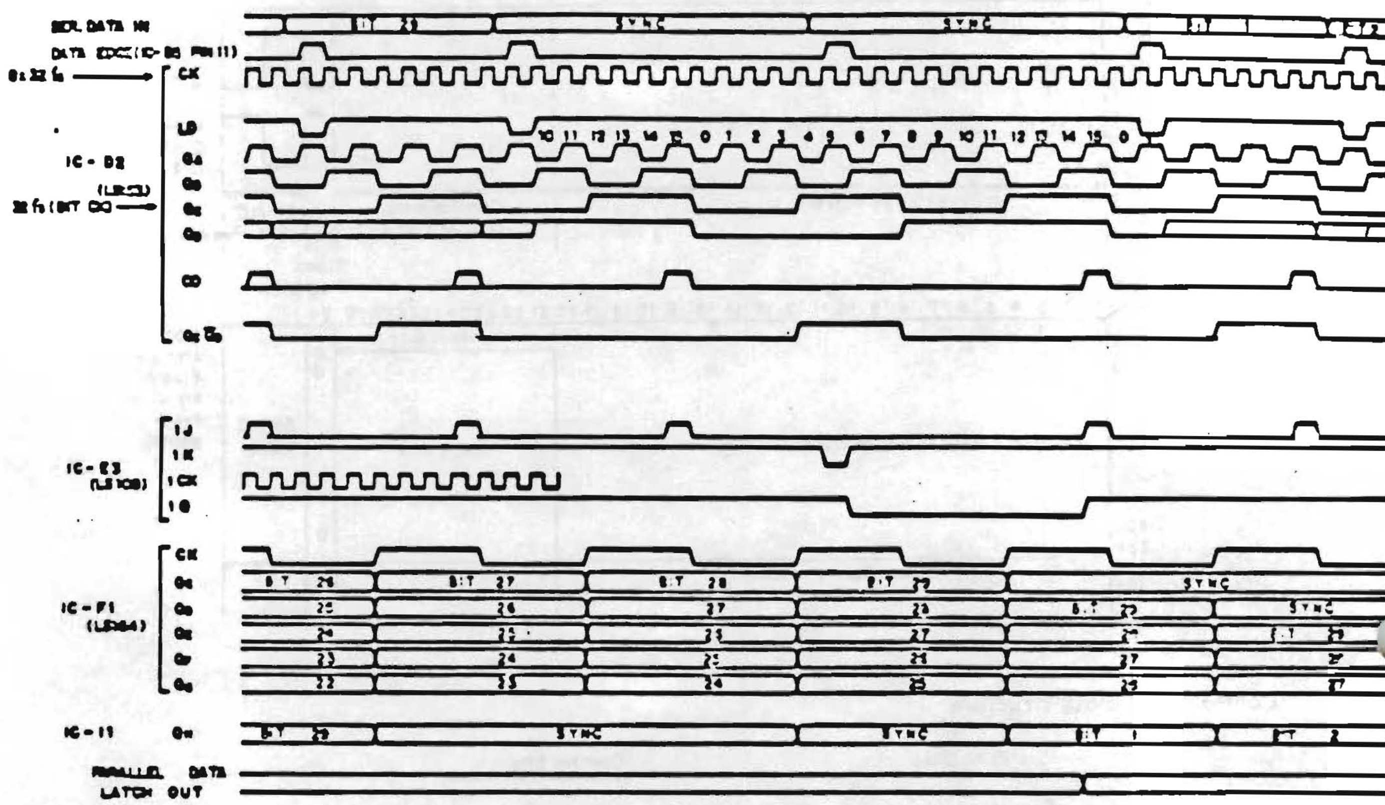


Figure 5-26 Word Sync Timing Chart

Serial data is input to ENCODER 1, and terminated by a 75-ohm resistor (switchable). The data is buffered by IC-A4 Line Driver, routed to IC-B6, and latched twice by High Rate Clock. At 1Q and 2Q, two data having different phases are output. Exclusive OR operation for this data is performed to obtain edge pulses between the respective data. From these edge pulses, only WORD SYNC edge pulses during 1.5T is extract by the high Rate Clock counter IC-D2 and the Logic Matrix Circuit comprising IC-C4, D3 and C3. The extracted edge pulses are used to make the data latch clock IC-E3 IQ with a JK flip-flop of IC-E3.

5.5.3 CONTROL BIT Extractor

Serial data from IC-A4 Line Driver goes into IC-F1 S/P Shift Register, and is shifted in turn to G1 to H1 to I1 according to the Qc output Bit Clock 32 fs of High Rate Clock Counter IC-D2.

When a latch pulse of E3 1Q goes up (at the leading edge) "27", "28", "29", "SYNC", "SYNC", and "SYNC" of serial data are output at Qf, Qe, Qd, Qc, Qb and Qa of IC-F1 respectively. Thus, when Qd output is high (i.e. the flag bit is "1"), the latch out 2Q of IC-F2 changes from low to high. This leading edge latches the D input (27) of IC-G3. So, by referring to the Q output, it is possible to know whether or not there is EMPHASIS Information. This Q output is transmitted through IC-A6 to the ENCODER circuit. When the Q output is high, information to say there is the EMPHASIS is added to the PCM signals.

5.5.4 PCM DATA Extractor (Figures 5-26 and 5-27)

Serial data from Qh of IC-G1 is shifted further to IC-H1 and then to IC-I1.

When a latch clock pulse (E31Q) of IC-H2 and I2 goes up (at the leading edge), the data MSB to 8th bit are latched at the IC-I1 outputs to Qh to Qa, and the data 9th to 16th bits are latched at the IC-H1 outputs Qh to Qa until the next leading edge of the latch clock. Then, they are sent to P/S Shift Register of IC-H3 and I3. By adding the S/L and CK pulses made from the internal clock pulse to the P.S Shift Register to load and shift the data, serial data in accordance with the internal data format is sent out in turn from Qh of IC-I3 to the ENCODER circuit. (DTEN(1)).

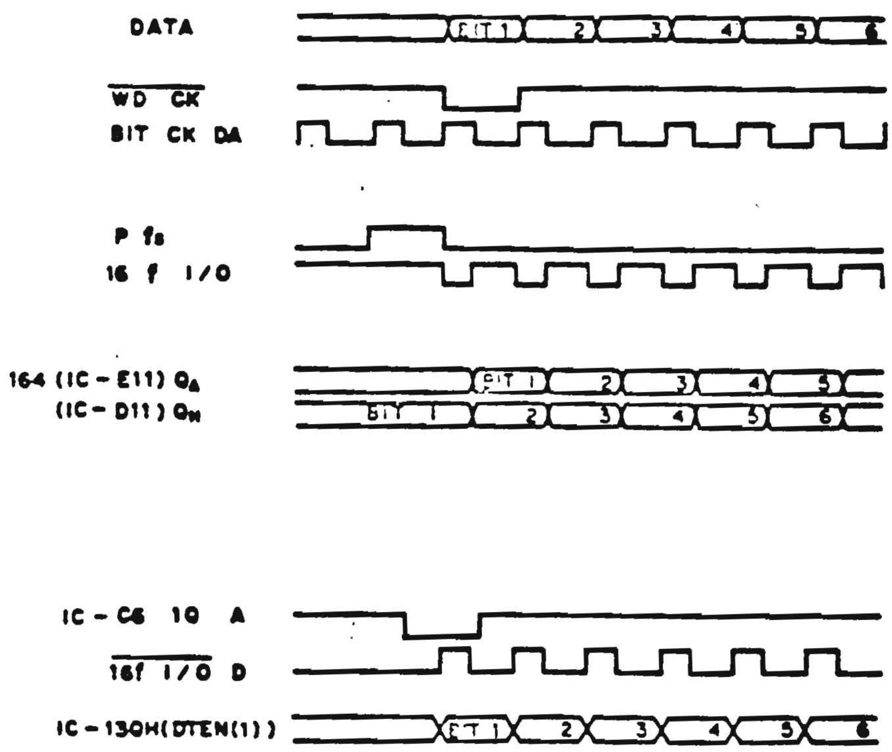


Figure 5-27 Clock/Data Timing Diagram

At this time, the S/L pulse of IC-H3 and I3 is made from pfs latched by BITCKDA at IC-C6, and 16f is used as the clock pulse. The signals, ANALOG/DIGITAL abnd INT/EXT, which are input to the PS terminal of IC-C6, are the input select signals of the ENCODER input and the D/A input respectively. When the signal is ANALOG and INT, the PS terminal output is low, and the Q output of IC-C6 is high. Therefore, the parallel input to IC-H3, I3, H9 and I9 is not loaded, but SIN (A/D OUT CH-1, CH-1 OUT) is input, shifted and output.

5.5.4.1 MUTING Circuit

The muting circuit clears and mutes the S/P Shift Register and the latch of the last stage either when the SYNC pattern of input serial data is different from the format or when no serial data is input anymore.

As described above, the outputs Qd, Qc and Qa of IC-F1 are "29", "SYNC", and "SYNC". When the SYNC pattern of input serial data is the correct format, as seen from the SYNC pattern Fig. 1, Qd, Qc, and Qa are either "low", "high" and "low" or "high", "low" and "high". Consequently, the AND IC-F6 output of the Exclusive OR IC-F3 output for Qd and Qc and the Exclusive OR IC-E3 for Qc and Qa is necessarily high.

When the SYNC pattern is different from the format for some reason, the AND IC-F6 output goes low, and also, the IC-F2 latch output 1Q, and the G2 CL terminal, and the CRY OUT CO all go low. Therefore, the respective CL terminals of IC-H1, I1, H2 and I2 all go low, and the S/P Shift Register and the latch are cleared and muted.

When the SYNC pattern becomes normal, the CRY of the counter IC-G2 becomes "high" at the 15th pulse counted from the latch pulse (IC-E3 1Q) of the normal IC-F6 output signal high. At the same time, the counting stops, the CRY stays high, and the muting is released.

When no serial data is input anymore, the mono multivibrator Q of the IC-F12 changes from high to low to clear IC-F2. Consequently, the 1Q output becomes low and muting is performed as described above. (The muting is released in the same way as described above.) At this time, the CL terminal of IC-G3 also goes low; thus the EMPHASIS information reference signal (IC-G3 Q) goes low as well.

D1
5-47

DIGITAL I/O BOARD

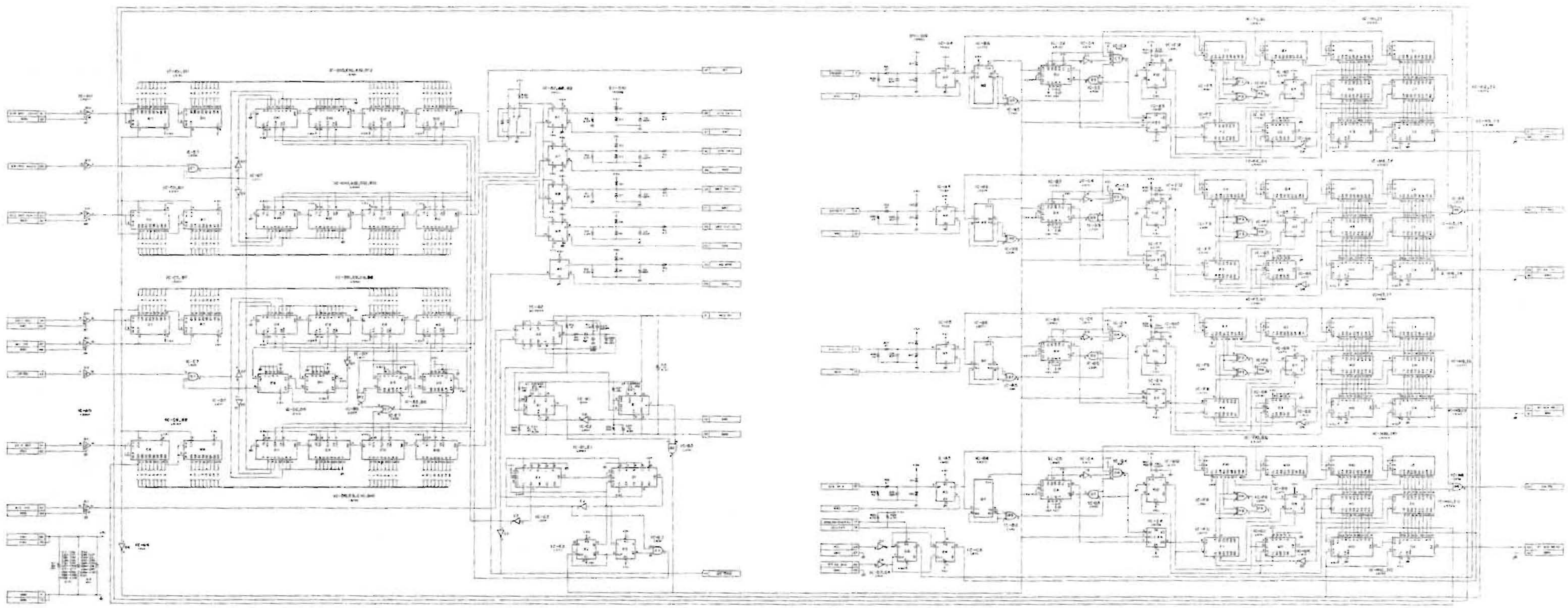


Figure 5-28 Digital I/O Schematic Diagram

Figure 5-29 Digital I/O Schematic Diagram

5.5.5 **Digital Output Circuitry** (Figures 5-28 and 5-29)

The Digital Output section is comprised of the following circuits:

- SERIAL/PARALLEL converter
- CONTROL/FLAG BIT generator
- SHIFT CLOCK generator
- PARALLEL/SERIAL converter
- WORD CLOCK generator
- MUTING circuit

(The schematics in Figures 5-28 and 5-29 can be found on pages 5A-41 and 5A-42 of the Operation and Maintenance Manual.)

5.5.6 **Serial/Parallel Converter** (Figure 5-30)

Serial data (CH1) sent from A/D OUT Is input first to the S/P Shift Register of IC-E11 and D11 to be converted into digital I/O format, and then converted to parallel data. That is, serial data is shifted in turn from MSB according to 16fI/OCK, and when MSB is output to IC-D11 Qh (16SB is output to IC-E11 Qa), the data is held until the next 16fI/OCK leading pulse arrives. While being held, the data is loaded to the next P/S Shift Register.

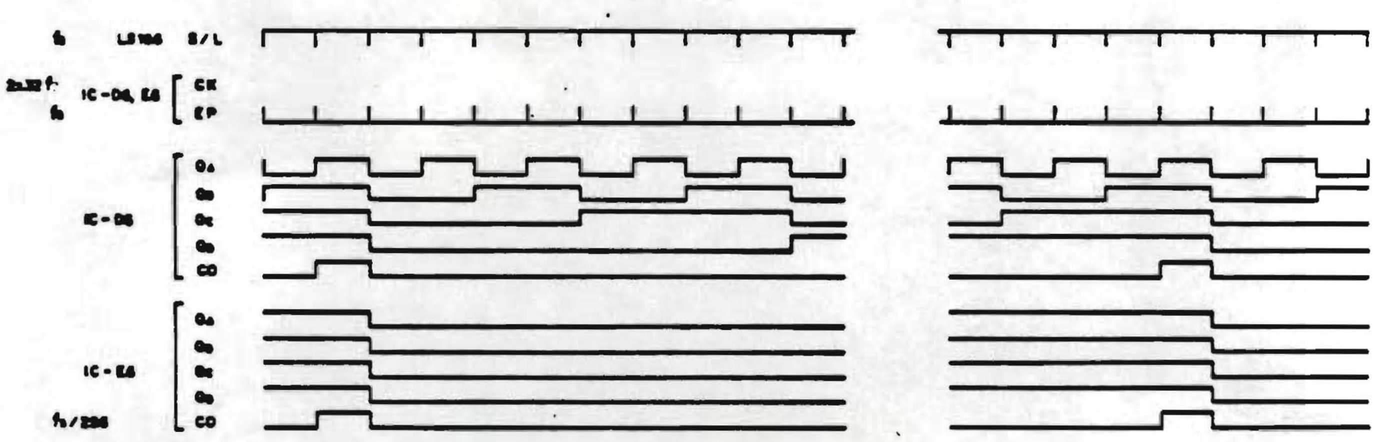


Figure 5-30 S/P Timing Diagram

5.5.7 **Control/Flag Bit Generator** (Figure 5-30)

The digital I/O format prescribes that the 29th flag bit is set at "1' every 256 words to insert the control bit information into 21SB to 28SB. In **PCM-1610**, 26SB and 27SB are used as EMPHASIS reference bits.

IC-D6 and E6 are counters to count pulses to be input to the EP terminal up to 256, and the CRY OUT of IC-E6 goes high every 256 EP pulses. The EP pulses are made by inverting the pulses which are used in item A to load parallel data to the P/S Shift Register in words. Thus CRY OUT of IC-E6 goes high every 256 words. This pulse is sent to IC-D10 D as the flag bit information, and to IC-D10 C as the SYNC pattern information. In addition, this pulse is used as a gate pulse to send EM-REC AUDIO i.e. EMPHASIS ON/OFF information at recording, to IC-D10F.

5.5.8 **CK INHIBIT Pulse Generator** (Figure 5-31)

This pulse generator produces, using the counter composed of IC-E5, D5, B2 and E7, the CK INHIBIT pulse for the 32-bit shift register composed of IC-D10, E10, E12 and D12 in the parallel digital block.

To make the LD pulse of E5 and D5, NAND is performed between the IC-D5 CRY OUT and the IC-E5 CRY OUT, and then AND is performed between NAND output (IC-B2 pin 6) and the IC-E7 pin 11 output which is made in Muting Circuit block. This AND Output (IC-E7 pin 8) is used as the LD pulse.

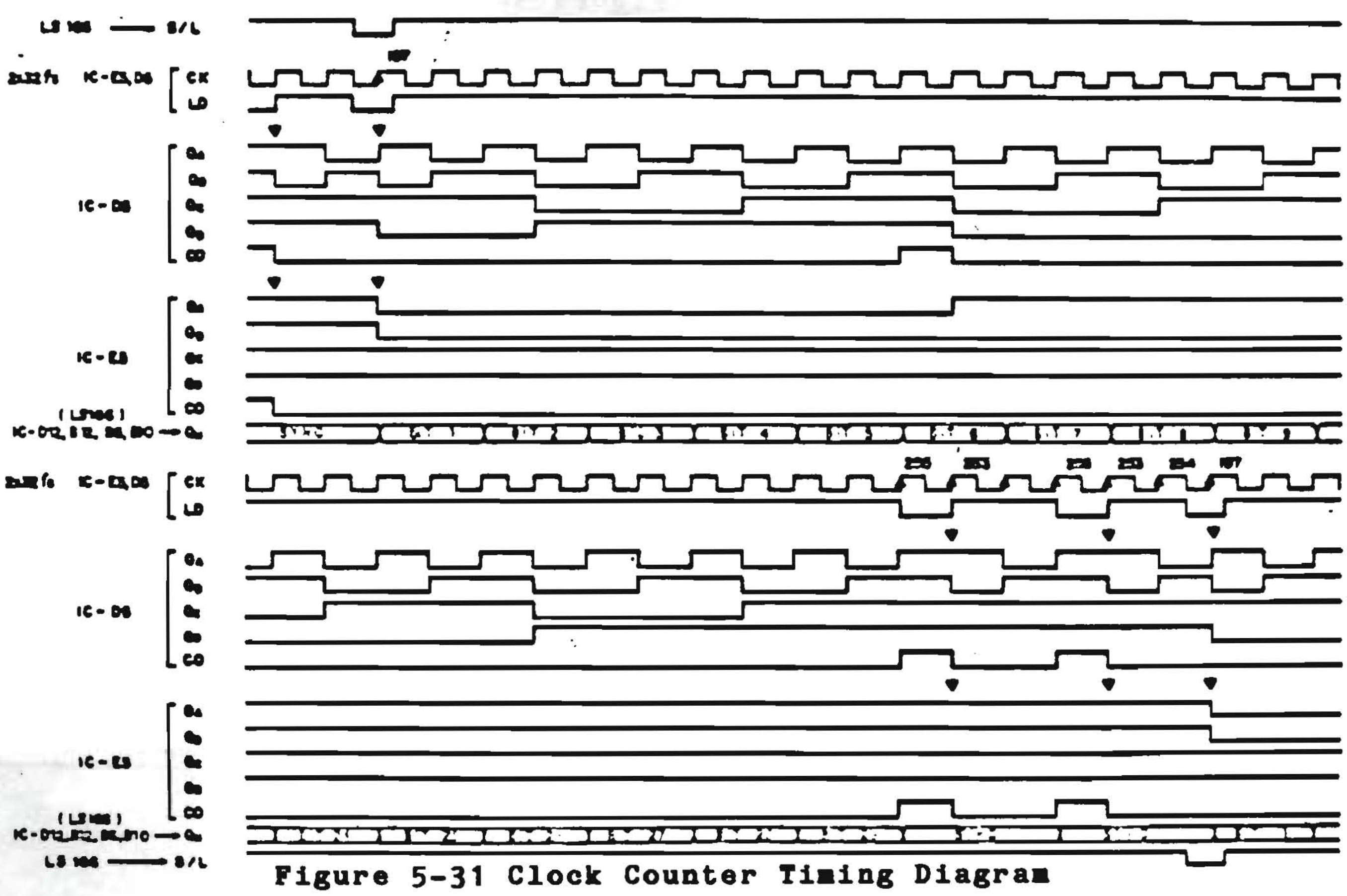


Figure 5-31 Clock Counter Timing Diagram

When IC-E7 pin 11 output is low and the LD pulse is generated, "0101" and "1100" are loaded respectively into IC-D5 (Qd, Qc, Qb, and Qa) and IC-E5 (Qd, Qc, Qb, and Qa) by the first CK (2X32fs) leading edge, and the counter starts counting from 197. When the CRY OUT of IC-D5 and E5 goes high and the NAND output (IC-B2 pin 6) goes low on the 255th CK leading edge, the LD pulse is generated. On the next CK leading edge, "1101" and "1111" are loaded respectively to IC-D5 and IC-E5, and the counter starts counting from 253. On the coming 2nd CK Leading edge, the counter becomes 255, and the LD Pulse is also generated, but by the next CK, the counter becomes 253 again. The counter advances further to 253, 254 and 255. When the counter become 255th CK's leading edge, the LD Pulse is generated this time by IC-E7 pin 11 output, and "197" is loaded to reset the counter.

Now, taking the 197th leading edge as a reference point, Qa of IC-D5, the reference pulse to the 29th pulse all have the same pulse width (T). The 30th and the 31st pulses, however, have a different pulse width (1.5T) and the 32nd and following pulses have the same pulse width (T) as before.

This Qa output is used as the CK INHIBIT pulse, 2 X 32 fs is as CK, and the LD Pulse as the IC-E7 pin 11 output. The said 32 bit P/S shift register is operated by these pulses as if it is operated by CK INHIBIT CK,. so that the data shifted out by the 30th and the 31st leading edges has a width of 1.5T (A SYNC pattern having a width of 3T can be obtained.)

5.5.9 **Parallel/Serial Convertor** (Figure 5-32)

This block consists of four P/S shift registers (IC-D12, E12, E10, and D10). The parallel data from MSB to 16SB from A is loaded from IC-D12 H to IC-E12 A. The control bit information, the flag bit information, the SYNC pattern information and the EMPHASIS information are loaded respectively to F, D, C and B of IC-D10. These data are shifted in turn according to the CK INHIBIT CK generated in C, and sent out in digital I/O format form from the serial out Qh of IC-D12.

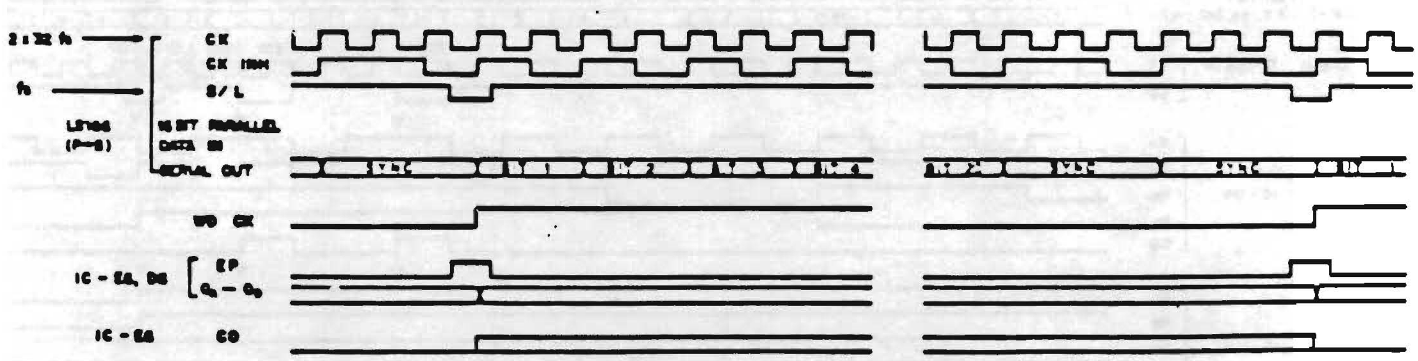


Figure 5-32 P/S Timing Chart

5.5.10 WORD CLOCK and 256 Fs Generator (Figure 5-33)

First master clock of 256 fs is made using the PLL circuit. With this clock as reference, the external work CK and 2 x 32 fs and fs are made. (fs = 44.056kHz or 44.1kHz)

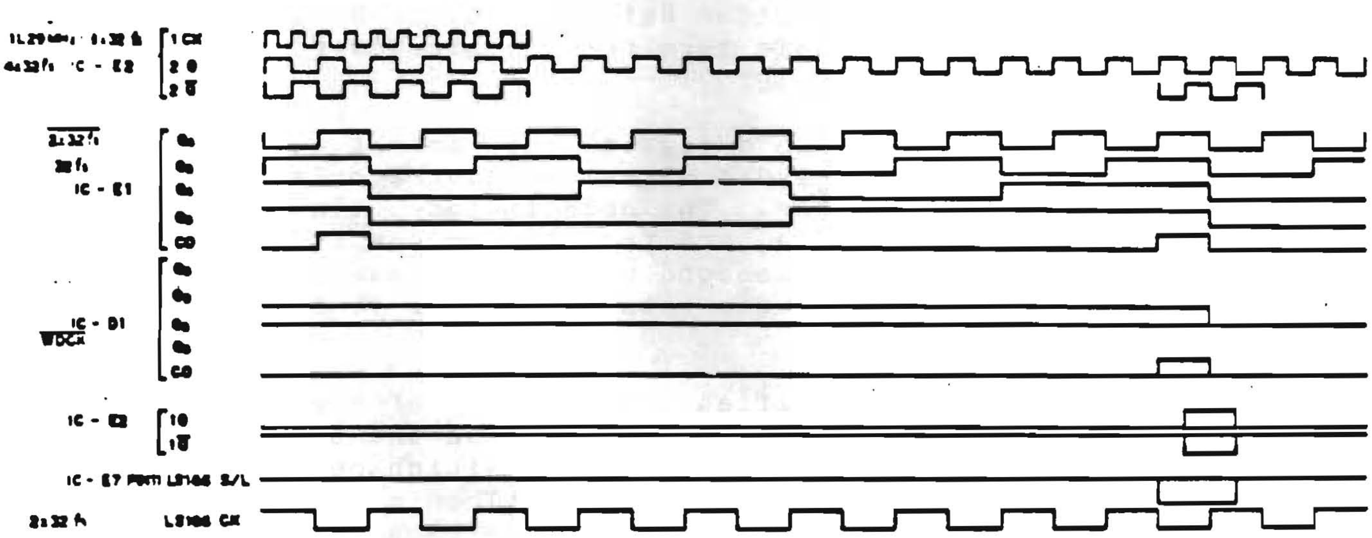


Figure 5-33 Fs and Word Clock Timing Diagram

5.5.11 Muting Circuit

When the power supply is turned on/off, the relay is controlled by the RY signal, and the line driver output of each digital output is made "0" for muting operation.

5.6 TIME CODE Board

This board generates the SMPTE time code, which can be recorded simultaneously with the PCM recording. The longitudinal format time code is recorded on the Audio CH-2 Track of the video recorder. By recording this code simultaneously the PCM recording is ready for editing by the **DAE-1100.**

5.6.1 SMPTE Format

The Society of Motion Picture and Television Engineers (SMPTE) has specified the "American National Standard Time and control code for video and audio tape for 525 line/60 field television systems" (ANSI C98.12-1975).

This standard specifies a digital code format and modulation method for video and audio magnetic tape recorders to be used for timing control purposes. The code includes time information of hours, minutes, seconds, and frames. In the SMPTE format, there are 30 frames for each second which resolves to a frame rate of 30Hz in the non-drop frame rate to conform to the color rate of 29.97Hz.

The standard also specified the location of the code on the tape and its relationship to other signals on the tape. The modulation method is such that a transition occurs at the beginning of every bit period (self-clocking bi-phase code). "One" is represented by a second transition one half of a bit period from the start of the bit. "Zero" is represented when there is no transition within the bit period. Fig. 5-30 shows a typical waveform. Each frame is identified by a unique address (80 bits). The tenth bit is the drop frame flag. It is "1" if certain numbers are dropped to resolve the difference between real time (60 fields/sec) and colour time (59.94 fields/sec).

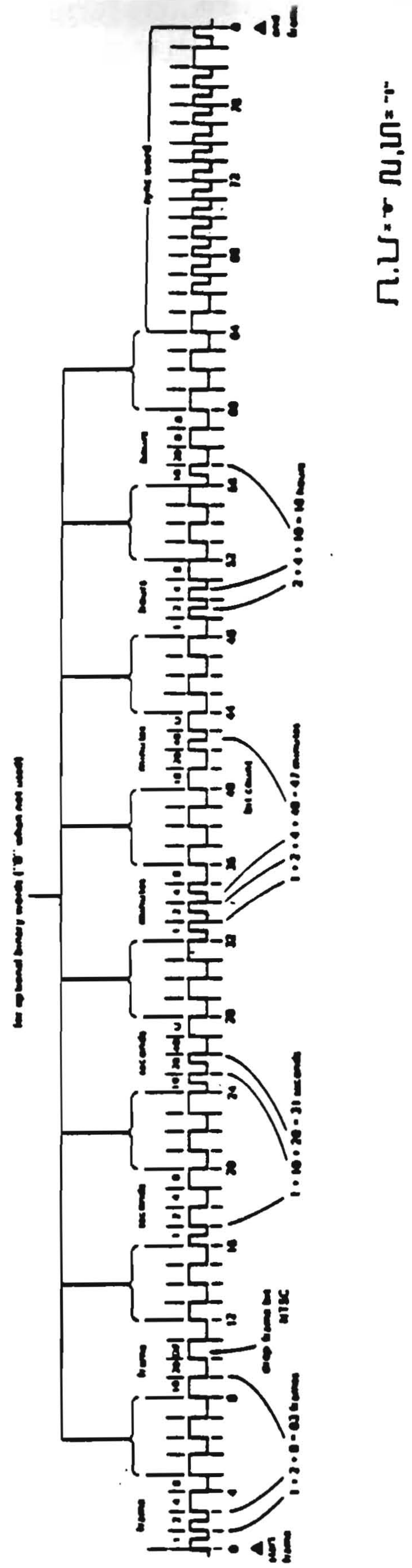


Figure 5-34 Longitudinal Time Code Signal

5.6.2 Block Diagram

The counter uses the frame pulses derived from the video signal to generate the time code. A preset ON/OFF switch makes it possible to preset a certain time code (from 00 hours 00 minutes to 23 hours 59 minutes). The presetting is done by 4 rotary switches on the board. A RUN/RESET switch on the front panel starts the time code generation. Fig. 5-35 gives the block diagram of the board. The time code is available via a XLR connector (balanced output) or via a BNC connector (unbalanced output).

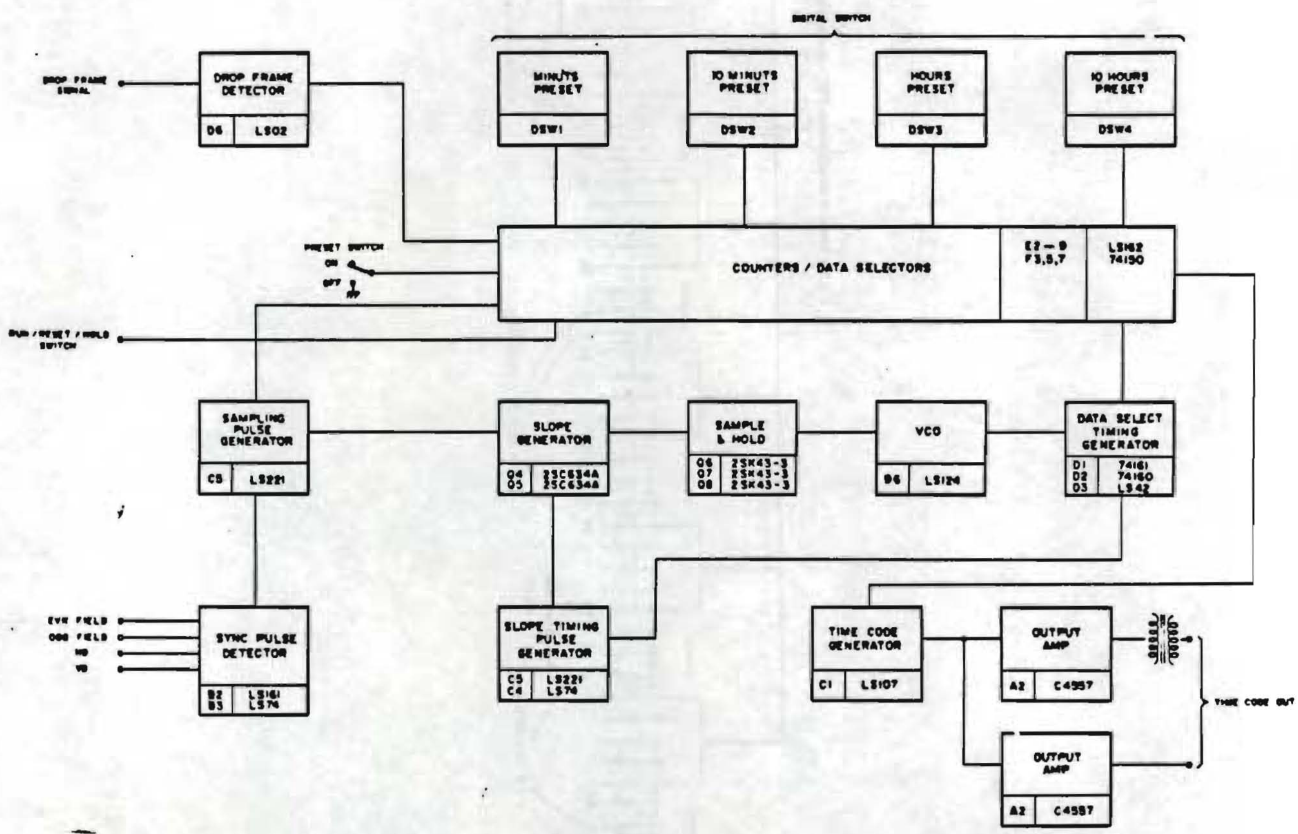


Figure 5-35 Time Code Board Block Diagram

5.6.3 SYNC Pulse Detector
(IC-B4, B3, and B2)

IC-B3 (LS74) gets the first and second field pulses and sends a window clock out from pin 5 (HD).

IC-B2 (74LS161) produces a frame pulse (at IC-B2 pin 12) by this pulse as a window and the IC-B4 pin 8 output (HD). As is clear from the composite sync out in Picture 2, the frame pulse starts rising at the 5th H counting from the leading edge of IC-B2 pin 1 (VD), and is used as a start point for the time code.

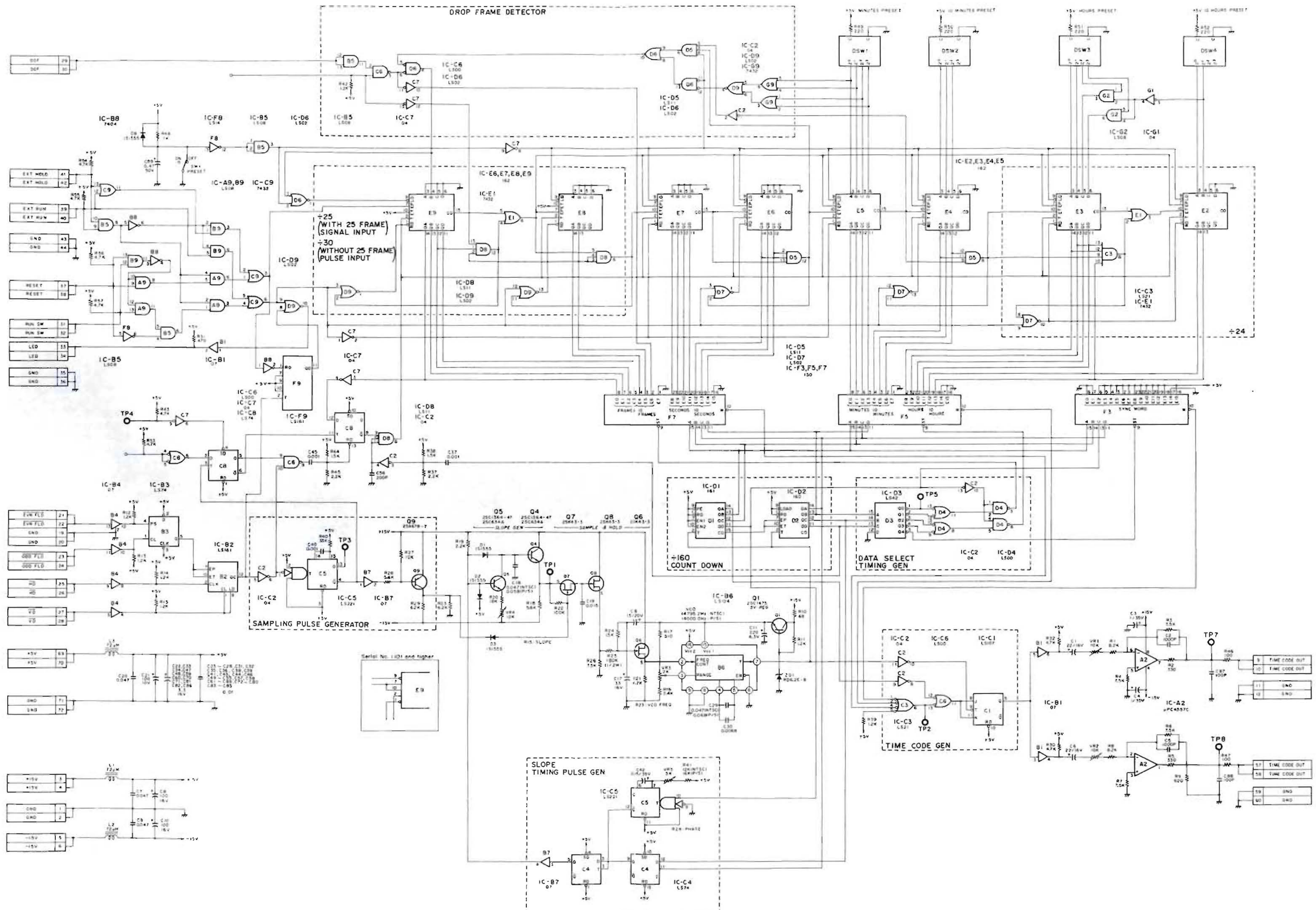
5.6.4 PLL Circuit
(IC-C2, C5, B7, B6, D1, D2, C4, B7, Q1, and Q4 thru Q9)

The phase locked loop (PLL) circuit produces a clock to derive the SMPTE time code from the frame pulse. The clock, the phase of which is locked with the frame pulse, is sent to the TIME CODE GENERATOR. The clock has 160 times the frequency of the frame pulse.

First VCO oscillates approximately 160 times the frequency of the frame pulse. This frequency is divided by a 1/160 frequency divider into a frequency close to the frame frequency, and then the waveform is converted to a trapezoidal waveform. The side slope of this waveform is sampled by a pulse made by the SYNC pulse generator so that the VCO frequency can be fixed at 160 times the frame frequency. Furthermore, the phase of VCO is controlled by a monostable multiplier to obtain the prescribed phase.

IC-B6 (74LS124) is an oscillator generating 160 times the frequency of the frame pulse. The oscillation frequency is adjusted at about 4795.2Hz by VR3 when Fs is 44.056kHz. IC-D1 (74LS161) and IC-D2 (74LS160) divide the oscillation frequency of IC-B6 by 1/160. IC-C5 (74LS221 pin 9 input) and IC-C4 determine the phase used to make the trapezoidal waveform. The phase is adjusted by VR5. C18, R20, VR4, Q5 and D2 are used to make a side slope of the trapezoidal waveform. The slope is adjusted by VR4. IC-C5 (74LS221 pin 1 input) makes a sampling pulse (about 20us) from the frame pulse. Q7 performs the sampling. C19 holds the sampling voltage. R25, R24 and C17 are used to decrease the stationary deviation. The sampling voltage is applied through the Q6 source to the VCO input to operate the oscillator.

TIME CODE BOARD



Note: CLEAR (CL) is synchronized with CLOCK
LOAD (LD) is synchronized with CLOCK

CLEAR of SN74162 is a synchronous decimal counter, and self-running as a 1/10 divider.

(2) 1/5, (1/3, 1/6) divider

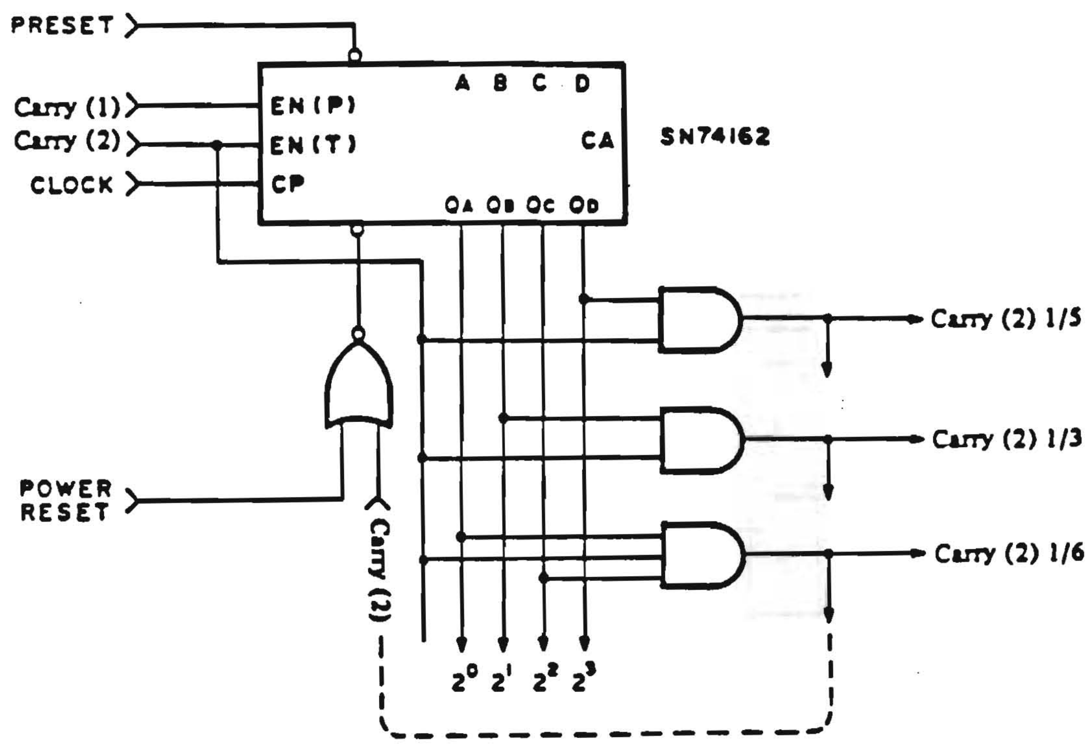


Figure 5-38 74LS162 Configured as a Divider

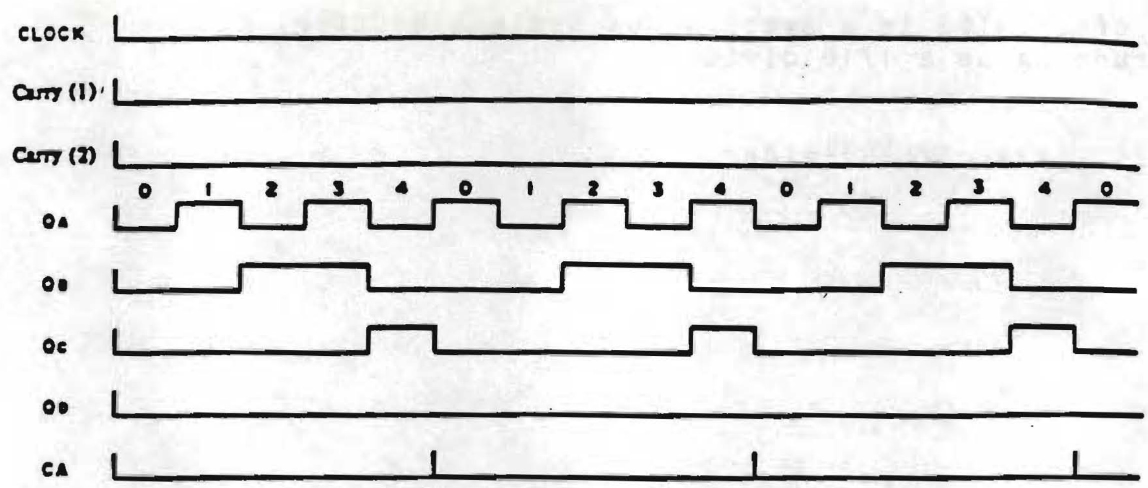


Figure 5-39 74LS162 Timing Diagram

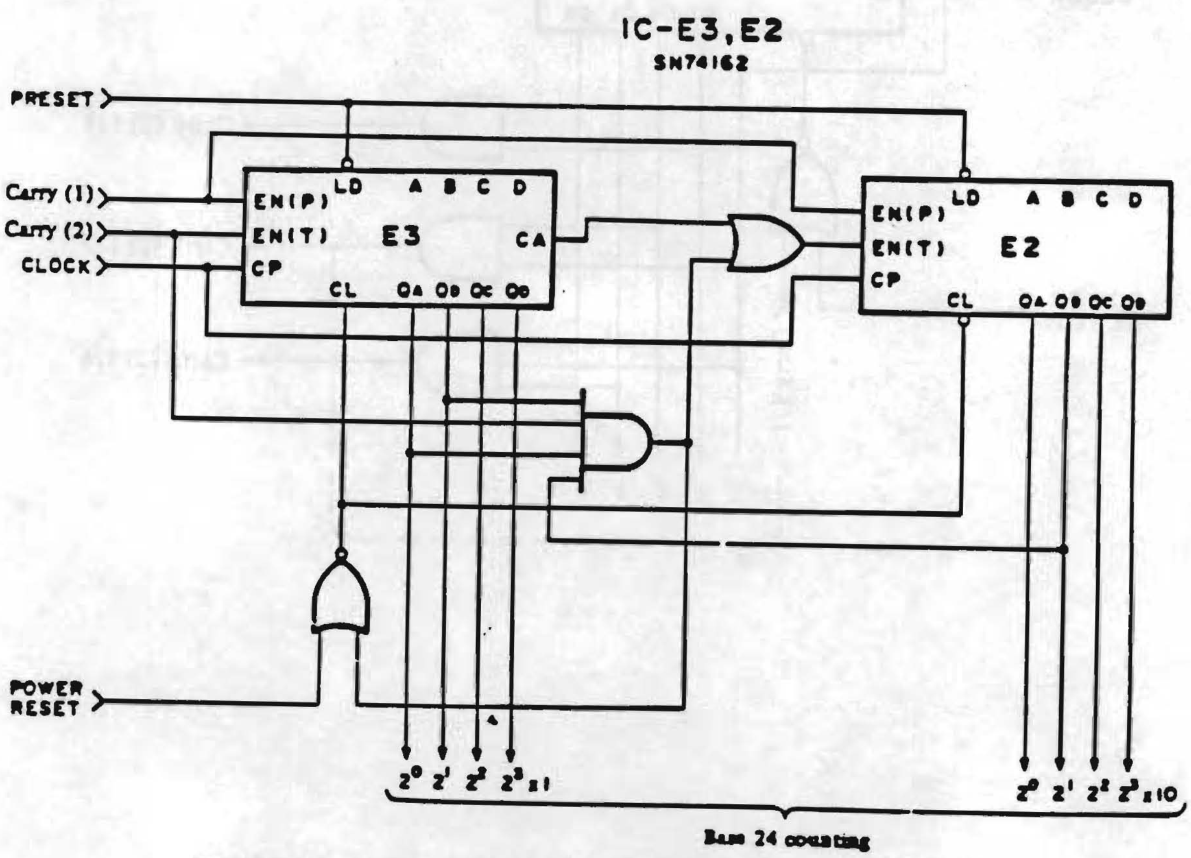
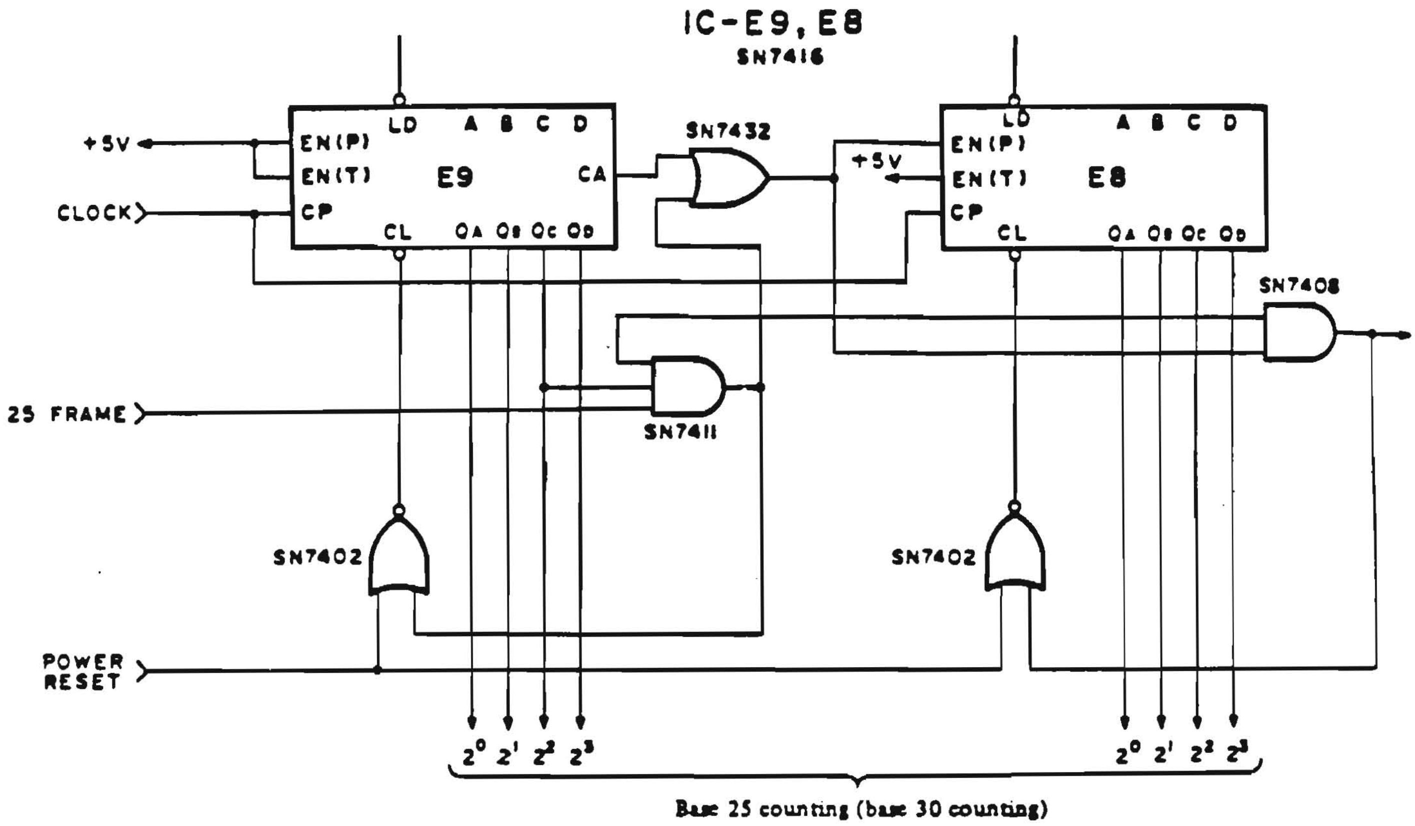


Figure 5-40 74LS162 Divide By 24 Arragement



When the 25 frame signal is applied, IC-E9 and E8 form a base 30 counter. When not applied, they form a base 25 counter.

IC-E8 works as a ternary counter.

Figure 5-41 74LS162 Divide By 25 or 30

5.6.5 Data Selector
(IC-F7, F5, and F3)

An 74LS150 is employed. The data selector selects the frames data, the seconds data, the minutes data, and the hours data according to the clock pulse made by the data select timing generator and sends the appropriate data to the time code generator. See Figure 5-42 for the logic array used for the drop frame generation.

5.6.6 Drop Frame Detector

Fig. 5-43 shows the relationship between the color time and drop frame.

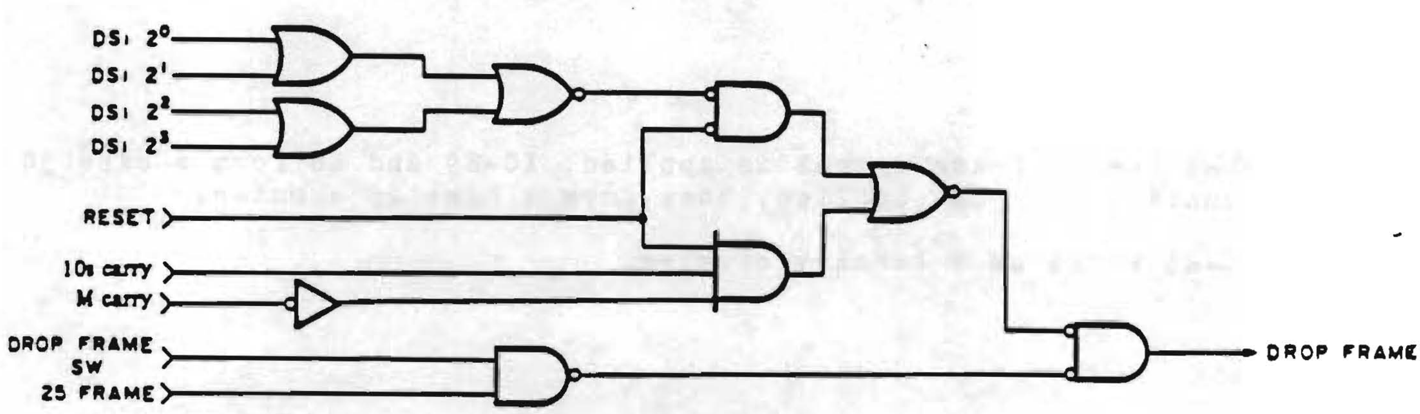


Figure 5-42 Drop Frame Generator

When the minute digit is not "0" in the preset mode, the drop frame signal is sent out.

In the non-preset mode, when there is carrying-up in the 10-second digit but not in the minute digit, the drop frame signal for the next count is sent out. The circuit is designed so that the drop frame signal can be applied to the frame digit in the preset mode. IC-E9 pin 4 is used for this input. No drop frame signal is sent out while counting is being performed at the 25th frame.

It is possible to stop the drop frame operation by way of the DROP FRAME switch on the front panel,

HOURS	MINUTES		SECONDS	FRAMES																													
	TENS	UNITS																															
00 ~ 23	0 ~ 5	0	00 ~ 59	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
		1 ~ 9	00	☒	☒	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
			01 ~ 59	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29

☒ : DROP FRAMES

	DROP FRAME ON	DROP FRAME OFF
NUMBER OF DROP FRAMES IN 10 MINUTES	18	0
NUMBER OF DROP FRAMES IN 1 HOUR	108	0
NUMBER OF FRAMES IN 1 HOUR	60x60x30−108 = 107,892	108,000
REAL TIME FOR 1 HOUR COLOR TIME	107,892 / f_F = 3,599.997 (SEC)	3,603.600 (SEC)
COLOR TIME ERROR IN 1 HOUR	3,599.997−3,600 = −0,003 (SEC)	+3,600 (SEC)

$4f_s = 14.31818$ (MHz)
$f_s = 3.579.545$ (MHz)
$f_H = 4f_s/910 = 15.73426$ (KHz)
$f_V = 2f_H/525 = 59.94005$ (Hz)
$f_F = f_V/2 = 29.97003$ (Hz)

Figure 5-43 Drop Frame vs. Color Rate

5.6.7 Data Select Timing Generator

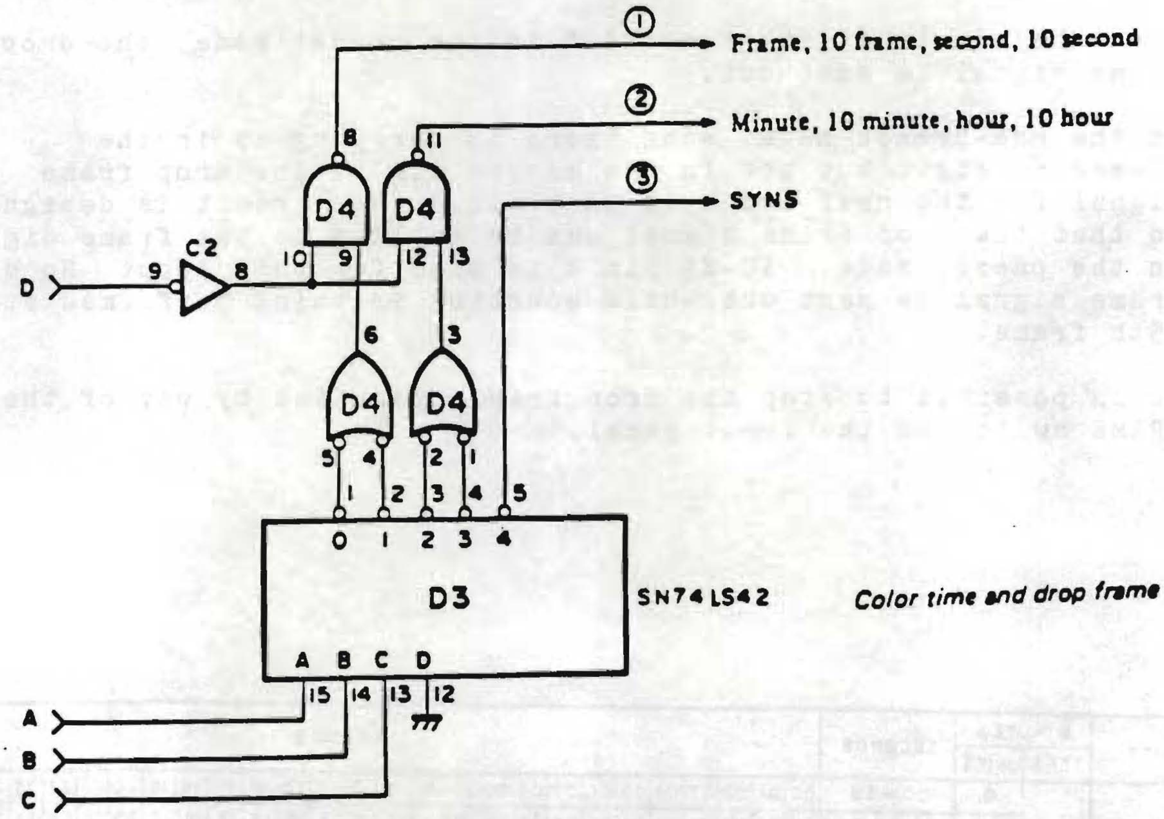


Figure 5-44 74LS42 Selector Circuit

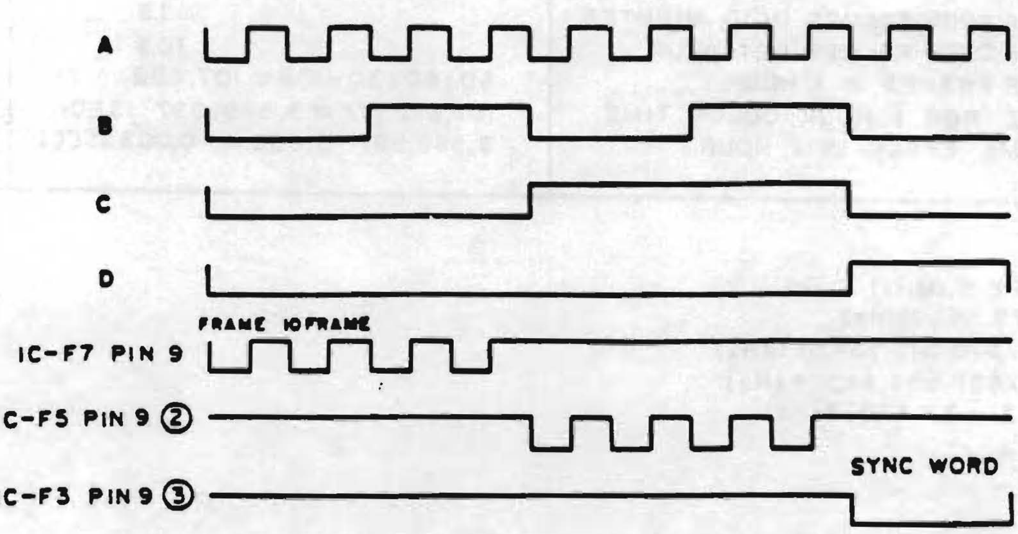


Figure 5-45 Data Select Timing Diagram

5.6.8 Time Code Generator

The time code generator encodes the timer output for the SMPTE code in the bi-phase format.

Circuit

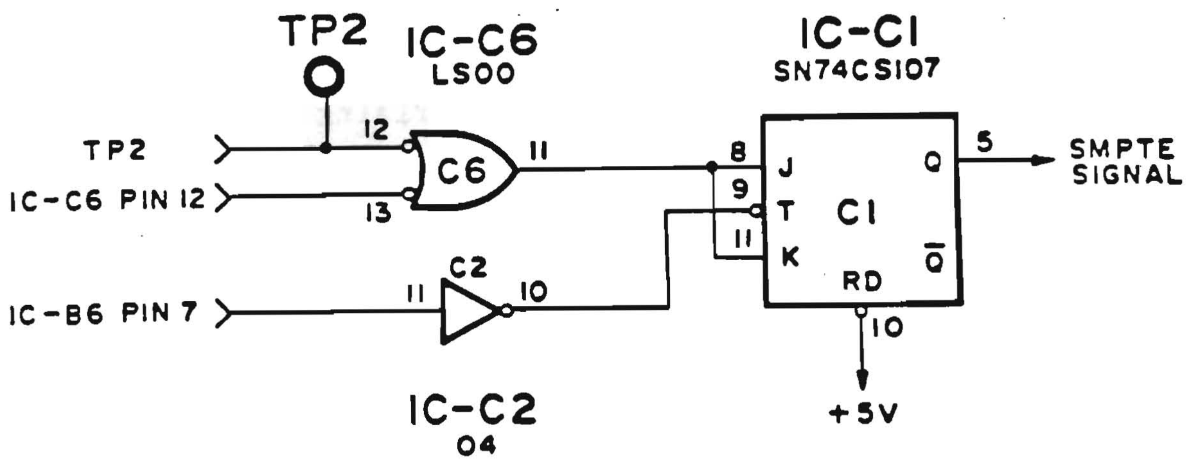


Figure 5-46 SMPTE TC Generator

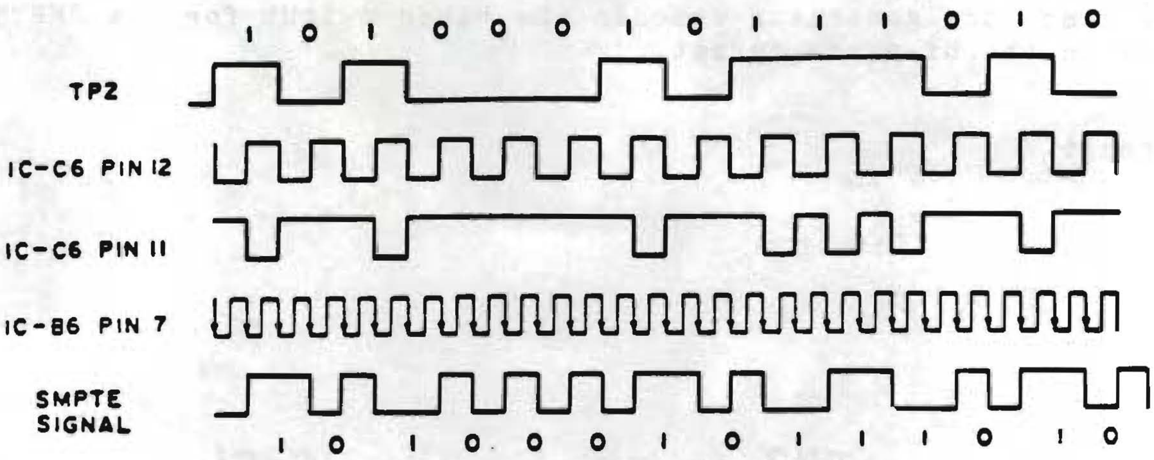


Figure 5-47 SMPTE TC Generator Timing Diagram

Figure 5-47 shows the overall timing. Figure 5-44 gives a clear picture of the timing relationship between the second and the frame pulses (IC-D4 Pin 3), the hour and the minute pulses (IC-D4 Pin 6), and the SYNC WORD pulse (IC-D3 Pin 5).

5.6.9 Function Controller Circuit

TIME CODE OUT		RUN	HOLD	RESET	X
REMOTE	RUN	H	L	L	H
CONTROL	HOLD	L	H	L	H

Table 5-8 Time Code Generator Remote Control Selection

INT \ EXT	RUN	HOLD	RESET	X
RUN	RUN	HOLD	RESET	RUN
HOLD	RUN	HOLD	RESET	HOLD
PRESET	RUN	HOLD	RESET	KESET

Table 5-9 Time Code Generator Local Control Mode Selection

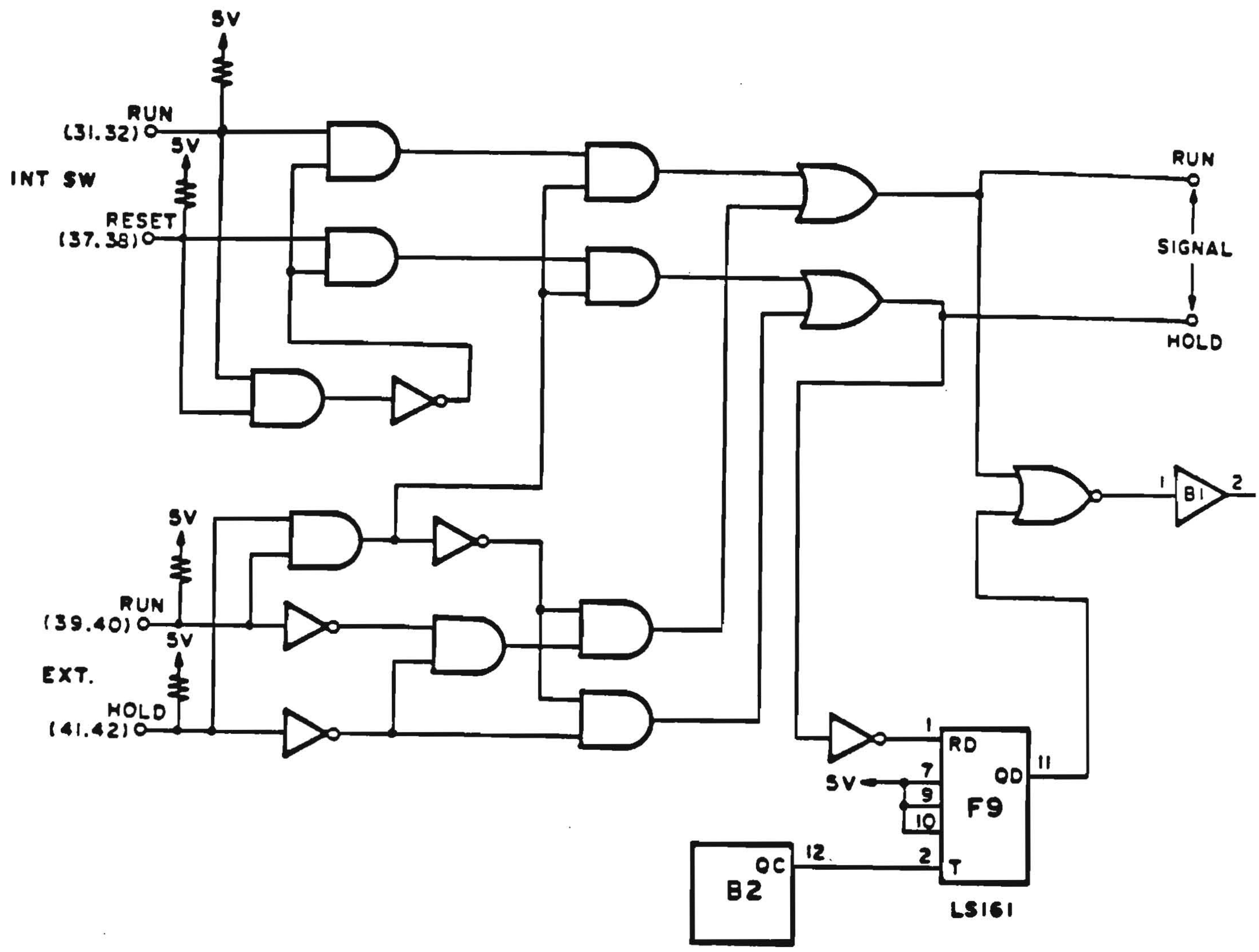


Figure 5-48 TC Generator Control Logic Diagram

The function controller gives first priority to the remote control signal regardless position the time code generator switch of the **PCM-1610** (See Tables 5-8 and 5-9). Figure 5-48 shows the relationship between the remote control terminals and the time code output.

5.6.10 Output Amplifier Circuit

The output signal is divided by a dual in-line type uPC4557 into two types of outputs; one is for a XLR-type connector (balanced output from an output transformer) and the other is for a BNC connector (unbalanced output). Their output levels can be adjusted by VR1 and VR2, respectively.

SECTION 6

PCM-1630 CIRCUIT DESCRIPTIONS

SECTION 6

PCM-1630

6.1 OUTLINE

The **PCM-1630** digital audio processor can be used PCM recording/playback system when it is combined with the **DMR-2000/4000** digital recorders or **BVU-800DB**.

- .When **DAE-1100A** digital editor is combined with the PCM recording/playback system, electronic (digital) editing can be performed.

- .When the digital recorders are combined with the **PCM-1630**, digital dubbing (or "cloning") can be performed.

- .When the **DMR-4000** is used as a digital recorder, the **PCM-1630** can perform the Read After Read (RAR) and Read After Write (RAW) functions. (In this case, a **DABK-1630** must be connected to the **PCM-1630**.)

- .Service tools and jigs, together with Test (TST) cards (handled as RPC, K/C and SEC) enable level adjustment and simplified functional check.

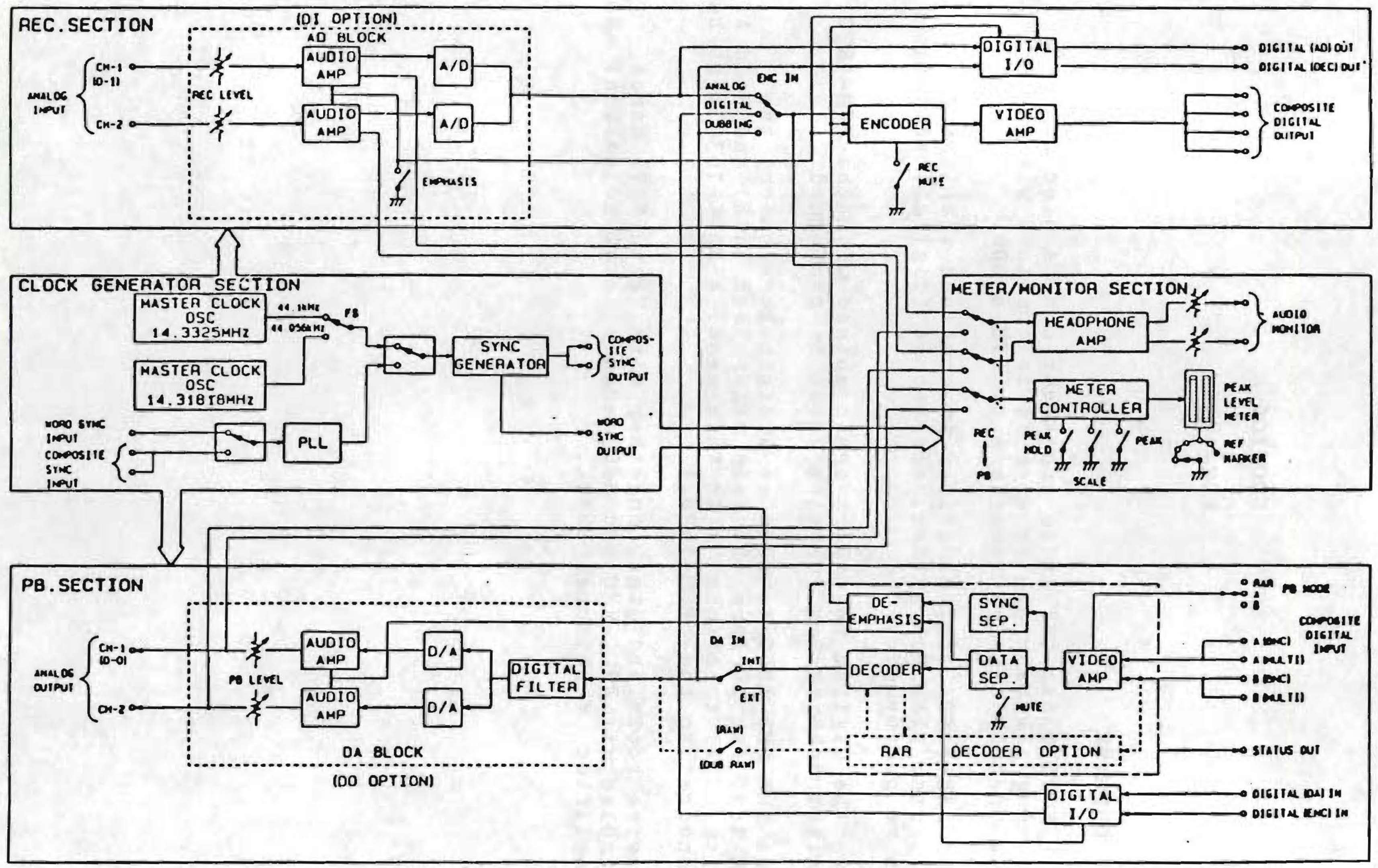
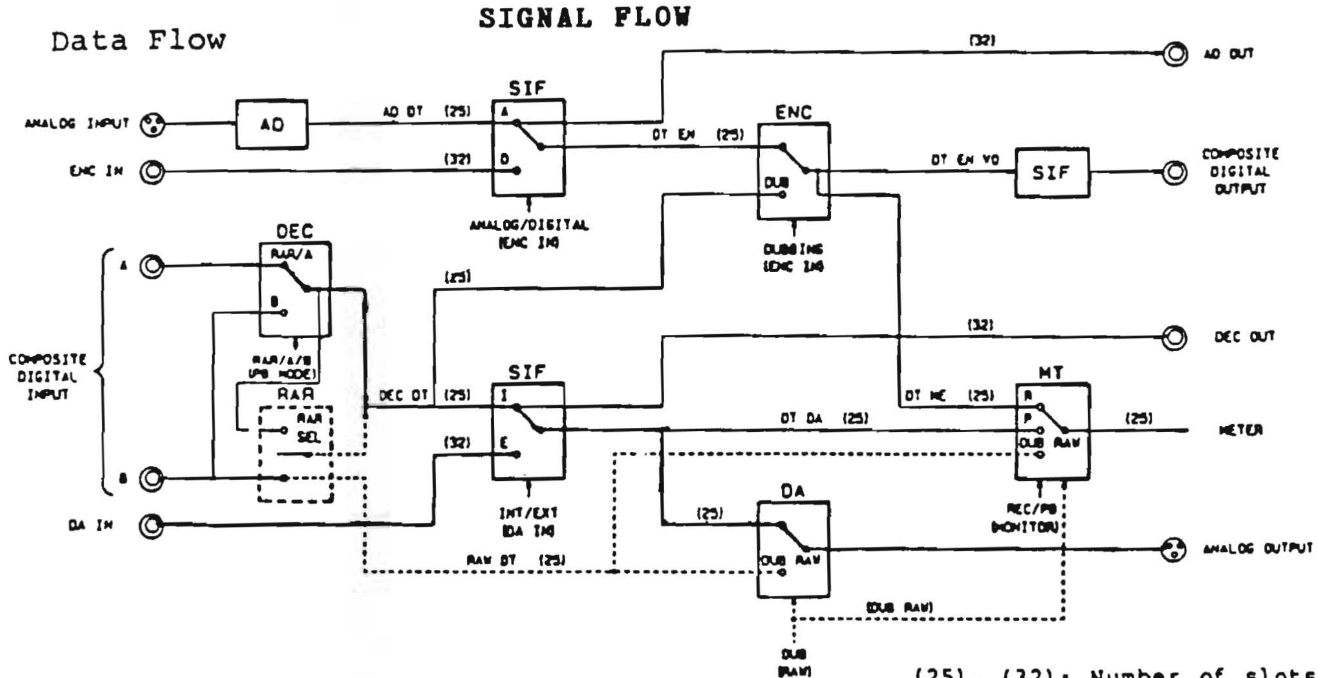

REC. SECTION
(DI OPTION)
AD BLOCK
AUDIO AMP
A/D
REC LEVEL
EMPHASIS
ANALOG INPUT
CH-1 (0-1)
CH-2
ENC IN
ANALOG
DIGITAL
DUBBING
DIGITAL I/O
ENCODER
VIDEO AMP
REC MUTE
DIGITAL (AD) OUT
DIGITAL (DEC) OUT
COMPOSITE DIGITAL OUTPUT
CLOCK GENERATOR SECTION
MASTER CLOCK OSC 14.3325MHz
MASTER CLOCK OSC 14.31818MHz
FS
SYNC GENERATOR
COMPOSITE SYNC OUTPUT
WORD SYNC OUTPUT
WORD SYNC INPUT
COMPOSITE SYNC INPUT
PLL
METER/MONITOR SECTION
HEADPHONE AMP
AUDIO MONITOR
METER CONTROLLER
PEAK LEVEL METER
REC
PB
PEAK HOLD
PEAK
SCALE
REF MARKER
PB. SECTION
ANALOG OUTPUT
CH-1 (0-0)
CH-2
PB LEVEL
AUDIO AMP
D/A
DIGITAL FILTER
DA BLOCK
(DO OPTION)
DA IN
INT
EXT
(RAW)
(DUB RAW)
DE-EMPHASIS
DECODER
SYNC SEP.
DATA SEP.
MUTE
VIDEO AMP
RAR DECODER OPTION
PB MODE
RAR
A
B
COMPOSITE DIGITAL INPUT
A (ENC)
A (MULTI)
B (ENC)
B (MULTI)
STATUS OUT
DIGITAL I/O
DIGITAL (DA) IN
DIGITAL (ENC) IN

FIGURE 6 - 1

Data Flow

SIGNAL FLOW



(25), (32): Number of slots

Figure 6-2 Overall Signal Flow

Switches

ENC IN selector: ANALOG/DIGITAL/DUBBING
DA IN selector: INT/EXT
MONITOR selector: REC/PB
PB MODE selector: RAR/A/B
RAW selector (on the optional RAR-1 board): EDT/OFF/DUB

EMPHASIS DATA FLOW

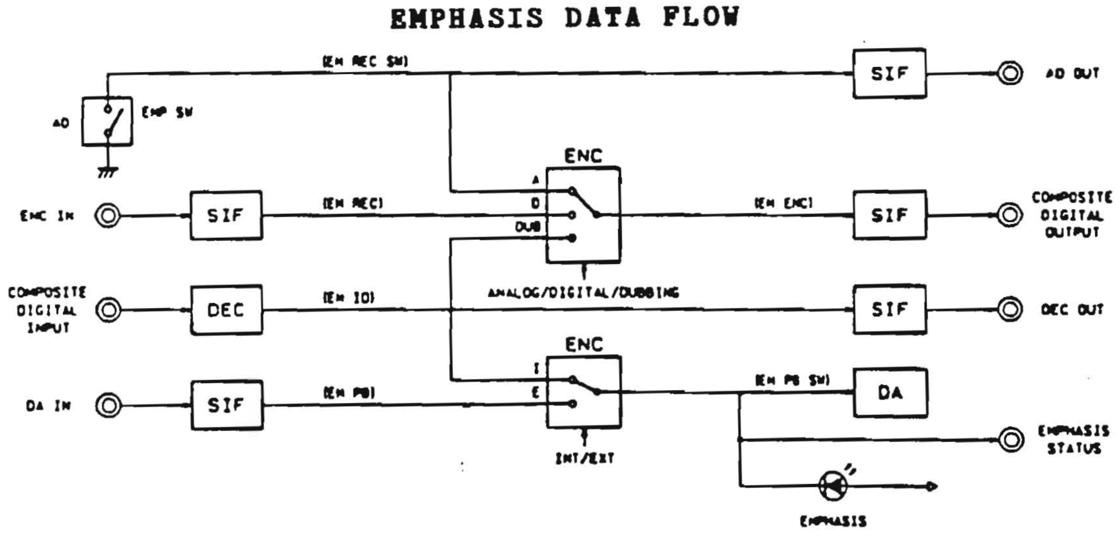


Figure 6-3 Emphasis Mode Data Flow

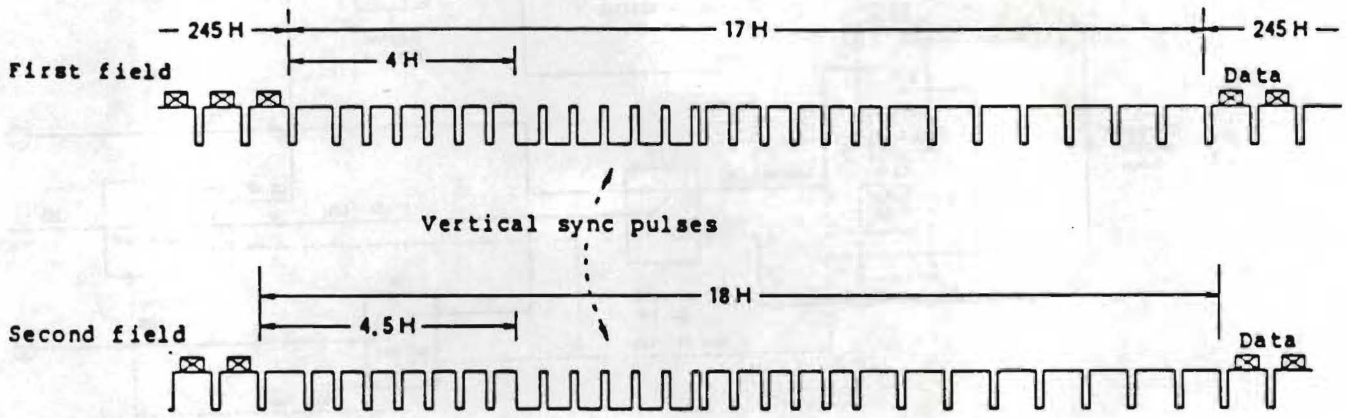
Switches

ENC IN SELECTOR: ANALOG/DIGITAL/DUBBING
DA IN selector: INT/EXT
EMP switch (on the AD-23 board): ON/OFF

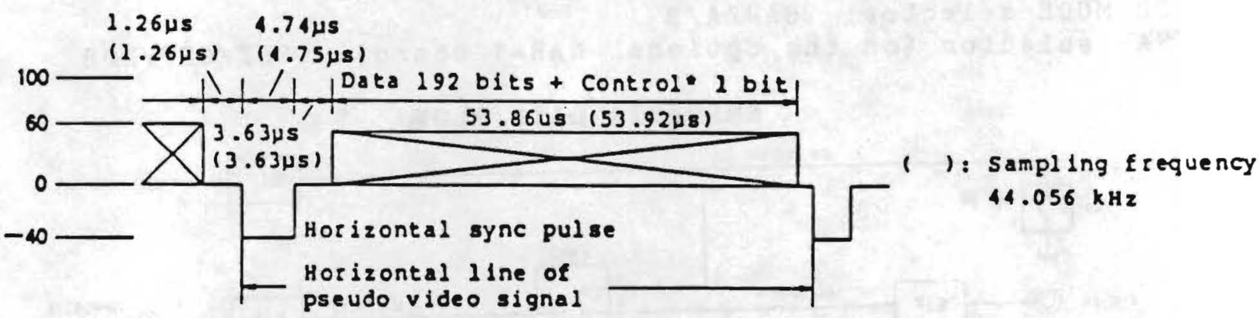
SIGNAL FORMAT

COMPOSITE DIGITAL (VIDEO) INPUT/OUTPUT SIGNALS

Data Configuration



COMPOSITE DIGITAL (VIDEO) WAVEFORMS



.Control bit (the 129th bit)

1 field = 7 blocks
1 block = 35 H

.Emphasis (the 1st H of each block)

ON: Data "0" (black on a monitor TV)
OFF: Data "1" (white on a monitor TV)

.Sampling frequency (the 2nd H of each block)

44.1kHz: Data "0" (black on a monitor TV)
44.056kHz Data "1" (white on a monitor TV)

Figure 6-4 Composite Digital (Video) Waveforms

6.2 AD-23 BOARD

The AD-23 board converts the 2-channel external analog signal into a serial digital code and send it to the SIF-1 board.

6.2.1 Analog Circuit

6.2.1.1 Input amplifier (IC101, IC102)

Analog input presented to clamping diodes through 20k-ohm resistors. IC101 and IC201 are input buffers whose output is fixed. The input resistance of the second stage (IC102, 202) is set by RV101 and RV201 (front panel) which determine the input attenuation. The emphasis circuit is found on the inverting input of the second input buffer stage. When enabled, a ground reference is given to the circuit consisting of C101, R106 and R102 (C201, R206, R207) through the FET switch Q103 (Q203). The FET is turned on by the front panel emphasis switch (S1) through IC1 optoisolator.

6.2.1.2 Emphasis amplifier

The emphasis function can be turned on or off using switch S1. The turnover frequencies are 3.183kHz (50usec) and 10.610kHz (15usec).

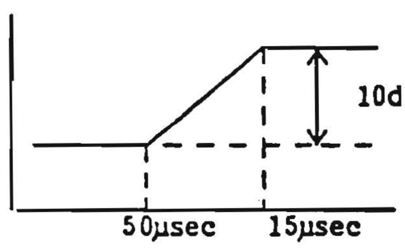


Figure 6-5 Emphasis Frequency Response Curve

6.2.1.3 Dither amplifier

The dither signal synchronized with a conversion command (CC) is added at -96dB with respect to the analog maximum input. The signal from the conversion command circuit, in this case CC, is presented to an input (pin 6) or a NOR gate (IC13) whose other input is grounded. The output is therefore inverted (CC) and routed to the dither switch (SW2). If the dither switch is ON, the CC signal is presented to the inputs of two MM5437, one for channel 1 (IC14) and the other for CH2(IC16). The outputs are fed through 1000pF capacitors and 100k resistors providing a low level sawtooth waveform which is summed with the input buffer signal at the input of the low pass filter buffer.

6.2.2.4 **Low-Pass Filter**

The input of the low pass filter is buffered by TL072 IC103 (IC203) which sums the analog input and the dither signals. The filter unit is AFL101 (AFL201) whose output is buffered by IC104 (IC204). The buffered output can be monitored on TP101 (TP201).

6.2.2 A/D Converter Circuit

6.2.2.1 Sample and Hold

When Q101 is turned on IC106 and IC107 are activated as an inverted amplifier. C106 is then charged to generate the voltage corresponding to the input signal at TP101.

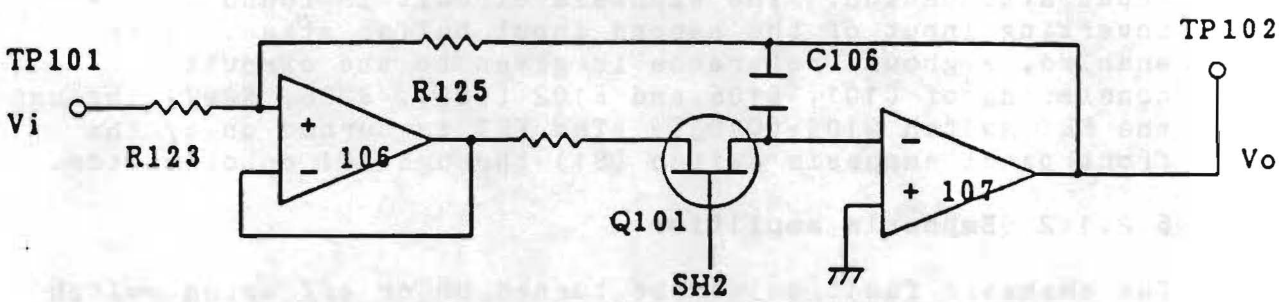
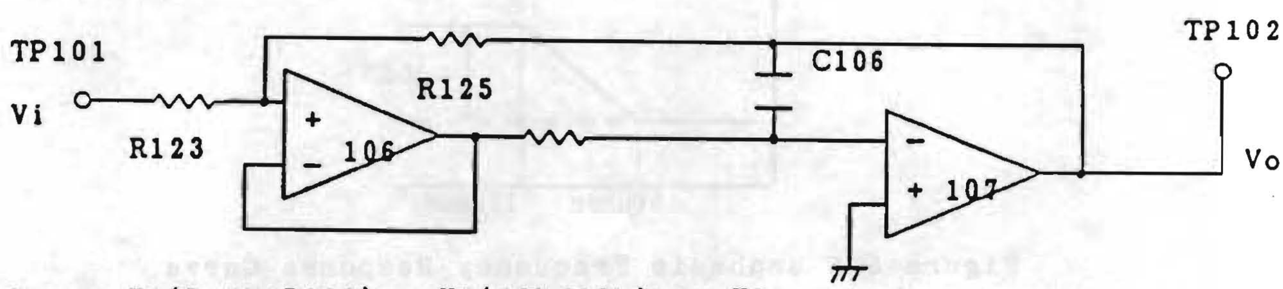


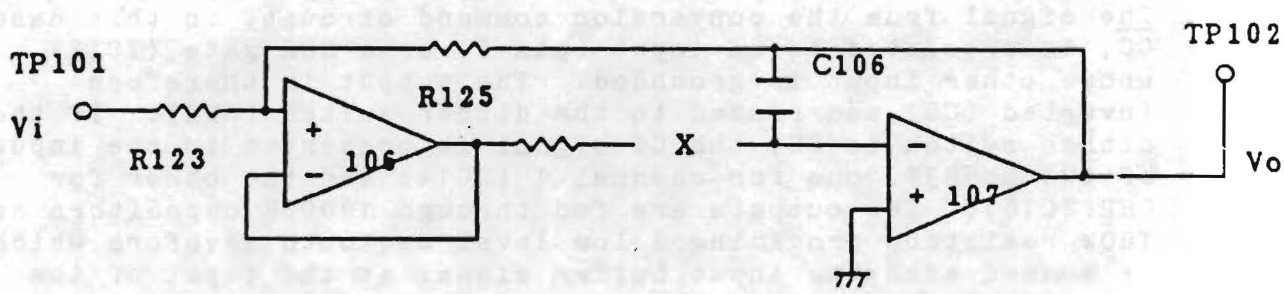
Figure 6-6 S/H Circuit Diagram

*When SH2 is high



Vo = -Vi(R125/R123) =-Vi(10k/10k) = -Vi

Figure 6-7 S/H Circuit in Sample Mode



*When Q101 is turned off, the voltage is held

Figure 6-8 S/H in Hold Mode

6.2.2.2 A/D Conversion

When the conversion command (CC) fed to IC109 (IC209) goes low, an IO signal is output from I out. The charge held by C106 (C206) is then discharged. The voltage across C106 (C206) is input through limiter IC108 (IC208) to the comparator in IC109 (IC209). When the IO signal is discharged, diode D103 (D203) is forward-biased and the output of IC108 (IC208) at TP103 (TP203) becomes +0.6V. The upper 9-bit counter is counted up using the IO signal. When the output voltage at TP103 (TP203) becomes negative, the comparator in IC109 (IC209) is inverted to stop the count-up operation. Next, the charge is C106 (C206) is discharged using the IO signal and the lower 7-bit counter is simultaneously counted up. When the voltage at TP103 (TP203) is equal to the VL2 signal voltage from IC109 (IC209), the lower 7-bit count up is stopped and the 16-bit (including the upper 9 bits) AD conversion is completed. The conversion command (CC) then goes high, and the 16-bit data is serially output in the order of most significant bit (MSB) to least significant bit (LSB).

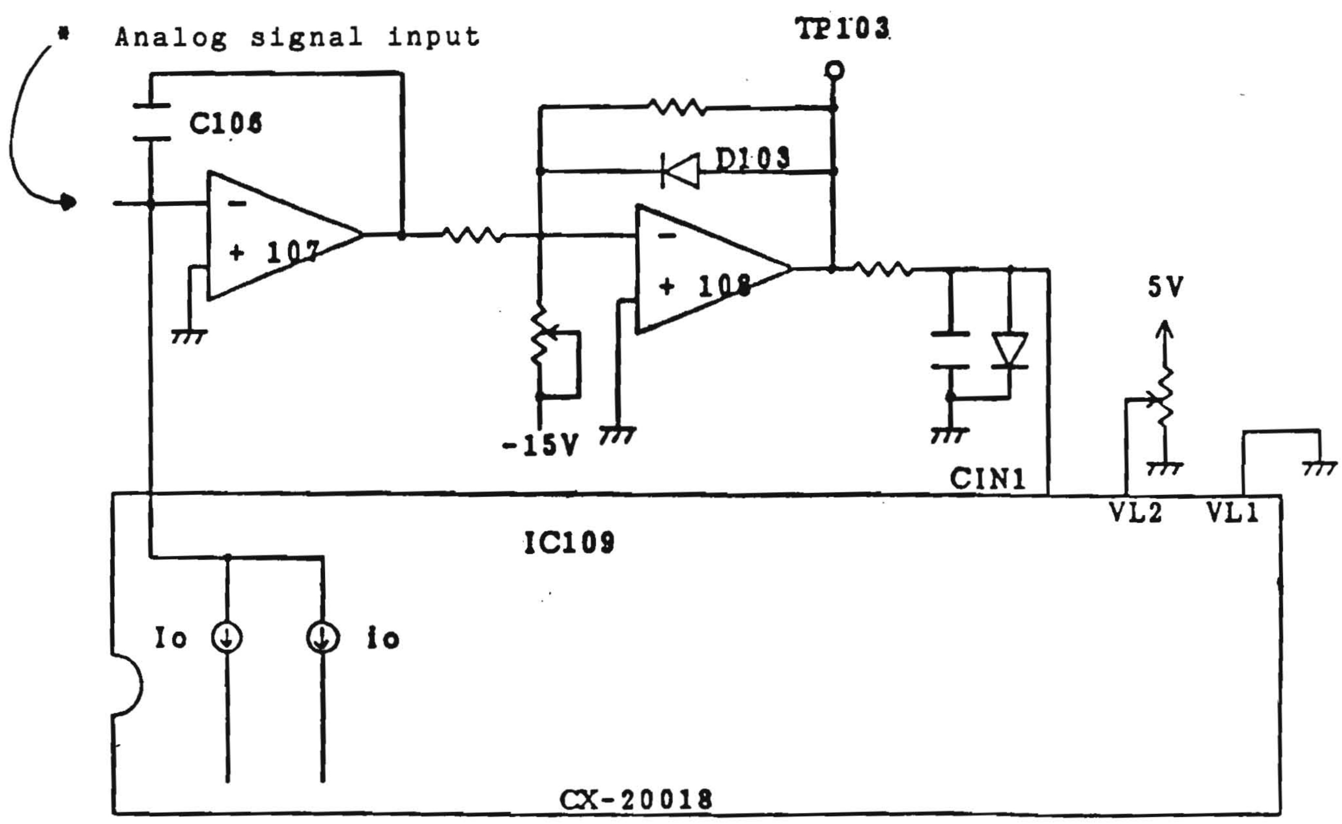


Figure 6-9 A/D Converter Schematic Diagram

6.2.2.3 A/D Offset Feedback

The most significant bit (MSB) is extracted from the A/D converted digital data by IC12 and integrated by IC103. When the analog signal contains a DC component, the potential at TP105 is biased in the plus (+) or minus (-) direction. The biased potential is fed back to IC106 to eliminate the offset.

To extract the MSB, A/D conversion is performed using the conversion command signal with the timing advanced by 1/2 bit with respect to the word clock (WDCK1) signal. Since the A/D converted data is advanced by 1/2-bit with respect to the WDCK1 signal, it is delayed by 1/2 bit using D flip-flop IC10 to send data synchronized with the WDCK1 signal.

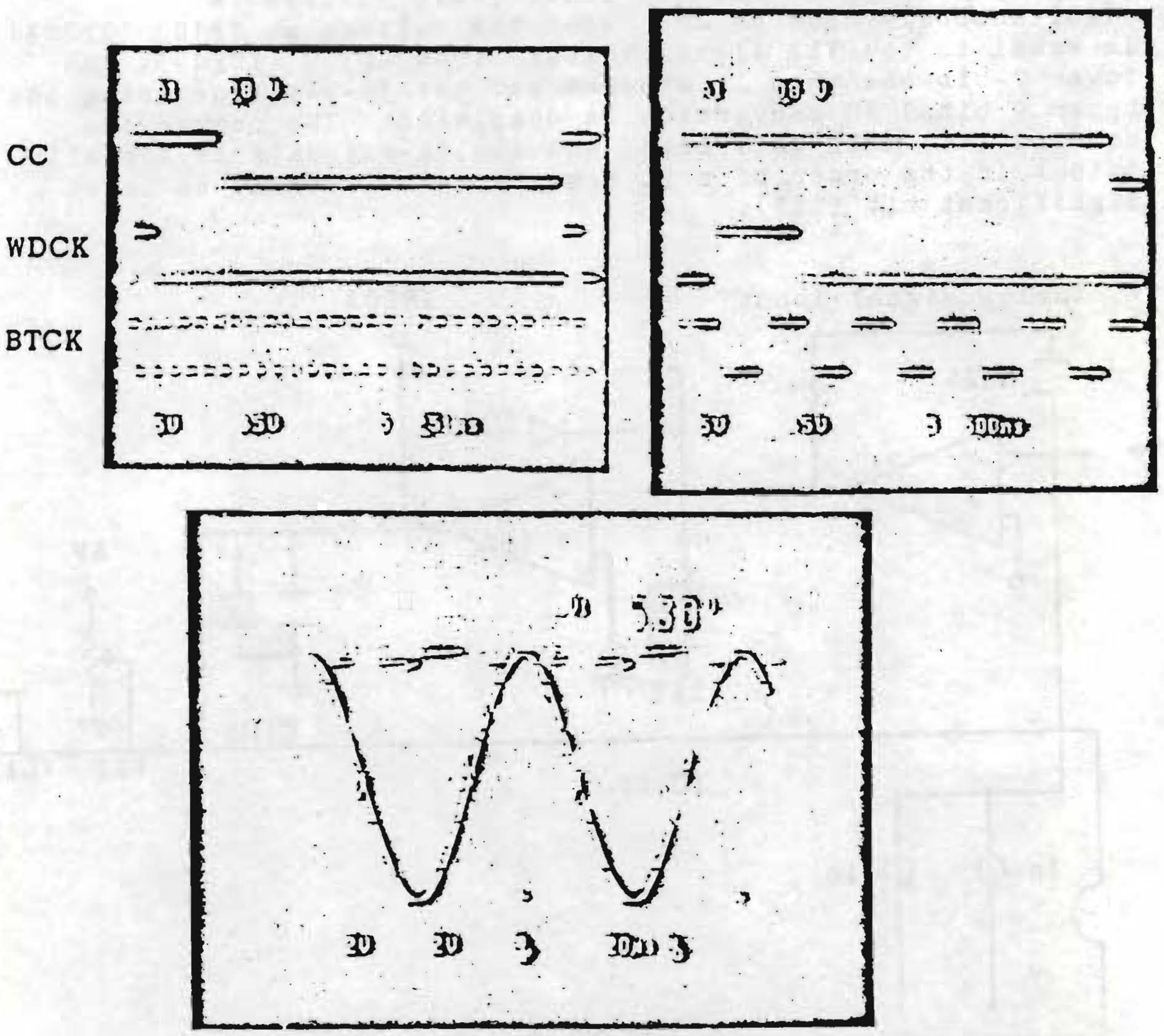


Figure 6-10 Conversion Clock, Word Clock, Bit Clock

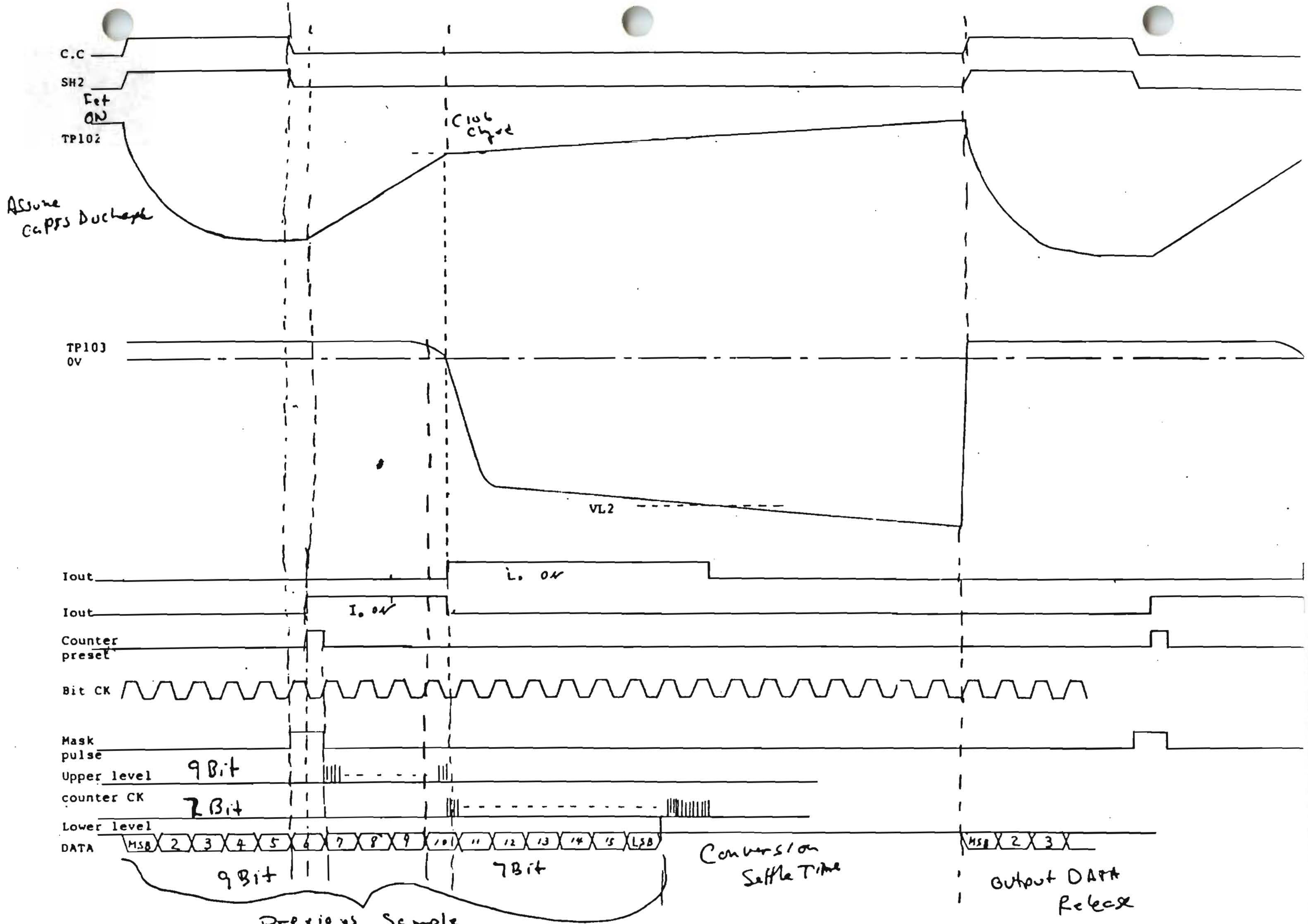

C.C
SH2
Fet ON
TP102
Assume CaPS Discharge
Clock Charge
TP103
0V
VL2
Iout
i. on
Iout
I. on
Counter preset
Bit CK
Mask pulse
Upper level
9 Bit
counter CK
7 Bit
Lower level
DATA
MSB
2
3
4
5
6
7
8
9
10
11
12
13
14
15
LSB
9 Bit
7 Bit
Conversion Settle Time
Previous Sample
Output DATA Release

FIGURE 6-11

6.2.2.4 Clock Input

The A/D converter requires two clock signals. The A/D clock is generated on board by a 48MHz crystal and 3 sections of IC15. It is tuned by CV1 (30pF variable capacitor) and feeds to the CLKIN input of IC109 (IC209). The serial output data is clocked by the bit clock input on pin 24 of the A/D converter chip (BCLK). This is derived from the data selector IC2 which selects either the BITCLK 1 or FILBITCLK signals.

6.2.2.5 Data Output

Converted analog signal data is routed to optoisolator IC9 whose output feeds to 74HC74 D-flip flops which are also clocked by the data selector IC2. The Q (inverted D-flip flop output) is buffered by a non-inverting buffer enabled by a signal produced by the FIL ON and TEST signals.

6.2.2.6 Power Regulator

An on board -5V regulator (7905) Q7 is provided to regulate -8V to -5V power supply for the A/D converters.

6.3 ENC-2 BOARD

6.3.1 Major Functions

After the two-channel analog signal is converted into two-channel, 25-slot, 16-bit digital data using an A/D circuit, encoding appropriate for the VTR based on a rotary head format is performed on the encoder board. This includes multiplexing of data to create a single data stream, HPM-1 encoding for allowing magnetic recording of the data waveforms, and addition of error correction codes.

6.3.1.1 Interleave Structure

The two-channel digital signal is word interleave processed and provided with error detection/correction check bits to limit code errors. In this case, the two-channel digital signal is time-division multiplexed on one line together with each check bit and compressed with respect to the time base to convert it into a video signal. Moreover, an EMPHASIS bit and FS ID bit are produced and added to the data signal.

6.3.2 Data Selector Circuit

One of the two data types (DT EN and DEC DT) fed to the ENC-2 board is selected using a data selector circuit analog/digital/dubbing switch). The data from the A/D converters is labelled DTEN and originates on the AD-23 card. The other digital data input comes from the decoder card and is labelled DEC DT. This is data from the decoder or from the external source.

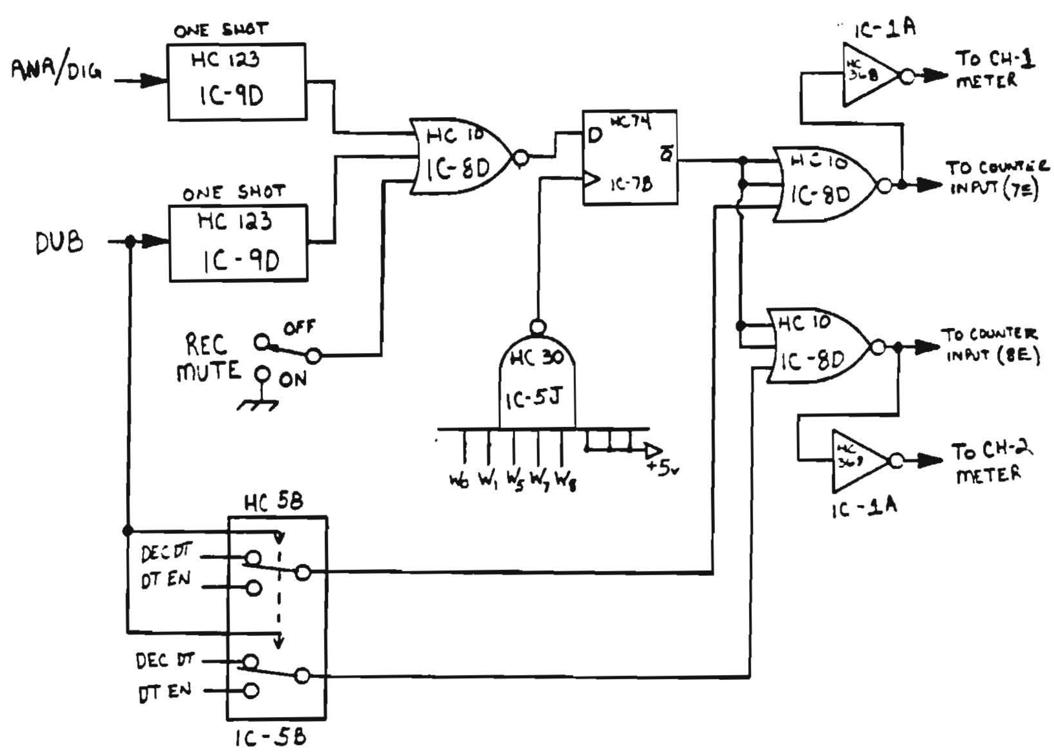


Figure 6-12 Data Selector Logic

The counter output is loaded to both the RAM data bus and to the inputs of HC195 counters. The RAM is addressed by either the R0 or R10 or W0 OR W10 signals, these being selected through 74HC157 2-to-1 data selectors (IC6H, IC6J, and IC6K) which are switched by the signal at pin 8 of IC5J. On the REC MUTE switch will cause the counters to output all zeros.

6.3.3 Interleaving

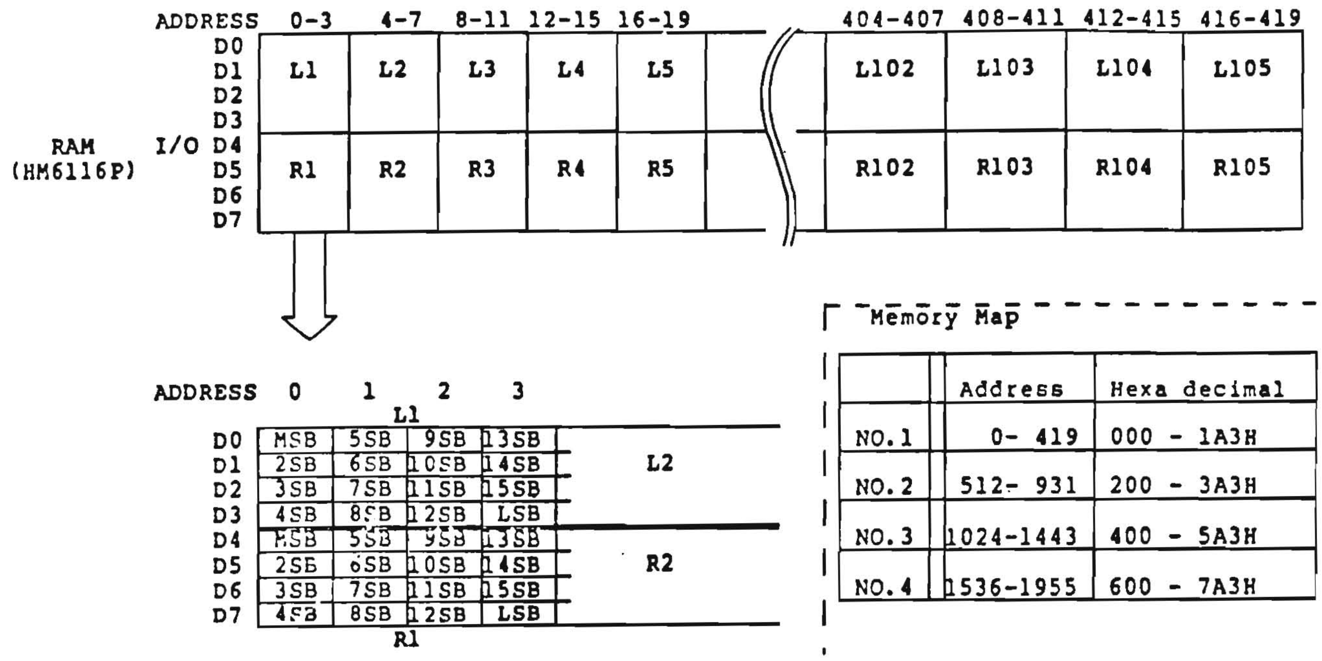
6.3.3.1 Format

As shown in Figure 6-13, data in channel 1 (L channel) and channel 2 (R channel) is written into RAM every interleaving cycle (every 35-H period.) Each of the four bits (eight bits in all) in L and R channels is assigned to one address. Using four addresses, two-word, 32-bit data is sequentially written into memory area numbers 1 through 4 in one RAM every 105 words (210 words in all) in L and R channels. As shown in Figure 6-14, data is read from memory area number 3 by interleaving the data while it is written into memory area number 1. Data is repeatedly read three times with the read speed which is 3.25 times higher than the write speed.

6.3.3.2 Write Address Counter

Using the $\overline{\text{WE}}$ clock signal produced from $\overline{\text{WE EN}}$, $\overline{\text{BIT CK3}}$, and $\overline{\text{CK MST}}$ signals, a 420 ring counter consisting of three 74HC161 counters and a 74HC30 gate is driven to generate an ADDRESS signal.

The RAM is also divided into four areas using another 74HC161(IC8K). Each of the four bits (eight bits in all) in L and R channels is assigned to one address. Two-word data is written using four addresses. Therefore, data corresponding to one interleaving block is written into a RAM consisting of 105 words x 2 = 210 words.



	Address	Hexa decimal
NO. 1	0- 419	000 - 1A3H
NO. 2	512- 931	200 - 3A3H
NO. 3	1024-1443	400 - 5A3H
NO. 4	1536-1955	600 - 7A3H

Figure 6-13 RAM Address Map

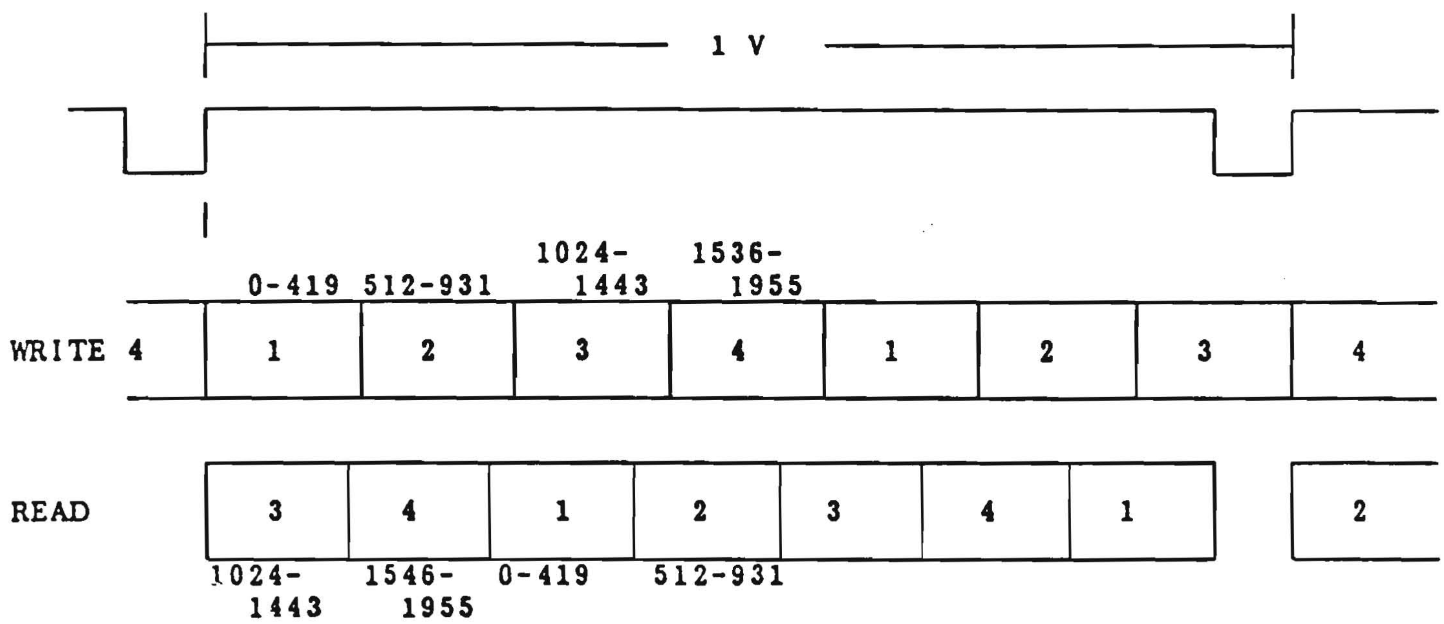


Figure 6-14 Read/Write Addresses

6.3.3.3 Read Address Counter and Data Selector

The read address counter consists of a 420 ring counter and a binary square counter for area assignment, as in the write address counter. The read speed is 3.25 times higher than the write speed. As shown in Figure 6-14, when the 35th block of data is read, the counter again returns to the former address, and the data is again read up to the 35th block.

Data at the same address is read three times in all. The data read from memory area number 3 consists of four bits in channel 1 and four bits in channel 2 (eight bits in all) for every address. The data is parallel-to-serial converted as serial data in a word unit using a 74HC195. When one line is read during coding, output Y of the data selector (74HC153) is connected to input C0 to send data (R1) in channel 2. Output Y is connected to C2 to send data (L2) in channel 1. Next, output Y is reconnected to C0 to send data (R3) in channel 2. After three-word data is sent, output Y is connected to C2. However, the four-word data inhibits the read address from being incremented and sends no data. Moreover, no data (16-bit) from the RAM can be sent using the AND-OR circuit (HC51) in the next stage. The CRC data (with respect to the above three-word data) calculated using a CRC generator (CX23021) is inserted during the period in which data is not sent (refer to Figure 6-16). As described above, CRC data is added to the three-word data as one CRC block. As a result, blocks one through 35 are executed, and the one-line read is completed. The two-line read is then performed. The address is returned to top address 1024 (400hex) of memory area number 3 and read is done as for one line.

Data in channels 1 and 2 is input to an exclusive OR circuit (IC5E) which functions as a parity generator at all times. Therefore, the output of IC5E becomes parity data, and output Y of the data selector is connected to C1 or C3 to send parity data, P1, P2, and P3 (16-bit, respectively). In the next four-word data, CRC data is added to parity data P1 through P3 as in the one line read. As a result, blocks one through 35 are executed as in the one-line read. Next, three-line read is done. The address is returned again to top address 1024 (400hex), and data is read as in the one line read. The above reading of one through three lines accomplishes one coding block.

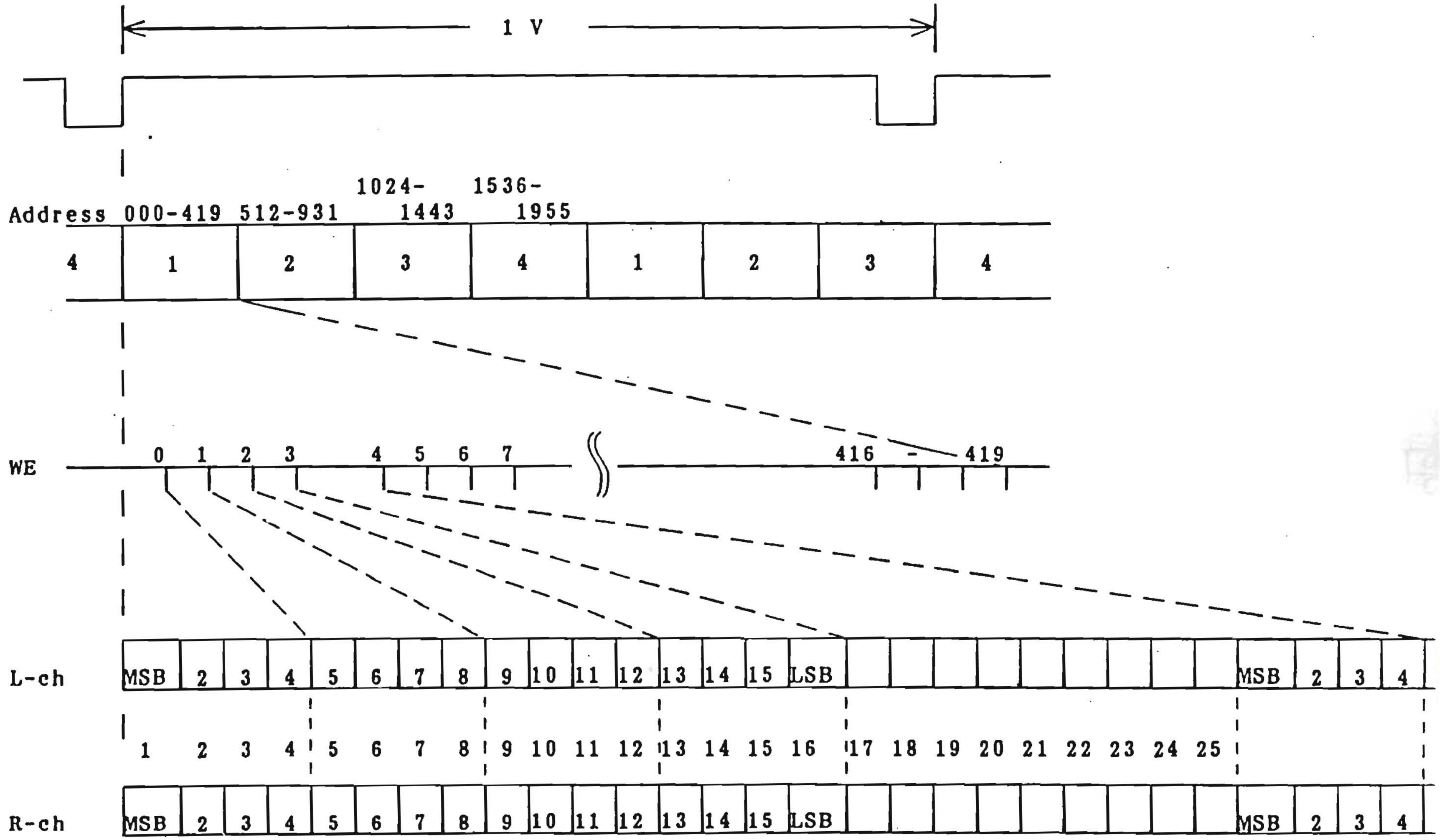
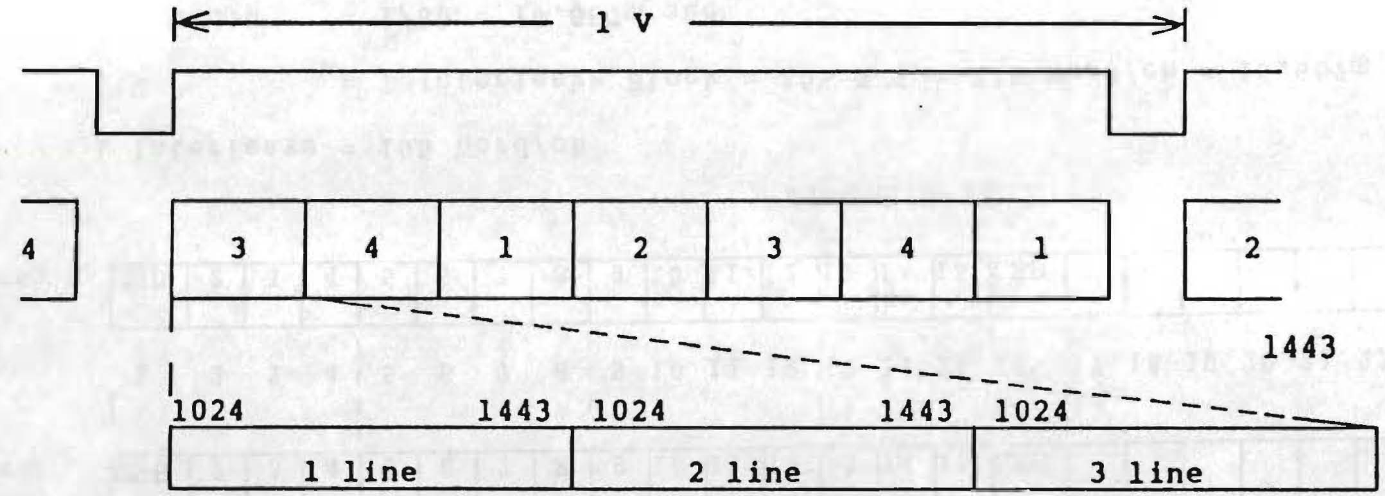


FIGURE 6-15

1 Interleave = 105 Word/ch

1 V = 7 Interleave Block = 105 X 7 = 735 Word/ch = 16.667m sec

1 V Width = 1/60 = 16.667m sec



1 Interleave

	1st Block				2nd Block				3rd Block					34th Block				35th Block			
1 line	R1	L2	R3	C	L4	R5	L6	C	R7	L8	R9	C		L100	R101	L102	C	R103	L104	R105	C
2 line	P1	P2	P3	C	P4	P5	P6	C	P7	P8	P9	C		P100	P101	P102	C	P103	P104	P105	C
3 line	L1	R2	L3	C	R4	L5	R6	C	L7	R8	L9	C		R100	L101	R102	C	L103	R104	L105	C

1 Interleave = 35H

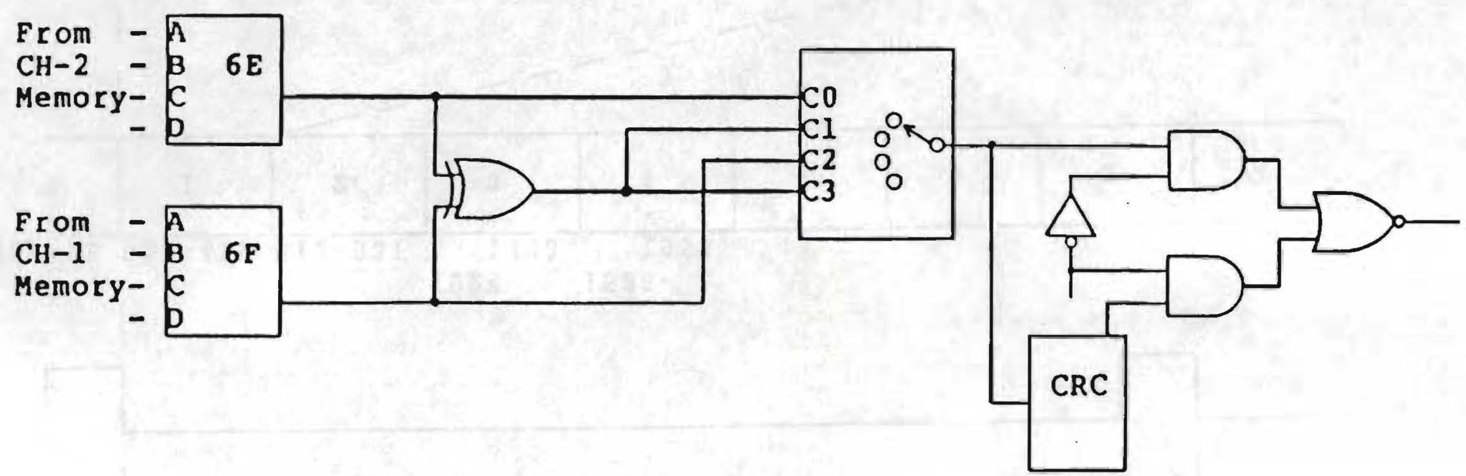


FIGURE 6-15

6.3.4 Skew Bit Adding Circuit (IC1B, IC1C, IC1D)

This circuit adds a skew bit to the interleaved data signal as a control bit. The data signal consists of a 192-bit 1H-sync signal (193 bits in all) with the one skew bit inserted after the 128th bit.

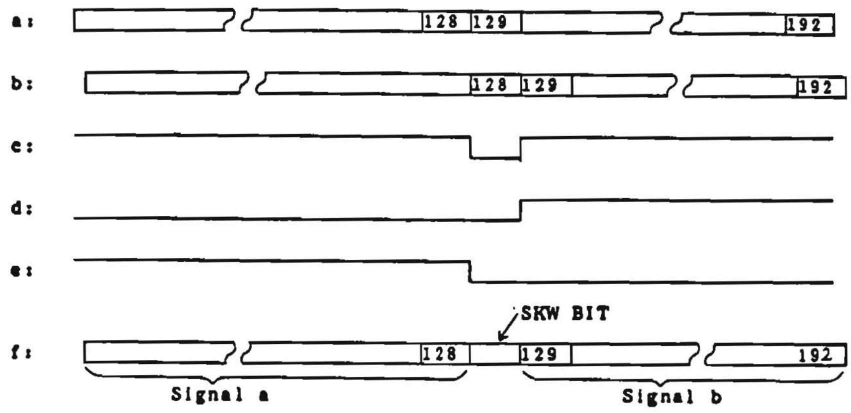


Figure 6-16 Skew Bit

Data signal a is delayed using a 74HC74 D flip flop to produce data signal b. The timing of data signals d and e from the skew bit is generated using another 74HC74 and selected at the 128th data position using the 74HC51 AND-OR gate. Consequently, data signal f can be obtained. The two-channel data is then coded, time-compressed into one line, and sent as a DT ENVO signal.

6.4 SIF-1 BOARD

6.4.1 Major Functions

The Serial Interface (SIF-1) card is located in the **PCM-1630** card rack.

6.4.1.1 External Sync Phase Lock Loop

When synchronization is established using an external sync signal (composite sync or WD sync signal), the unit is synchronized with the external sync signal using a PLL circuit.

6.4.1.2 Master Clock

A master clock is produced to generate the clock necessary for the video circuit.

6.4.1.3 Composite Digital Output

The coded data signal on the ENC-2 board is mixed with the composite sync signal and output to the external unit as a composite digital signal.

6.4.1.4 Data Compression/DC Compression

The one-word 25-slot digital signal is converted into a 32-slot signal and sent to a transfer line. The 32-slot signal from the transfer line is converted into the 25-slot signal.

6.4.2 External Sync

6.4.2.1 Switching Circuit

The external sync signal contains a word (WD) sync, composite sync, and digital data input DI sync (AES/EBU) signals. The composite sync signal is a video signal level which is converted into a TTL level using D1, D2, D3, and Q7 and fed to IC4J (HC221), where an equalizing pulse and V sync signal are eliminated to produce a continuous H sync signal. The H sync signal and the WD sync or DI sync signal passed through receiver IC4B (SN75124) are selected using the switching circuit in the NAND gate circuits (3K, 4K, and 6K). When the H sync signal and WD sync or DI sync signal are sent at the same time, the composite sync signal is selected with priority (refer to Figure 6-17).

6.4.2.2 Phase Locked Loop

The sync signal selected using the switching circuit described above is fed to the REF terminal of phase comparator IC3N (MC4044) which constitutes a phase locked loop PLL circuit. When the composite signal is input to the REF terminal, the output of a comparator (NE529) is frequency-divided by 910 using a counter consisting of IC5M, IC5L, and IC6L (HC163). The resultant signal is fed to the V terminal of IC3N and compared. The PLL circuit is then locked, the gen-lock is activated (CX7903), and various synchronized TV signals are produced (CX773B).

14.3325MHz 910 = 15.75kHz
14.31818MHz 910 = 15.734kHz

When the WD clock is input to the REF terminal, the output of VCXO is frequency-divided by 325 on the DEC-15 board, sent to the V terminal as a sync signal (S/L and compared with the WD clock. The PLL circuit is then locked.

14.3325MHz 325 = 44.1kHz
14.31818MHz 325 = 44.056kHz

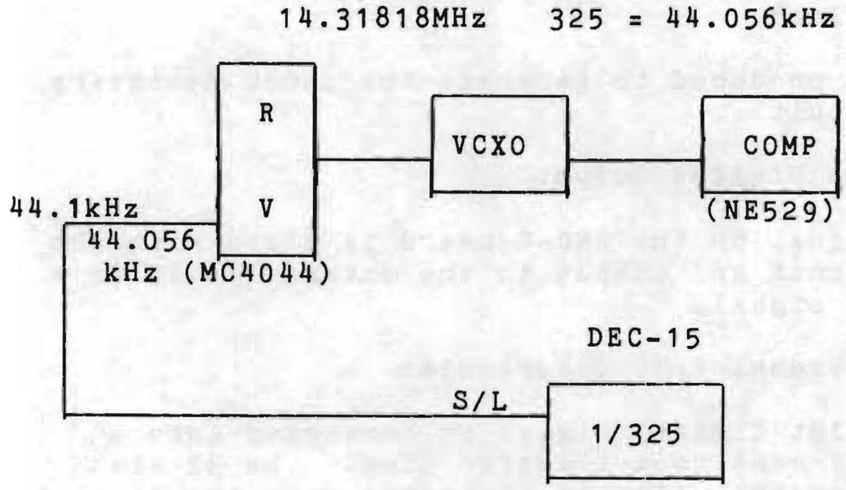


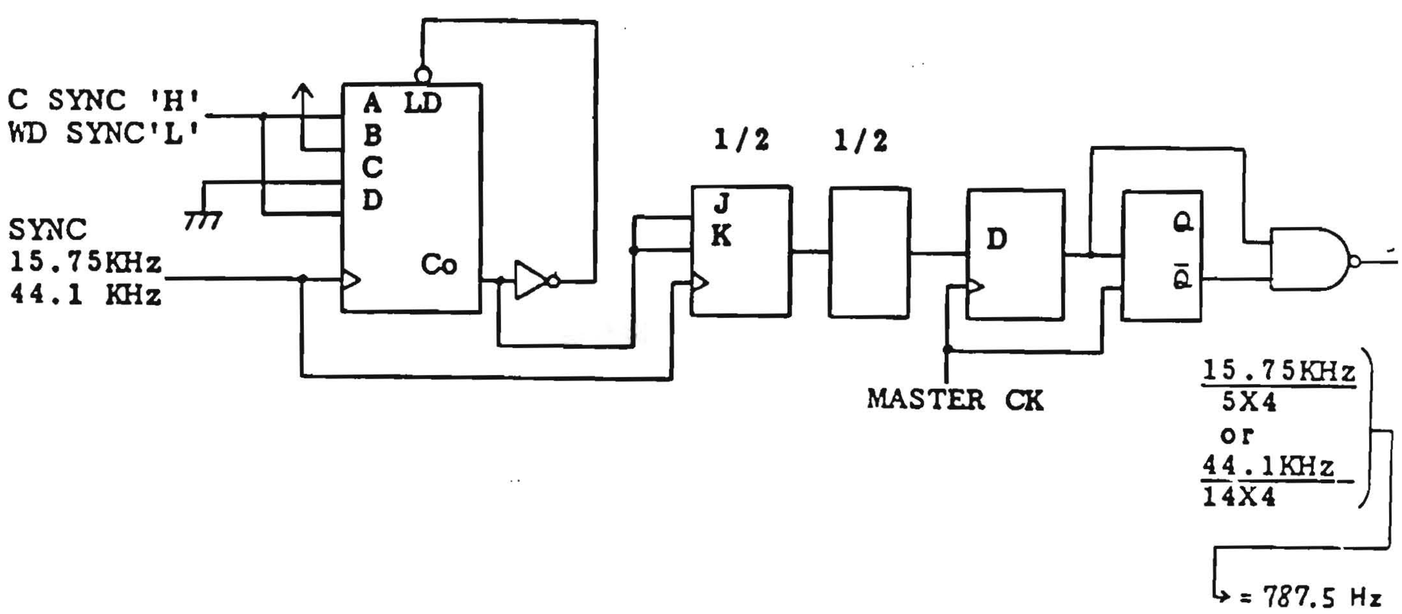
Figure 6-17 PLL Circuit Block Diagram

When synchronization is established using the external sync signal, the VCXO output in the PLL circuit is used as the master clock. When no external sync signal is input, the internal oscillating clock output is used as the master clock (IC6N, IC7M, and IC7N). The master clock is sent to TV sync signal generator IC7H (CX773B) to produce the TV sync signals (composite SYNC signal, VD pulse, HD pulse, even field pulse, and odd field pulse). The composite sync signal is output through a sync amplifier consisting of Q15, Q16, and Q17. The composite sync signal is also sent to IC2C (UA733), where the coded data on the ENC-2 board is added to it. The resultant signal is amplified using a video amplifier consisting of transistors Q18 and Q19 and output as a composite digital signal.

6.4.3 44.1kHz/44.056kHz Discriminator Circuit

When the **PCM-1630** receives an external sync signal, this circuit discriminates whether the WD clock IN signal is 44.1kHz or 44.056kHz (15.75kHz or 15.734kHz for the composite sync IN signal). At that time, the LED indicator lamp on the front panel lights (IC1K, IC1J, IC2K, IC3K, IC1F, IC2F, IC3F, IC4F, IC4K, and IC2J).

.For composite sync IN



* For C sync: 1/5
* For WD sync: 1/14

Figure 6-18 Discriminator Circuit

The difference between 44.1kHz and 44.056kHz is 0.1%. Therefore, discrimination is based on how many internal master clock pulses are inserted during the period by frequency-dividing the WD clock or composite sync signal. For the actual discrimination, a half time of the above period is taken.

$$T1 = (15.75/5 \times 4)^{-1} /2 = (44.1/14 \times 4)^{-1} /2\text{msec}$$
$$T2 = (15.734/5 \times 4)^{-1} /2 = (44.056/14 \times 4)^{-1} /2\text{msec}$$

EXTERNAL SYNC / Internal Master Clock	44.1kHz (15.750kHz) T1	44.056kHz (15.734kHz) T2	Discrimination Point
14.3325MHz	9100	9109	<9105<
14.31818MHz	9090	9099	<9095<

Figure 6-19 Sync/Discrimination Point Table

.When the master clock is 14.3325MHz.

If the counter is set so that it is counted up at 9105 when the external sync signal is 44.1kHz (15.75kHz), count is completed at 9100 during the T1 period. The output (QD) of counter IC4F is held high, so the 44.1kHz EXT LED indicator lamp lights. When the external sync signal is 44.056kHz (15.734kHz), the counter is counted up by 9109 during the T2 period, so it is counted up at 9105 and the QD goes low.

.Muting circuit (IC2J, IC3J, IC3H, IC4M and IC4N)

If the sync signal is disturbed and the synchronization is not established for any reason (connecting or disconnecting of an external sync signal line, etc.) when the **PCM-1630** is synchronized with the external sync signal, the muting circuit supplies a muting signal (MUT3) to the DEC-15 board and prevents click noise.

6.4.4 11.2896MHz PLL Circuit (Q10, Q11, Q12, Q13, Q14, IC9N, IC8J, IC8K, IC9J, and IC9K)

The PLL circuit is used to produce a digital input/output clock. The S/L signal (CK MST(44.1kHz) frequency divided by 325 on the DEC-15 board is input to the REF terminal of IC9N (4044).

The output (11.29MHz) of the PLL circuit is frequency-divided by two using IC8K, by 16 using IC8J, and by eight using IC9J. (i.e., by 256 in all).

$$\frac{11.2896\text{MHz}}{256} = 44.1\text{kHz}$$

When the resultant signal is input to the V terminal of IC9N(4044), an input/output clock which is phase-synchronized with the S/L signal can be obtained.

6.4.5 Digital I/O Circuit

The CX23070 is a serial data interface LSI used for communication between devices with **PCM-1610** format digital I/O.

Figure 6-20 show the **PCM-1610** digital I/O format. The digital I/O signal is a serial PCM audio signal which is synchronized with a word sync signal and where a word consists of 32 slots. In the **PCM-1610**, however, signal processing is performed at 25 slots per word, so 32 slot-25 slot word conversion is required.

The LSI consists of two blocks: digital IN and digital OUT. The digital IN block extracts sync signals from 32-slot signals sent by the external device and converts them to 25-slot signals. It also makes control bit extraction every 256 words. The digital OUT block converts 25-slot signals to 32-slot signals for transmission to the external device (see Figure 6-20. (One channel is handled for each I/O operation).

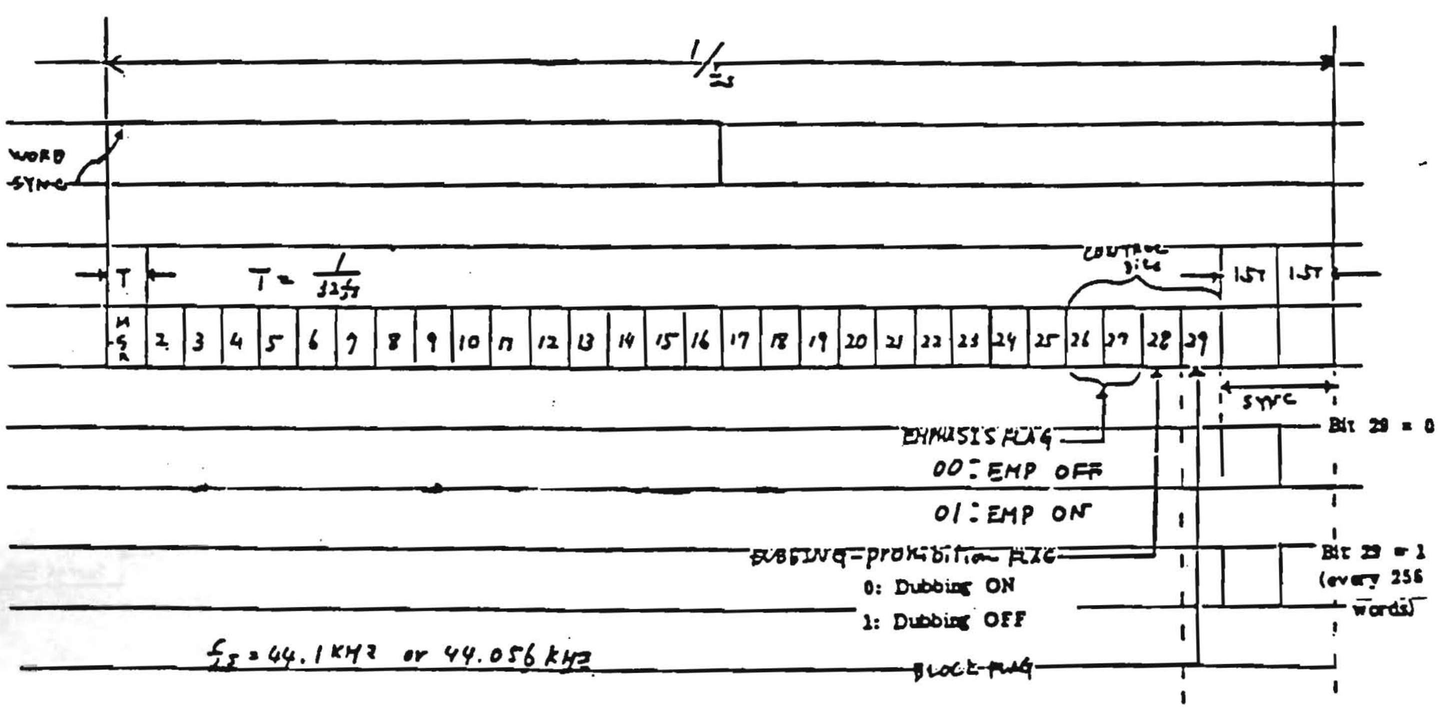


Figure 6-20 Data/Sync Timing Diagram

This LSI allow master/slave control by setting its TE04 pin to H or L. A usual data interface handles two channels at the same time. Such an interface therefore needs two CX23070 serial data interfaces. But if two CX23070 devices operate separately, block flags will not synchronize. To synchronize block flags, one LSI must be used as the master and the others used as slaves.

To operate two or more CX23070 devices individually and synchronize block flags, a power on reset operation needs to be performed using TE07 and TE08 pins.

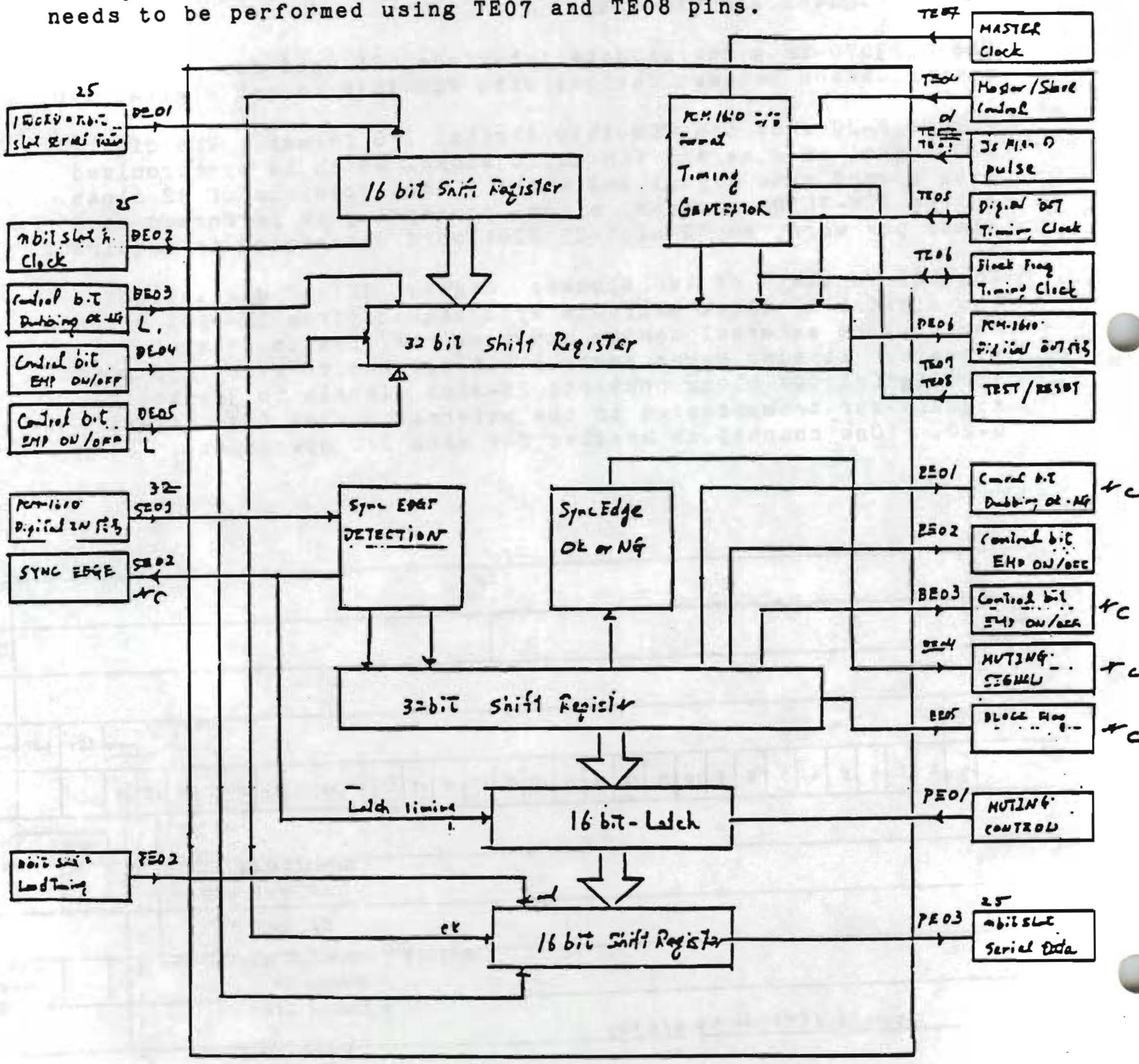
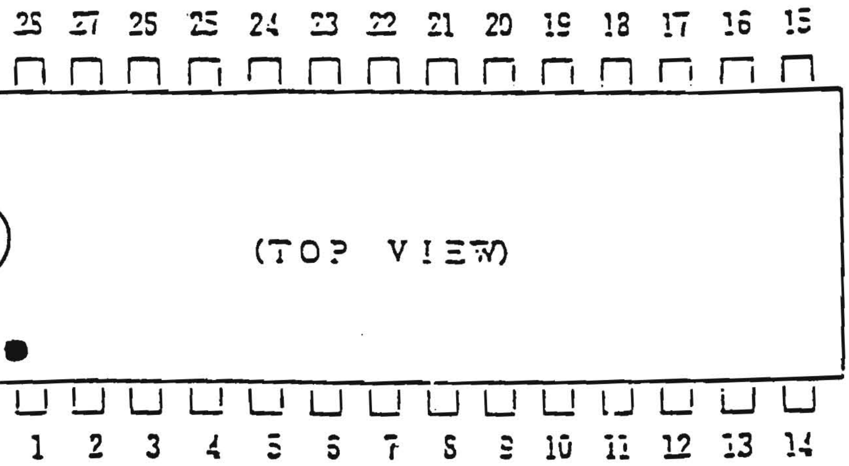


Figure 6-21 CX23070 Block Diagram

MB 63H124 (CX23070)

NOTE: Indicates a Fujitsu part.

Pin assignment (DIP-23)



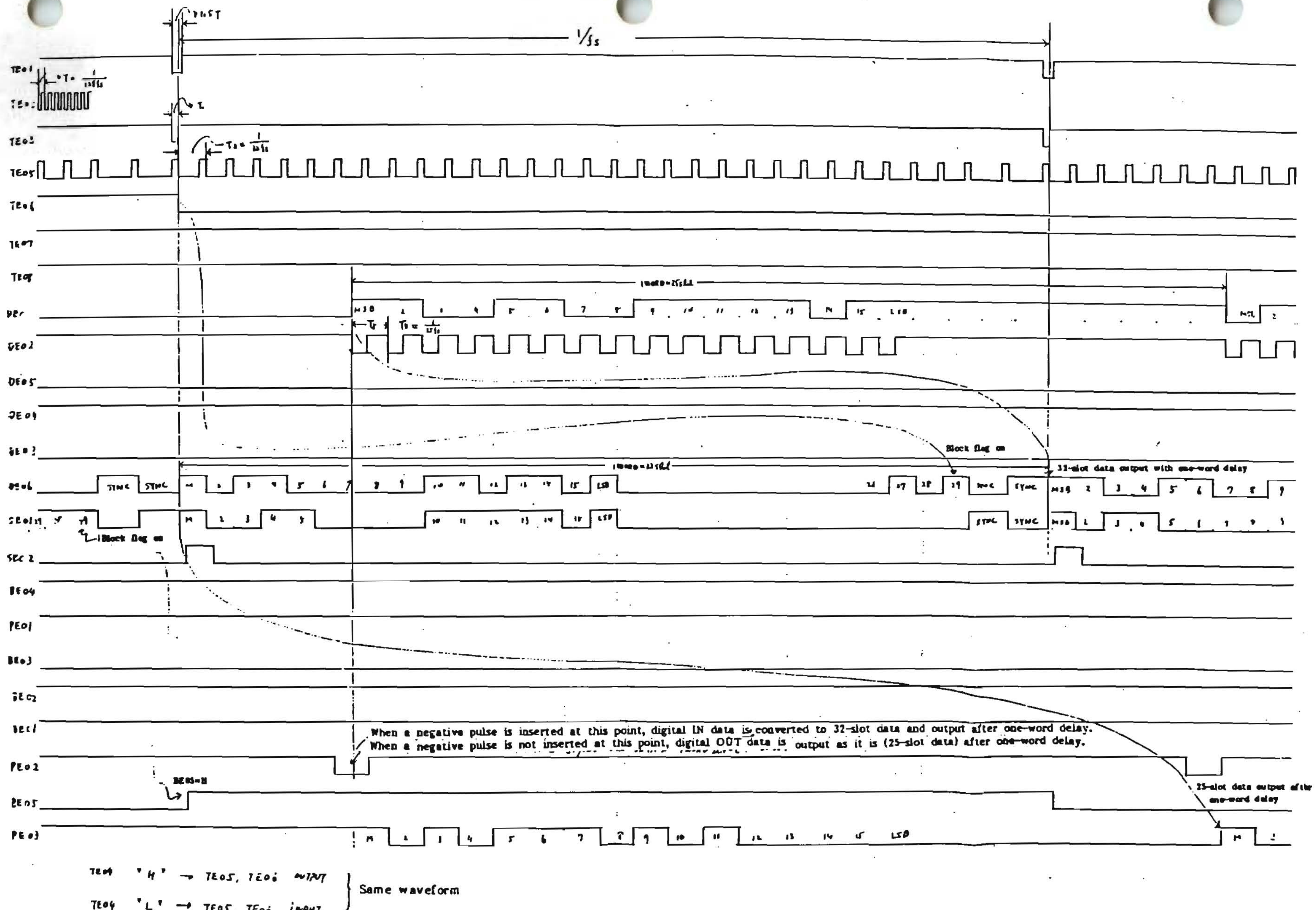
Pin no	I/O	Pin name	Pin no	I/O	Pin name
1	I	TE01	15	Ō	DE06
2	I	TE02	16	I	SE01
3	I	TE03	17	Ō	SE02
4	I	TE04	18	Ō	BE04
5	I/Ō	TE05	19	I	PE01
6	I/Ō	TE06	20	-	NC
7	—	VSS	21	-	VDD
8	I	TE07	22	Ō	BE03
9	I	TE08	23	Ō	BE02
10	I	DE01	24	Ō	BE01
11	I	DE02	25	I	PE02
12	I	DE05	26	-	NC
13	I	DE04	27	Ō	BE05
14	I	DE03	28	Ō	PE03

Figure 6-22 CX23070 Pin-out

Pin No.	Pin name	I/O	Polarity	Waveform	Description
1	TE01	I	Negative		Timing signal for digital OUT clock generation (32 slots) (fs period)
2	TE02	I	Negative		Master clock. 5.6778MHz when fs=44.1kHz. 5.639/60MHz When f=44.056kHz
3	TE03	I	Negative		Timing signal (32 slots) (fs period)
4	TE04	I	Positive		Master/slave control signal. H indicates master and L slave.
5	TE05	I/O	Negative		In master mode, sends digital OUT timing clock to slave LSI. In slave mode, receives clock from master LSI.
6	TE06	I/O	Positive		In master mode, sends block flag timing signals to slave LSI. In slave mode, receives signals from master LSI.
7	Vss	–			Ground (0V)
8	TE07	I	Positive	Direct current	Test pin. Allows power-on-reset. Usually H.
9	TE08	I	Positive	Direct current	Test pin. Allows power-on-reset. Usually H.
10	DE01	I	Positive		Digital OUT data. The bit's change point is synchronized with the trailing edge of the clock input to DE02. 16-bit data preceding with respect to the leading edge of TE03 is valid.
11	DE02	I	Negative		n-bit slot per word signal*
12	DE05	I	Positive	Direct current	Digital OUT 26 SB control pin. Usually L.
13	DE04	I	Positive	Direct current	Digital OUT 27 SB control pin. L when emphasis=off and H when
14	DE03	I	Positive	Direct current	Digital OUT 28 SB control pin. L when dubbing=on and H when dubbing=off.
15	DE06	O	Positive		Digital OUT signal (32 slots). Synchronized with the trailing edge of TE05 signal (output in master mode and input in slave mode).
16	CE01	I	Positive		Digital IN signal (32 slots)
17	CE02	O	Positive		Digital IN timing signal for sync extraction
18	BE04	O	Negative		Digital IN muting signal
19	PE01	I	Negative	Connected to BE04 or 5 V	Digital IN muting control signal. Usually connected to BE04.
20	NC	–			
21	VDD	–			+5V power
22	BE03	O	Positive		26 SB for digital IN data. Usually L
23	BE02	O	Positive		27 SB for digital IN data. L when emphasis=off and H when emphasis=on.
24	BE01	O	Positive		28 SB for digital IN data. L when dubbing=on and H when dubbing=off.
25	PE02	I	Negative		Digital IN timing signal (or H). Negative pulse synchronized with fs. First DE02 transient (fall) is to occur during this signal=L.
26	NC	–			
27	BE05	O	Positive		29 SB for digital IN data. Digital IN block flag detection.
28	PE03	O	Positive		n-bit slot signal for digital IN data

* n=16, that is, 16-bit slot.
n=25 in PCM-1610.

Figure 6-23



This timing chart is for 25-bit - 32-bit slot conversion. Other slot conversion is also possible.

Figure 6-24

6.4.6 CX23070 APPLICATION

Basically, the CX23070 is for 25-slot to 32-slot converter. But it also allows 32-slot to 32-slot conversion or regeneration. This can be done by supplying 32-slot timing signals to DE02 and PE02 pins. In this case, input pin DE02 for digital OUT data must be supplied with 32-slot data.

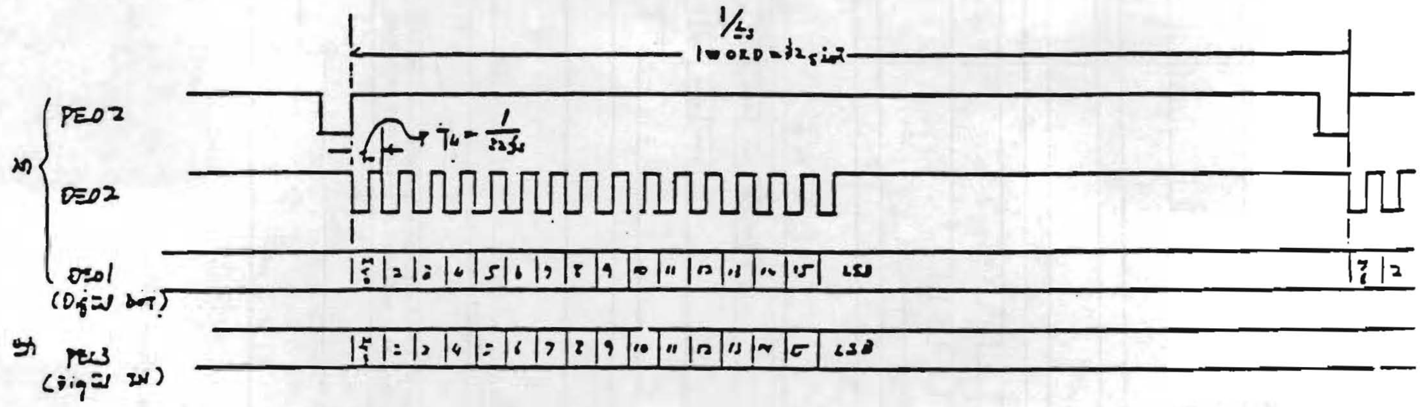


Figure 6-25 Slot Timing

6.5 DEC-15 BOARD

6.5.1 Major Functions

6.5.1.1 Sync Separator

- Separates the transmitted digital composite signal into the sync and data components.

- Using the separated sync, it also generates a clock required to decode data.

6.5.1.2 Data Separator

- Sends data to the DEC-A block after performing a CRC check for data.
- Detects the emphasis signal in data.
- Determines the sampling frequency (fs).
- Sends the muting signal to the DEC-B block if sequential errors have occurred during monitoring of errors.

6.5.1.3 DEC-A Block

- Deinterleaves interleaved data.
- Stretches data to be clocked in the normal sampling intervals because data has been compressed and inserted into part of the video signal.
- Generates syndromes S21, S22, and S23.
- Generates the bit and word clocks from the master clock.

6.5.1.4 DEC-B Block

- Corrects errors in deinterleaved data by means of the CRC error byte (syndrome).
- Mutes data in the MUTE-3 mode if the external sync is out of lock, and in the MUTE-2 mode if errors are frequently detected during CRC check.

6.5.2 Sync Separator

6.5.2.1 Selecting the Composite Digital Signal

One of the digital composite signals fed from the decoder to input terminals A and B can be selected by the input A/B select switch on the front panel.

The switch turns the positions from A to B or vice versa during horizontal sync. If switching is done at any time in a frame, spikes or other types of noise can appear in the picture frame.

6.5.2.2 Sync Tip Clamp and Pedestal Clamp

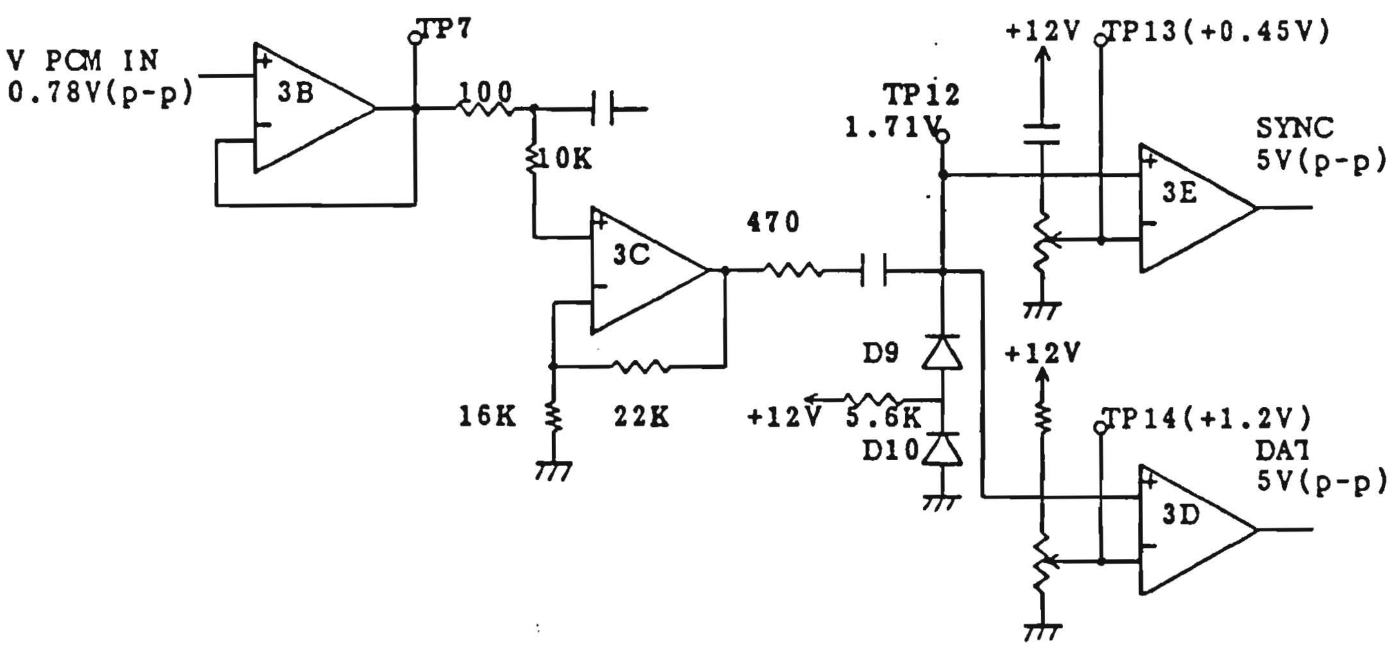


Figure 6-26 Sync Tip and Pedestal Clamp Circuit

The digital composite signal is amplified by approximately 7dB (2.2 times) in IC3C. The digital composite signal is tip-clamped by using D9 and D10 to sample the sync component. RV1 determines the threshold DC voltage and IC3E compares the digital composite signal with the threshold DC voltage to output the sync component. The sync component is sent to IC9K.

IC3D compares the digital composite signal with the threshold DC voltage to output the data component. The data component is sent to IC9K.

IC9K (CX23074) generates the pedestal clamp pulse (PCLP) by picking up the signal between the horizontal sync and data when the data and sync components are sent from IC3D and IC3E, respectively.

C13 is charged by driver Q3 while gate Q1 is opened by making the voltage at the gate of Q1 high. C13 is a capacitor for the integration circuit. The voltage across C13 is fed to IC2C during the 1H period. The pedestal of the digital composite signal is unchanged by this type of pedestal clamping.

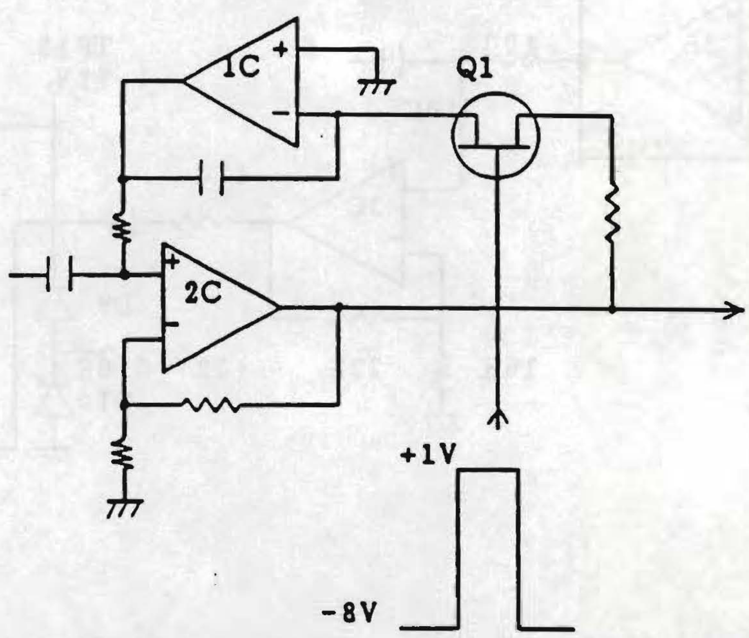


Figure 6-27 Pedestal Clamping

6.5.2.3 Separating the Sync From Data

The digital composite signal with its pedestal level fixed is fed to IC2E to sample the data component and to the PCDT terminal of the sync separator. IC1E samples the sync component, and the sync component is sent to the sync terminal of the sync separator. The signal at pin 9 of IC1E is fed to an integration circuit consisting OF R34 through R36, C19 and C20 to detect the vertical sync. The vertical sync is then fed to the VPLS terminal of IC9K.

The threshold voltage for sampling the digital composite signal (V PCM IN) is optimized by the automatic threshold level control circuit (ATC), then fed to IC1E and IC2E.

The ATC circuit consisting OF IC2M, IC3K, IC4K, IC2J, and IC2H detects the peak of the data component while comparing the data component with the pedestal level of the digital composite signal with its pedestal level fixed. Half the peak value is specified as the sampling level for data in IC1L, IC1K, and IC1J. The sampling level for the sync component is specified as (data sampling level) x (-0.8) in IC1H.

6.5.2.4 Sync Separator

The CX23074 is one of the LSI series (CX23071 to CX23074) used in the data playback system of the **PCM-1610** format digital audio processor. It extracts sync signals from playback signals on which PCM data from the recorder is superimposed and generates various clock signals necessary for the playback system.

This LSI consists of the following four blocks:

- .H sync detection block
- .V sync detection block
- .Control clock pulse generation block
- .Pedestal clamp pulse generation block

Each block is protected in various ways to prevent incorrect sync and clock signals from being generated. These blocks are synchronized with master clock CKMS.

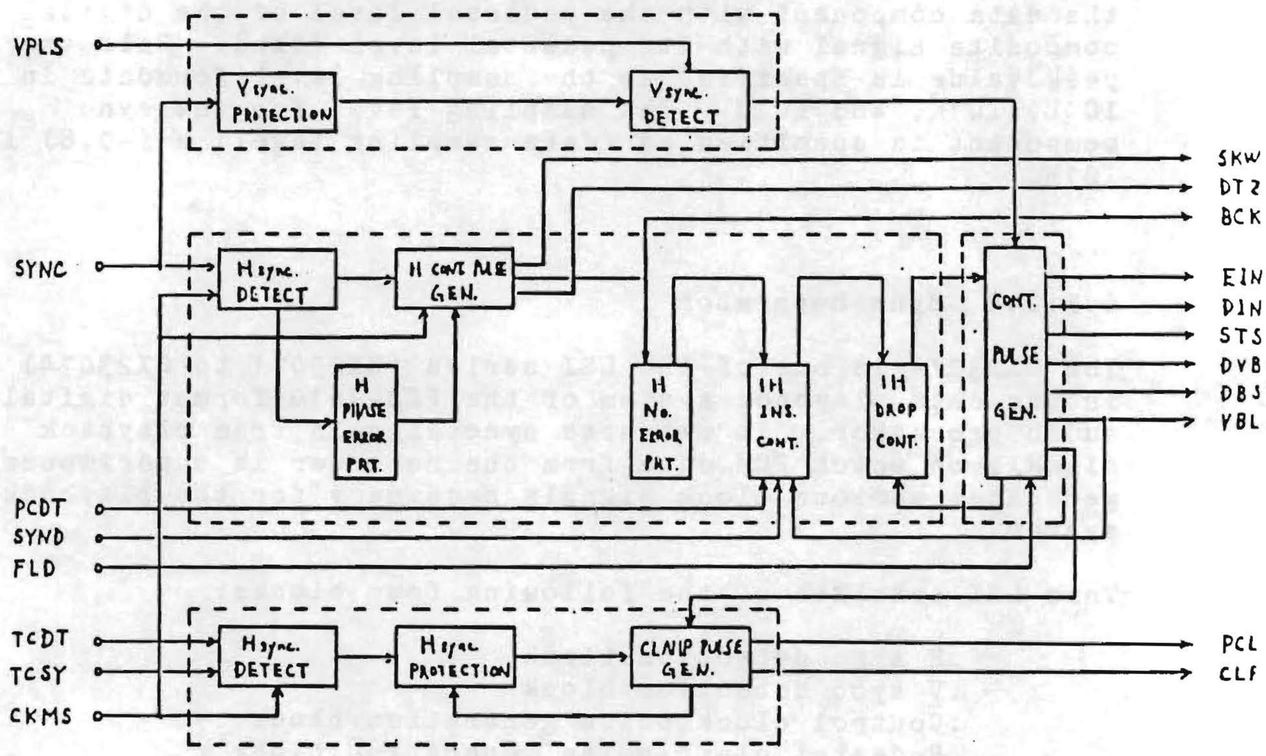
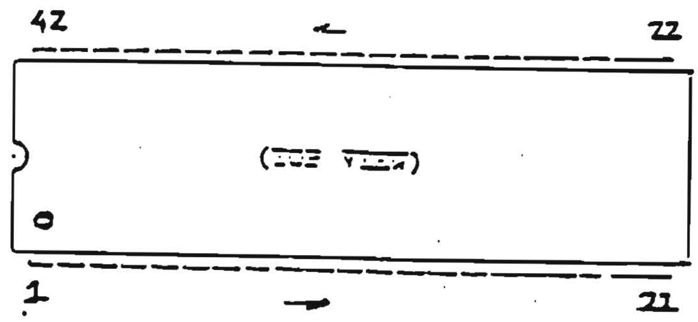


Figure 6-28 CX23074 Block Diagram

PIN ASSIGNMENT (DIP-42)



Pin Numbers and Names

PIN NO.	I/O	Pin name	PIN NO.	I/O	Pin name	PIN NO.	I/O	Pin name
1	I	TEST	15	O	VBLK	29	O	VPRT
2	I	RST1	16	O	DBSY	30	O	SKWB
3	I	RST2	17	O	DVBL	31	O	BCKP
4	O	HLD	18	O	VBCK	32	—	VDD
5	O	HPPR	19	O	INTB	33	O	DTZN
6	O	PBE	20	O	STSC	34	O	TCLP
7	O	HJPR	21	I	FLD	35	O	CLPF
8	O	HDRP	22	I	SYND	36	O	PCLP
9	O	CKDM	23	O	DINT	37	I	TCDT
10	I	CKMS	24	O	EINT	38	I	TCSY
11	—	VSS	25	O	VRST	39	I	PRSW
12	O	HWDW	26	O	INTV	40	I	VPLS
13	O	HPRT	27	O	PBV	41	I	PCDT
14	O	INTH	28	O	PBV6	42	I	SYNC

Figure 6-29 CX23074 Pin-out

No.	Names	I/O	Polarity	Waveform	Description
1	TEST	I	Posi	Direct current	Test mode set pin. H in test mode. Usually connected to ground.
2	RST1	I	Posi	Direct current	Test mode reset pin. When H, test mode is off. Usually connected to ground.
3	RST2	I	Posi	Direct current	Test mode reset pin. When H, test mode is off. Usually connected. to ground.
4	HLD	O	Nega	H	Indicates back edge of H sync. This signal is protected and has same pulse width as master clock. Check pin.
5	HPPR	O	Nega	H	Output signal for H sync detection and protection. During HPPR=H, H sync is not detected. Check pin.
6	PBH	O	Nega	H	Detects back edge of H sync. This signal is protected by HPPR and it is the same as HLD so long as no error occurs. Check pin.
7	HJPR	O	Posi	H	Output signal for H sync phase jump protection. During HJPR=L, H sync is not detected. This signal makes 2H protection when there is change in H sync phase. HLD is protected by this signal. It has opposite polarity with respect to DTZM so long as no error occurs. Check pin.
8	HDRP	O	Nega	V	Drops H sync 1H. This signal is controlled during the V period and H. so long as no error occurs. Check pin.
9	CKBM	O			Outputs CKMS/2 clock signals. Check pin.
10	CKMS	I	Nega		Master clock input pin. Reference clock for pulse decay. fs = 44.056kHz: 14.31818MHz fs = 44.1kHz: 14.3325MHz
11	VSS	—			GND
12	HWDW	O	Posi	H	H sync gate signal for pedestal clamp pulse generation block. H when H sync has predetermined length. Check pin.
13	HPRT	O	Nega	H	H sync detection and protection signal for pedestal clamp pulse generation block. During HPRT=H, H sync is not detected. Check pin.
14	INTH	O	Nega	H	Clock signal for control clock pulse generation block. Same as BCKP. This signal is protected by many signals. Check pin.
15	VBLK	O	Nega	V	Indicates V blanking (non-data zone). Synchronized with leading edge of BCKP.
16	DBSY	O	Nega	V	DVBL + BCKP signal
17	DVBL	O	Nega	V	1H-delayed VBLK signal. Synchronized with BCKP.
18	VBCK	O	Nega	V	Indicates portion of DVBL following back edge of V sync. Check pin.
19	INTB	O	Nega	1FH	Indicates interleave block. Check pin.
20	STSC	O	Nega	V	Output signal sent to CX23073 to check start point of data zone during the V period.
21	FLD	I	O/E	O E	Odd/even field separation input signal for frame synchronization. FLD=H indicates odd field.
22	SYND	I	Nega	V	Signal sent by CX23073 to respond to OK syndrome STSC. Indicates start point of data zone (CRCC check.)
23	DINT	O	Nega	1FH	Indicates start of interleave block. This signal has the same pulse width as BCKP.
24	EINT	O	Nega	1FH	Indicates start of interleave block. This signal has 1H-pulse width and is delayed 1H from INTB.
25	VRST	O	Nega	V	Indicates back edge of V sync. Reference reset signal for control clock pulse generation block. Check pin.

Figure 6-30

No.	Name	I/O	Polarity	Waveform	Description
26	INTV	O	Nega	V	Reset signal used to form VRST. This signal is periodically output by an internal counter. Check pin.
27	PBV	O	Nega	V	Back edge of V sync signal detected when playback V sync is input and used to form VRST. Usually, synchronized with INTV in phase. Check pin.
28	PBV6	O	Nega	V	Sixth pulse of playback V sync. Check pin.
29	VPRT	O	Posi	V	Indicates V sync for V sync detection and protection. Check pin.
30	SKWB	O	Nega	H	Indictates skew bit position (129th bit of 1H). This signal has 1-bit pulse width.
31	BCKP	O	Nega	H	Back porch signal from back edge of H sync to data start point.
32	VDD	–			+ 5 V
33	DTZN	O	Posi	H	Indicates data zone of 1H
34	TCLP	O	Nega	H	Indicates center of sync tip. Reference signal.
35	CLPF	O	Nega		This signal goes L when no sync is input for 4V to turn clamp off. Turns pedestal clamp off when TCSY (composite sync) is not input.
36	PCLP	O	Nega	H	Pedestal clamp pulse signal
37	TCDT	I	Nega	H	Input data detected by external sync tip clamp block. This signal controls pedestal clamp pulse generation block.
38	TCSY	I	Nega	H	Input composite sync detected by external sync tip clamp block. This signal controls pedestal clamp pulse generation block.
39	PRSW	I	Nega	Direct current	Input pin for testing. Usually fixed at H.
40	VPLS	I	Nega	V	External V sync integration signal. To input this signal, sixth pulse of V sync must be L. This signal controls V sync detection block.
41	PCDT	I	Nega	H	Input data detected by external pedestal clamp block. This signal controls H sync detection block's protection circuit.
42	SYNC	I	Nega	H	Input composite sync detected by external pedestal clamp block and used for H sync detection

Figure 6-31

2-6. TIMING CHARTS

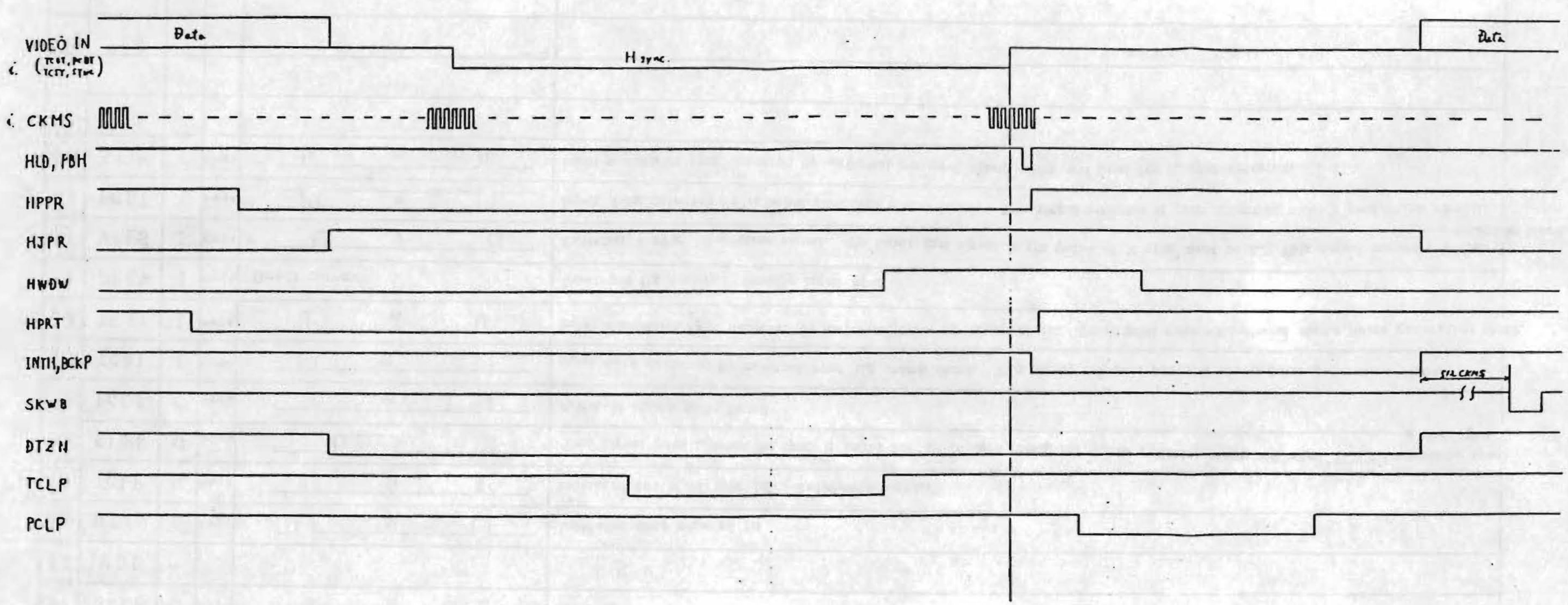


Figure 6-32

Timing chart (2)

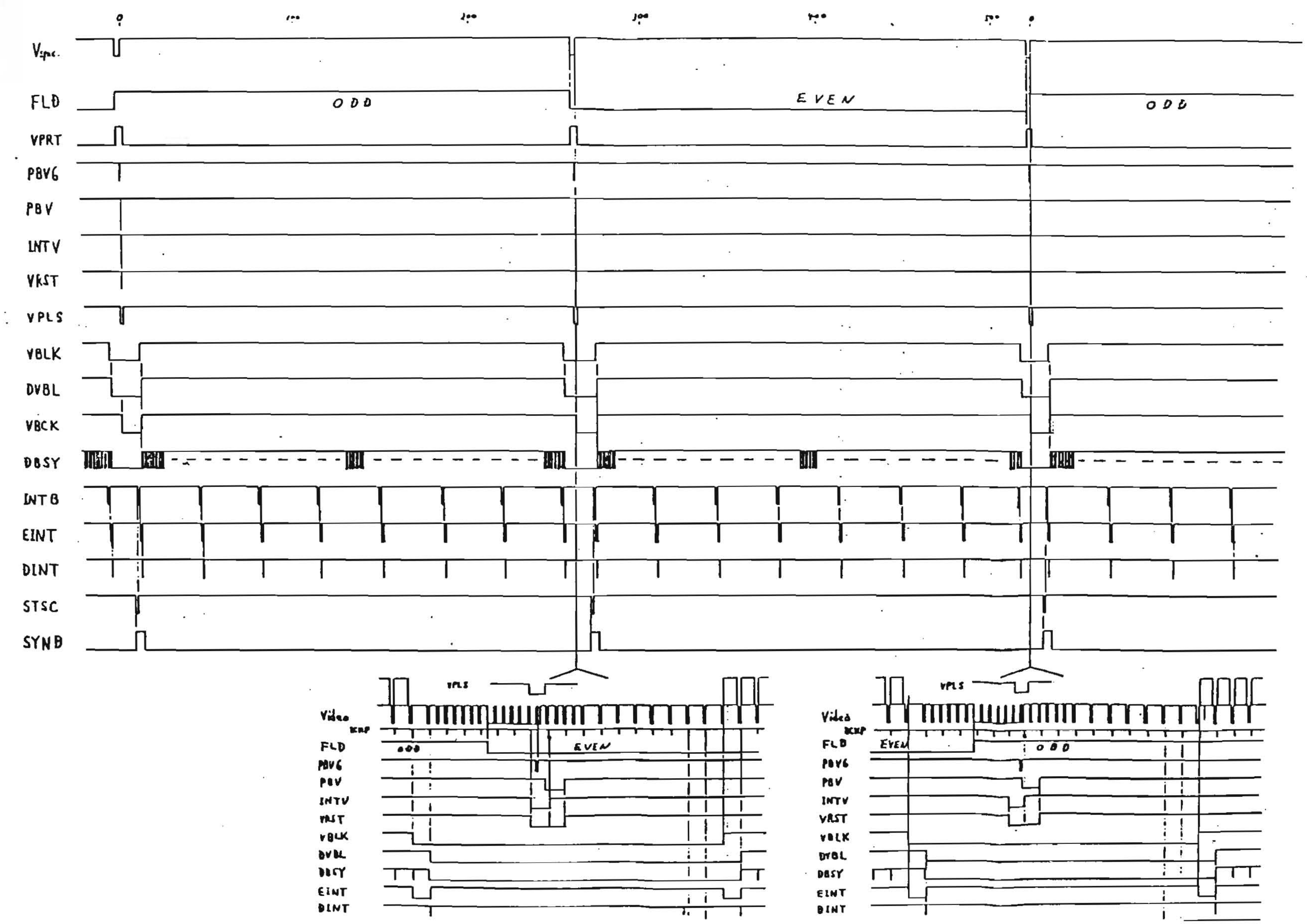


Figure 6-33

INTER-LSI CONNECTION

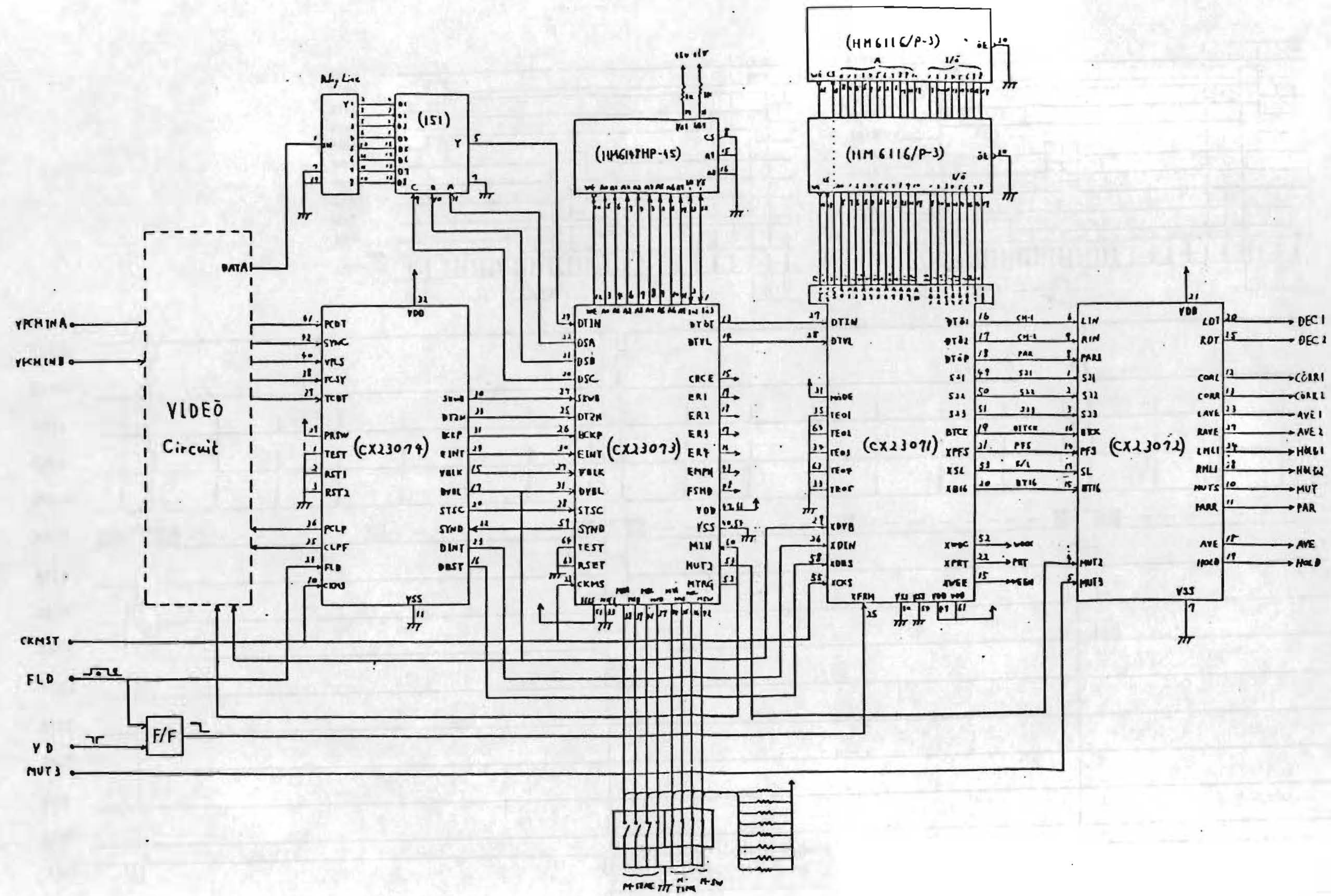


Figure 6-34

6.5.3 Data Separator

6.5.3.1 Major Functions

1. Data Handling
   Divides data separated by sync separator into four phases per bit, performs a CRC check, and automatically adjusts the delay of input data to the result of the CRC check.

2. Emphasis
   Detects the emphasis signal in data.

3. Sampling Frequency
   Detects the FS ID signal in data.

4. Muting
   Sends the muting signal if consecutive data bits are erroneous.

6.5.3.2 Circuit Descriptions

1. Data Handling
   Data separated by the sync separator can have jitter, and dropouts can occur. Data passed through the delay device (ZT35-200) is sent to the DTIN terminal of CX23073. Data clocked at four times the bit clock rate is input to the RAM in four phases per bit. One data bit is input to the RAM four times and stored in the RAM. At the same time, a CRC check is made for date to detect errors. The proper delay time is selected to sample the optimum data bits.

   The data selector selects one (either phase 2 or phase 3) of the four phases corresponding to the result of the CKL check and reads it from the RAM. The timing between recording and reading operations for the RAM is 1H.

   The RAM content stored before 1H in the same address is read out and the next data is recorded (refer to the timing chart in the CX23073).

2. Emphasis
   The emphasis information is inserted into the video signal at bit 129 of the first H in the interleaved signal. When data is 0, the emphasis signal is set to on. When data is 1, the emphasis signal is set to off. The emphasis signal is output to the FET switch on the DA-15 board to control the deemphasis circuit.

3. Sampling Frequency

The sampling frequency can be detected in second H of the interleaved signal. When the sampling frequency detection signal is high, the sampling frequency is 44.056kHz. When the sampling frequency detection signal is low, the sampling frequency is 44.1kHz and the FS ID signal is output to light the LED on the front panel.

4. Muting

If consecutive errors are detected by the CRC check, noise can occur in the playback signal if the signal is not muted. When switches S2 through S4 are properly selected by the user, the signal cannot be muted. The time during which the signal is muted can be selected by S201 through S203.

6.5.4 DEC-A (CX23071)

6.5.4.1 Major Functions

.Data interleaved from the control and data signals sent from sync separator CX23074 and data separator CX23073 is stretched to convert it into that in the digital sampling intervals. The signals arranged in the order of CH-1, CH-2 and PARITY are output (the LSB is sent first).

.A CRC check for input data is made to generate sydromes S21, S12, and S23, corresponding to the errors detected in input data by the CRC check.

.The PITCK and WDCK signals required for 25 slots are generated.

6.5.4.2 Circuit Descriptions

1. Deinterleaving

Data sent from data separator CX23073 is converted into parallel data blocks every two bits by using the serial-to parallel converter, then stored in RAM HM6148. At that time, a CRC check for each block of data is made, and bit 16 of the OF CRC data to be sent to the RAM goes high if any error has occurred.

Data CH-1, CH-2 and PARITY, without their time axis compressed, can be obtained by using four RAM chips each having a capacity of 35H (or 840 bytes). If block 1 specifying single interleaving is written in RAM, data of block 3 can be read out of the RAM.

If block 2 is written into RAM, data of block 4 can be read out of the RAM.

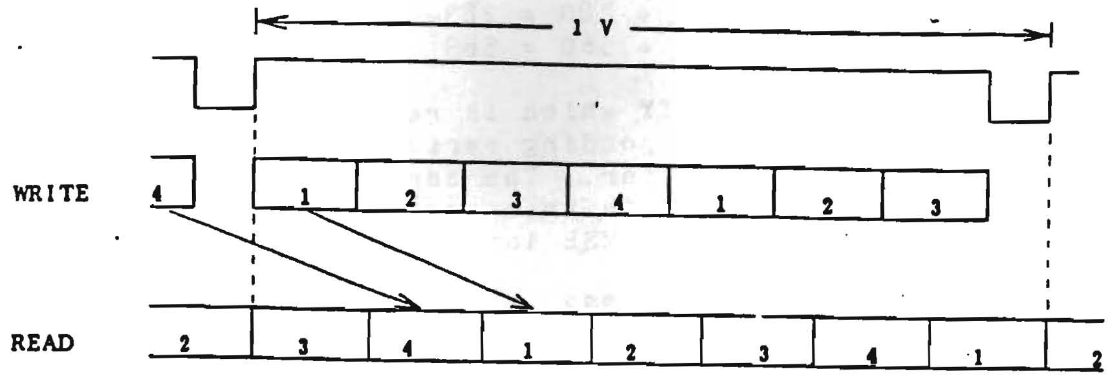


Figure 6-35 RAM Read/Write Arrangement

If the following data format is assumed read operations cannot directly be performed and modification is required:

```
CH-1      L1, L2, L3, L4...........L105
CH-2      R1, R2, R3, R4...........R105
PARITY    P1, P2, P3, P4...........P105
```

An address is assigned in eight data bits. A counter incrementing from 000 to 999 and the 0/280/560 count generator are utilized to specify the read address.

R1 0, 1	L2 2, 3	R3 4, 5	C1 6, 7	L4 8, 9	R5 10, 11	L6 12, 13	---	R103	L104	R105	C103 278,279
P1 280,281	P2	P3	C3	P4	P5	P6	---				C105
L1 560, 561	R2	L3	C2	R4	L5	R6	---				C104 838,839

Figure 6-36 Interleaving of the Data

When the counter contents and 0, 280, or 560 are added together, address range 0 through 279, 280 through 559, or 560 through 839 can be specified.

L1 = 0 + 560 = 560, 1 + 560 = 561
P1 = 0 + 280 = 280, 1 + 280 = 281
R1 = 0 + 0 = 0, 1 + 0 = 1

L2 = 2 + 0 = 2, 3 + 0 = 3
P2 = 2 + 280 = 282, 3 + 280 = 283
R2 = 2 + 560 = 562, 3 + 560 = 563

Data CH-1, CH-2, or PARITY which is read out of the RAMs, is converted into the corresponding serial signal by using the parallel-to-serial converter. The serial data is synchronized with the WDCK signal. It is then sent to DEC-B (CX23072) with the LSB first and the MSB last.

2. Syndromes S21, S22, and S23

S21: When high, errors have occured in data CH-1.
S22: When high, errors have occured in data CH-2.
S23: When high, errors have occured in parity data.

The syndromes can be obtained by the operations below. Three CRC bits are read out of the RAM in each sample during three sampling periods, and they are stored in the register. The register contents S21, S22, and S23 are output every word.

6.5.5 DECODER-B (CX23072)

1. Digital data obtained from the deinterleaving circuit (CX23071) and the syndrome data are processed to correct errors if necessary.

2. Data is muted if the external sync goes out (MUTE-3) or if errors have occurred in the CRC check (MUTE-2).

6.6 DA-15 CIRCUIT DESCRIPTION

6.6.1 Major Functions

1. A digital signal fed from the DEC board or external circuit to the DA IN terminal is converted into the corresponding analog signal and sent to the ANALOG OUT terminal.

2. An analog signal fed from either the AD board or D/A converter is selected and the selected signal is sent to the headphone monitor.

6.6.2 Circuit Description

6.6.2.1 Digital Circuit

1. Digital filter

IC15 is used to double the digital signal sampling frequency (fs) and can process two-channel data. Processed data is input to pin 9 (DIN) of IC101 and IC201. This is oversampling since the timing clock rate is doubled.

WCLK, LRCK, and BCLK, each of which has a clock rate twice subcarrier, are sent from pin 21 (02) pin 22 (03), and pin 20 (01), respectively. Data is sent from pin 19 (D7). When LRCK at pin 22 is high, data in channel 1 is selected. When LRCK at pin 22 is low, data in channel 2 is selected.

2. Phase comparator and VCO

IC16 and IC17 are provided to generate the clock for IC15. The clock at a frequency of 384 times the sampling rate is sent from IC16. If the sampling rate is 44.1kHz, this frequency is given by 16.9344MHz. Phase comparator IC17 compares the clock signal (at TP7) generated from WDCK1 with the other clock signal (at TP8) generated by dividing the output signal of IC16.

3. Reference clock

The timing to indicate the end of inputting 16-bit data to the DA-15 board is generated by IC14. When WDCK1 goes low, IC14 counts the number of BTCK1 pulses. When the 16th BTCK1 pulse is counted, CO at pin 15 goes high.

4. Frequency divider

IC15 divides the frequency of the output of IC16 by two, and the output of IC15 appears at pin 4 (CDCK). The output signal has a clock rate of 192 times the color subcarrier. The output of IC15 is fed to IC2 and IC9 where the clock rate is counted down to the color subcarrier. The final output signal is fed from pin 6 of IC9 to pin 6 of IC17.

5. Data Selector

IC3 selects data to be input to the DA-15 board. IC4 and IC5 provide two functions. One is to arrange data in channels 1 and 2 into one serial signal. The other is to provide an offset for the low-order fourth bit of data. The offset is provided by using ADD1 through ADD4 at pins 5 through 8 of IC4 and IC5. Only ADD4 is high, and "1" is added to the low-order fourth bit of data at a timing of CLK1.

If the following data format is assumed read operations cannot directly be performed and modification is required:

CH-1	L1, L2, L3, L4...........L105
CH-2	R1, R2, R3, R4...........R105
PARITY	P1, P2, P3, P4...........P105

An address is assigned in eight data bits. A counter incrementing from 000 to 999 and the 0/280/560 count generator are utilized to specify the read address.

6. **Timing control**

This circuit is used to generate the clocks for IC4 and IC5 as well as the clock for the digital filter.

Offset data sent from IC4 and IC5 is latched by the internal register at the timing given from pin 11 of IC6. The gate pulse to send data to IC4 and IC5 is fed from pin 10 of IC11.

The clock signal for IC4 and IC5 is synchronized with the clock signal at pin 6 of IC9 when the pulse signal at pin 5 of IC12 is sent to this circuit.

6.6.2.2 **D/A Converter**

1. **D/A converter**

IC101 (IC202) is an integral D/A converter.
Q101 (Q201) is the constant current source which defines the integration current of IC101 (IC201).

$$ISET = \frac{5V}{8.2 + 0.47\ (k\Omega)} = 0.58\ (mA)$$

$$I_o = 4.ISET = 2.3mA$$

$$i_o = \frac{1}{64}.ISET = 9.1uA$$

I_o, i_o are obtained by integrating the high-order and low-order eight bits of 16-bit data. When D/A conversion is accomplished by data of full-scale value the voltage across C110 and C111 (C210 and C211) is given by the following:

$$Vomax = \frac{(Io+io)X(2^8-1)}{C\ X\ fCLK} = \frac{(2.3+9.1)x255x10^{-3}}{1500x39.9347x10^{-6}} = 9.8(V)$$

Data in the left and right channels is converted into the corresponding oversampled digital data using IC101 (IC201) operating at a clock rate of 88.2kHz. These signals are sampled by IC104 and IC105 and added using IC106 (IC206) to generate a pulse train sampled at 88.2kHz.

2. **Oscillator**

This circuit is used to generate a count clock for IC101 (IC201). This frequency tends to cause a beat (notified phase relationship) when it is mixed with the sampling frequency. The count clock frequency is set so that the beat frequency lies above the audio frequency. The count clock frequency is 39.9347MHz, and the beat frequency is 16kHz or above.

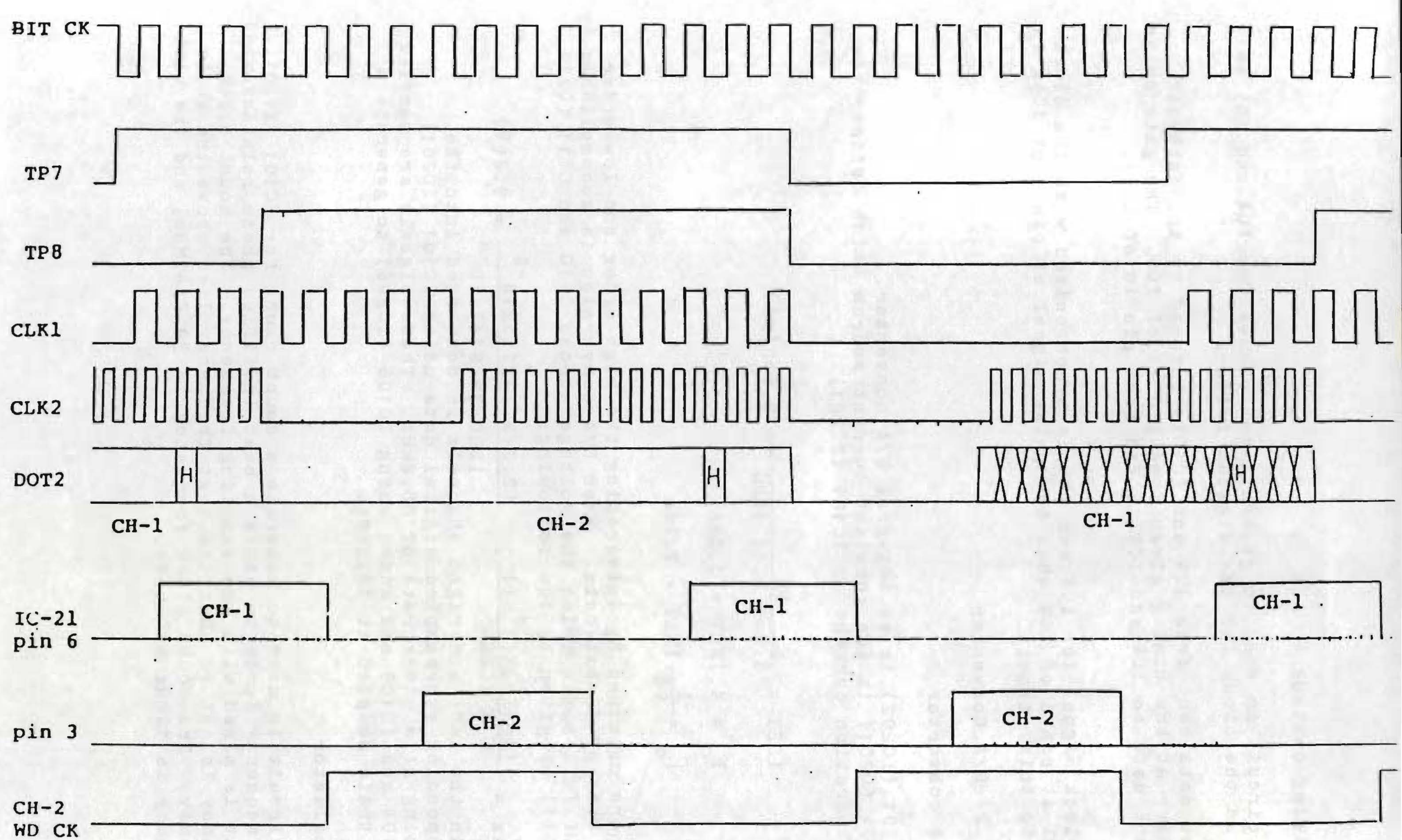

BIT CK
TP7
TP8
CLK1
CLK2
DOT2
H
H
H
CH-1
CH-2
CH-1
IC-21
pin 6
CH-1
CH-1
CH-1
pin 3
CH-2
CH-2
CH-2
WD CK

Figure 6-37

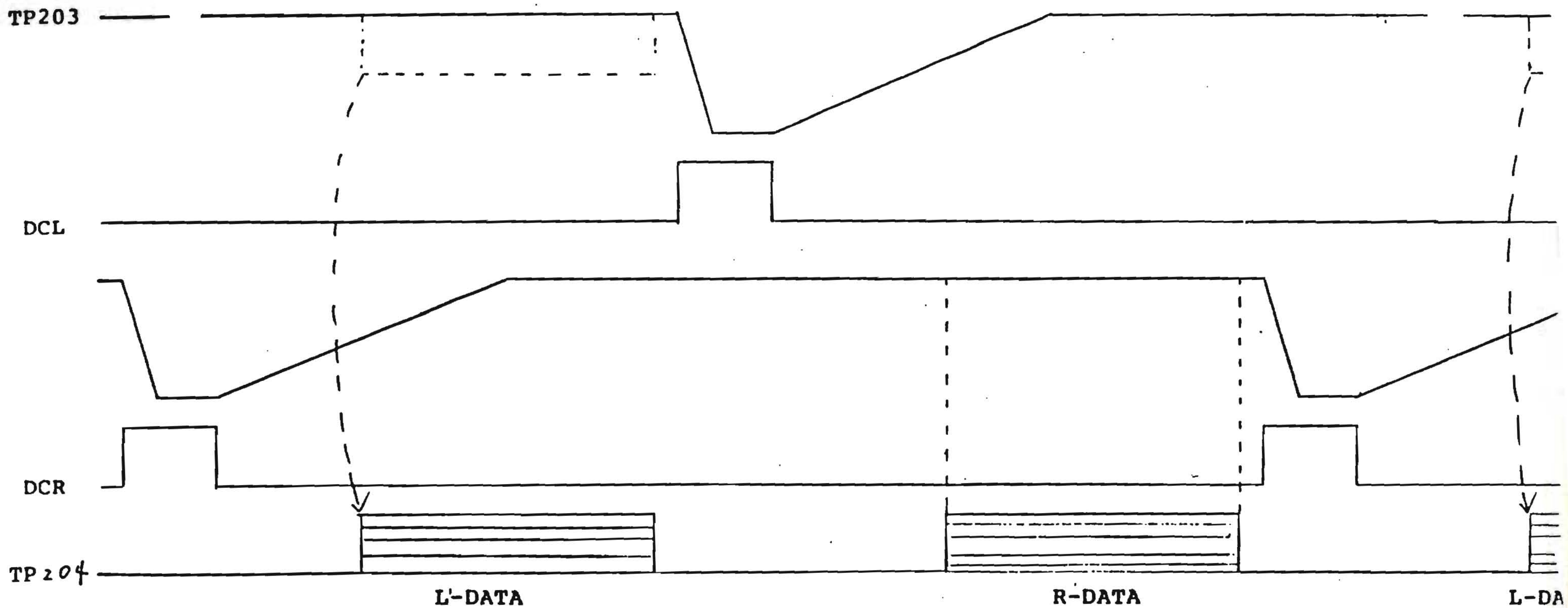


Figure 6-38

6.6.2.3 Analog Circuit

1. Low-pass filter

This low-pass filter in AFL101 (AFL201) has a cutoff frequency which corresponds to the sampling frequency at 88.2kHz. This has attenuations of 3dB at 24kHz and 86dB at 68kHz. The null point appears at 44.1kHz.

2. De-emphasis circuit

The de-emphasis circuit has a transfer function inverse to that of the emphasis circuit on the AD-23 board.

3. Level control

RV101 (RV201) on the front panel can be adjusted to control the gain in a range of 12dB or more.

C169 (C269) is used to make the frequency response flat. Generally, the frequency response is considered to be acceptable when there is approximately 0.5dB lower level than the reference at 20kHz.

IC109 (IC209) is used to cancel the DC component of the signal.

4. Line amplifier

IC112 and IC113 (IC212 and IC213) constitute a balanced line amplifier. If the COLD lead of the line amplifier is connected to ground, the output becomes unbalanced.

IC109 (IC209) is incorporated to stabilize the balanced output.

5. Headphone circuit

Headphone monitor signals are provided in the REC and PB channels. IC110 (IC210) is used to select either the REC or PB signal. The selected signal if fed to the level adjuster on the front panel through R129 (R229). The monitor signal attenuated by the level adjuster is fed again to the D/A board. This signal then appears at the headphone terminal.

6.7 MT-16 CIRCUIT DESCRIPTION

The MT-16 circuit controls the level meter display in accordance with the input digital data levels. Operation of this circuit is based on the program built into the CPU (uPD8749HD). One of the three types of input data (DT DA, DT ME, and RAW DT) are selected at the data selector. The data selector can be controlled with the monitor select (REC/PB) switch and the RAW (DUB/OFF/EDT) switch on the optional RAR-1 board. The RAW DT data, DT ME data and DT DA data are selected respectively in the DUB mode (DUB/EDT = 0), REC mode (REC/PB = 0) and PB mode (REC/PB = 1). The selected data undergo the processing procedure, which is controlled by the control clock generator, and then go in to the CPU. In more detail, both channels of data are first converted into 16-bit parallel signals in the serial/parallel convertor circuit. The signals expressed using the 2's complement notation are then converted into absolute values in the subsequent absolute value convertor circuit. Next, at the comparator, these values are compared with the output data (COMPARISON DATA) from the following latch circuit, and if their level is equal to or higher than the comparison data level, they are latched into the latch circuit.

Operation hereafter is placed under the control of the CPU that operates on the basis of approximately 11MHz clock: The data passes through the bus buffer and read into the CPU, with 8 bits at a time. Once the data is read into the CPU, a reset signal is output from the reset pulse circuit, cleaning the latch circuit and resetting the COMPARISON DATA to zero. Since the CPU data read cycle is 3 msec., if new input data (having a greater level than the latch circuit's data level) arrives before the latch circuit has been cleared (ie, before the previous data has been read into the CPU), the old data in the latch circuit will be replaced by the new.

External switch information (SCALE, PEAK, HR1 - 6) and internal switch information are read into the CPU from the switch encoder and the mode selector respectivly. The CPU processes data based on the information obtained from these sources. The 64 CPU controlled meter LEDs (32 per each channel) are divided into 4 segments, each consisting of 16 LEDs. In order to make them light up and go out dynamically at 6msec. intervals, the CPU data are first led by the segment driver to MA 1-4 (designed to control the anodes for the 4 segments) and then to the I/O expander port. They are then output from the digit driver as MD 0 - 15 for controlling 16 individual LED cathodes within each segment.

There is also a over level detector circuit which counts how many full-scale data have been input in succession. The OVER display is activated by the output from this detector circuit. Futhermore, the 25-slot word clock, bit clock and data are sent from the RS-422 driver to the STATUS connector as a remote signal (R WDCK, R BITCK, R DT1 and R DT2).

6.8 PS-81 BOARD

The PS-81 board generates the voltages necessary for each circuit and generates a muting signal to prevent noise when power is turned on or off.

The generated voltages are described below.

VOLTAGE	(CAPACITY)	APPLICATION
+5V	(4A)	Logic circuit
+5V-M	(1.5A)	Meter driving
+12V	(0.5A)	Video circuit
-12V	(0.5A)	Video circuit
-8V	(0.6A)	AD/DA circuit
+22V	(1.5A)	Analog circuit
-22V	(1.5A)	Analog circuit

For voltages other than +/-22V, the regulated voltage is obtained using a regulator IC. The +/-22V is obtained by a regulated power supply circuit employing individual transistors. The +5V (4A) and +/-22V can be fine-tuned using RV1 and RV2. The -22V is set by adjusting the +22V because it tracks the +22V. Since other voltages depend on individual IC characteristics, they cannot be adjusted.

The above power supplies have a short-circuit protection function. Therefore, when the voltage output is short-circuited, the power supply is turned off. After the +5V (4A) and +/-22V supplies are turned off, they are not reset under the shut-down condition. When power is turned on again 30 seconds after being turned off, the supplies are reset to the normal condition. For other voltages, the protection function is activated only during the short-circuit; they are reset on removal of the short-circuit.

Muting signal MUT 1 which prevents noise during the power on/off sequence is generated using an integrator circuit (consisting of R15, C25, D21, etc.) or a circuit consisting of photocoupler PC1. When power is turned on, the muting function is activated for approximately three to four seconds. When power is turned off, muting is again activated.

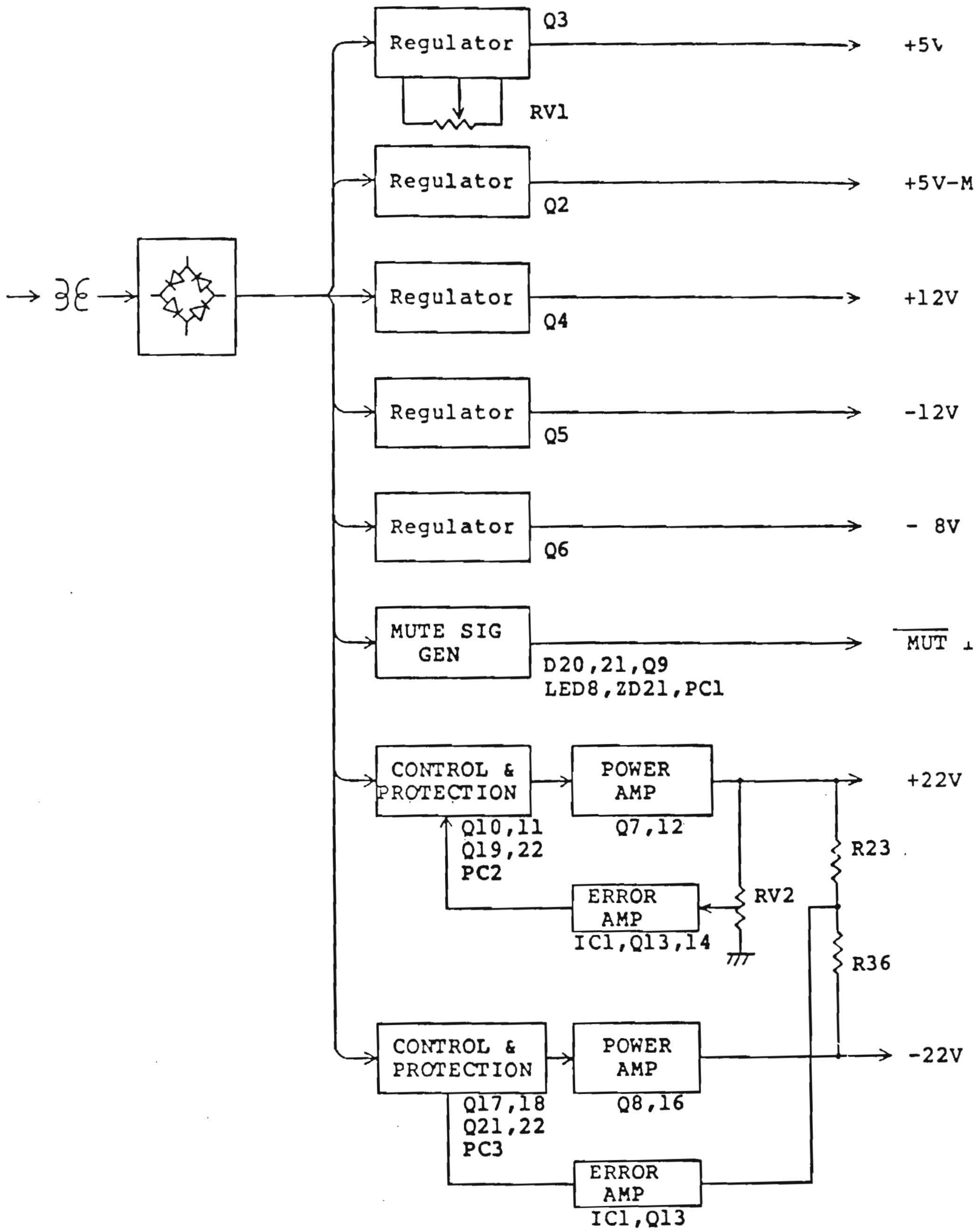

Regulator
Q3
+5V
RV1
Regulator
Q2
+5V-M
Regulator
Q4
+12V
Regulator
Q5
-12V
Regulator
Q6
- 8V
MUTE SIG GEN
D20,21,Q9
LED8,ZD21,PC1
MUT
CONTROL & PROTECTION
Q10,11
Q19,22
PC2
POWER AMP
Q7,12
+22V
R23
ERROR AMP
IC1,Q13,14
RV2
R36
CONTROL & PROTECTION
Q17,18
Q21,22
PC3
POWER AMP
Q8,16
-22V
ERROR AMP
IC1,Q13

Figure 6-39

6.9 CX23073 DATA SEPARATOR

In the data playback system of the **PC-1610** format digital processor, the CX23073 performs CRCC error check and synchronization processing on PCM data in playback video signals to extract data, emphasis information, and sampling frequency information, and generates error and muting signals.

This LSI consists of the following blocks:

. Control pulse generation block

. Error checking block (CRC-CCITT: $X^{16} + X^{12} + X^{5} + 1$)

. Data selection block

. Skew bit extraction block

. Muting signal generation block

. Data delay control block

The control pulse generation block generates various control pulses and also generates address signals for external memory 1H delay. The error checking block checks four-phase data (which was read, using four-phase clock for each one bit of data) for errors and generates error signals based on error checking results. The data selection block reads one phase of data (second or third phase of data) from external memory according to error checking results and outputs the data after a 1H delay due to memory read/write operations. The skew bit extraction block extracts skew bits (129th bits of 1Hs) from each interleave block. The extracted bits are of the first 1H providing emphasis information and of the second 2H providing sampling frequency information, and of the third and fourth 1Hs which are not defined. The muting signal generation block generates muting signals, which depends on the continuity of error signals. A level of sensitivity causing muting, muting time, and muting-on/off are controlled by an external switch. The data delay control block receives four-phase error signals from the error checking block and generates data phase advance/delay control signals to enable data to be extracted correctly.

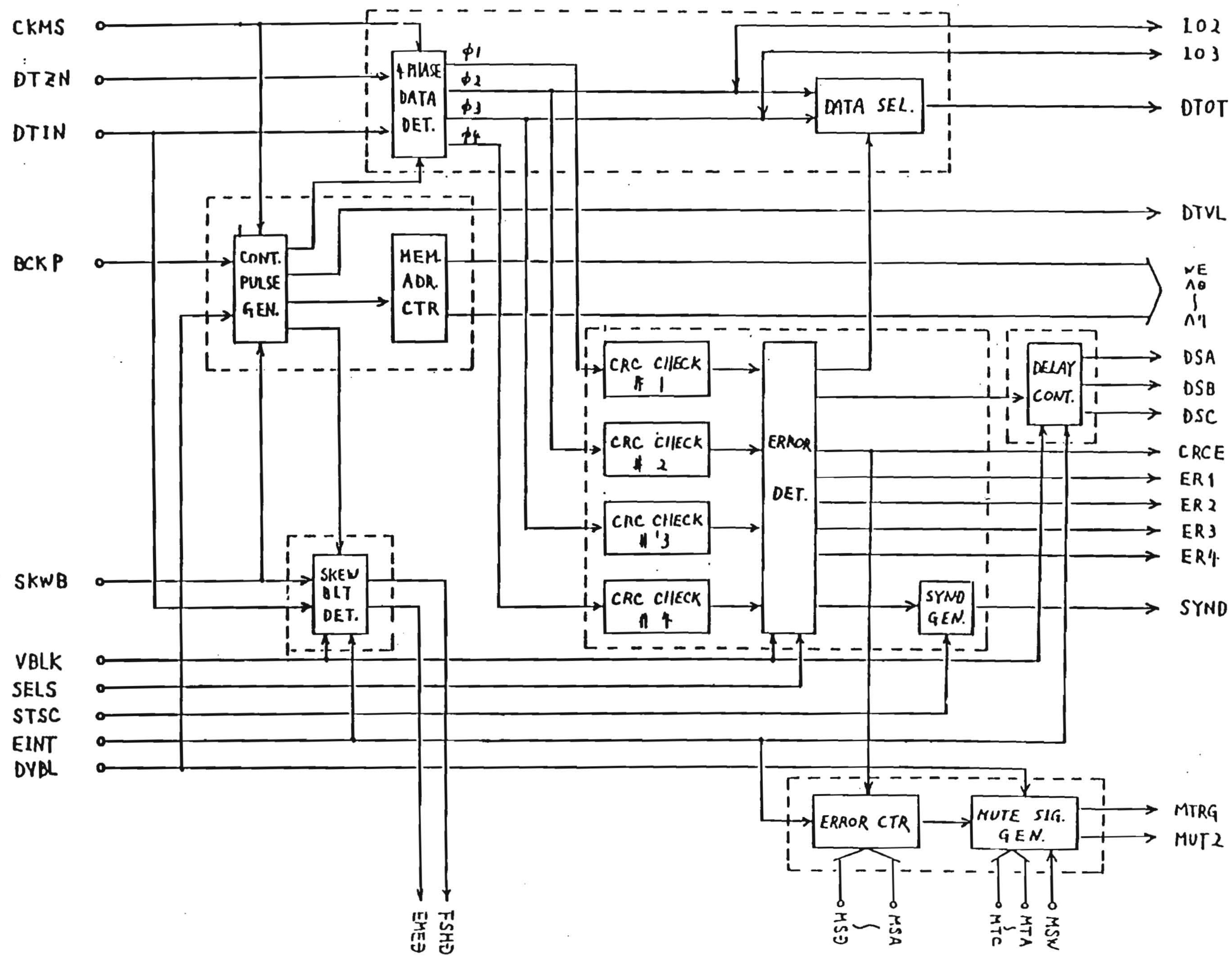
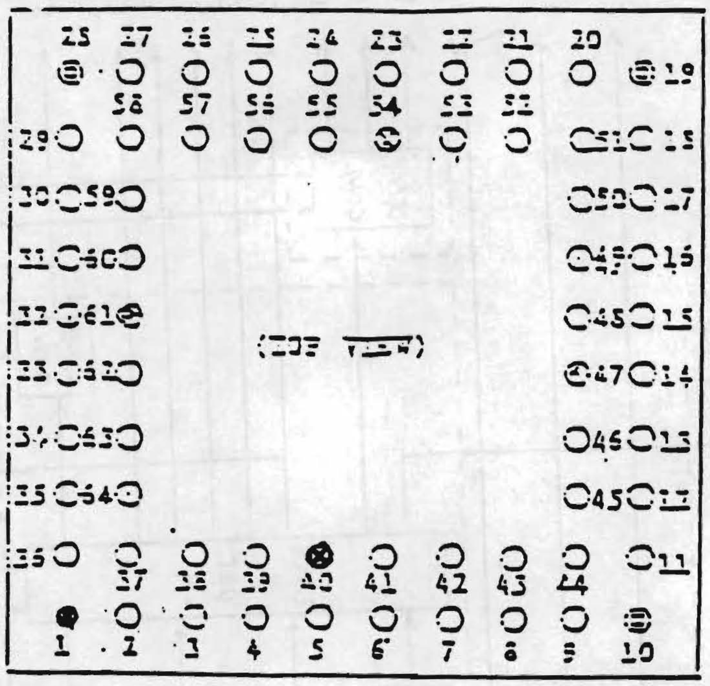


Figure 6-40 CX23073 Block Diagram

PIN ASSIGNMENT



Pin Numbers and Names.

PIN NO.	I/O	Pin name	PIN NO.	I/O	Pin name	PIN NO.	I/O	Pin name	PIN NO.	I/O	Pin name
1	I/O	IO3	17	O	ER3	33	I	MSEL	49	O	DTCK
2	I/O	IO2	18	O	ER2	34	I	MTA	50	O	SELO
3	O	A0	19	O	ER1	35	I	MTB	51	I	SELS
4	O	A1	20	O	DSC	36	I	MTC	52	O	MTRG
5	–	N.C	21	O	DSB	37	I	MSD	53	O	MUT2
6	O	A2	22	O	DSA	38	I	MSA	54	–	VSS
7	O	A3	23	I	CKMS	39	I	MSB	55	O	CRCK
8	O	A4	24	I	DTIN	40	–	VSS	56	O	DTAD
9	O	A5	25	I	DTZN	41	I	MSC	57	O	DTDL
10	O	A6	26	I	BCXP	42	I	MSW	58	O	SKWC
11	O	A7	27	I	SKWB	43	O	EMPN	59	O	SYXD
12	O	WE	28	I	STSC	44	O	FSID	60	I	MIK
13	O	DTOT	29	I	VBLK	45	O	SKW3	61	–	VDD
14	O	DTYL	30	I	EINT	46	O	SKW4	62	–	N.C
15	O	CRCE	31	I	DVBL	47	–	VDD	63	I	RSET
16	O	ER4	32	–	N.C	48	O	FSND	64	I	TEST

Figure 6-41 CX23073 Pin-out

PIN DESCRIPTION

No.	Name	I/O	Polarity	Waveform	Description
1	IO3	I/O	P		External memory data I/O pin. 3rd phase of data for DTIN. Input data is delayed 1H.
2	IO2	I/O	P		External memory data I/O pin. 2nd phase of data for DTIN. Input data is delayed 1H.
3	A0	O	P		External memory address signal (lowest order bit). An address consists of eight bits from A0 to A7.
4	A1	O	P		〃
5	NC	—			
6	A2	O	P		External memory address signal
7	A3	O	P		〃
8	A4	O	P		〃
9	A5	O	P		〃
10	A6	O	P		〃
11	A7	O	P		External memory address signal (highest order bit)
12	WE	O	N		External memory WE signal. When L, data is written into external memory. During WE=L, clock cycle is one and a half times of master clock cycle.
13	DTOT	O	P		Output data synchronized with DTCK
14	DTVL	O	P		Indicates that output data is valid (H). This signal is H for 192 bits of 1H other than skew bit (129th bit).
15	CRCE	O	N		Data error signal indicating error checking result. L indicates error. A result is output for each CRC block (1H=CRC blocks). *1
16	ER4	O	N		Error signal for 4th phase of data and output for each CRC block. L indicates error.
17	ER3	O	N		Error signal for 3rd phase of data and output for each CRC block. L indicates error.
18	ER2	O	N		Error signal for 2nd phase of data and output for each CRC block. L indicates error.
19	ER1	O	N		Error signal for 1st phase of data and output for each CRC block. L indicates error.
20	DSC	O	P		Input data (DTIN) delay control signal (highest order bit)
21	DSB	O	P		〃
22	DSA	O	P		Input data (DTIN) delay control signal (lowest order bit). Change occurs in units of Vs.
23	CKMS	I	N		Master clock input. Reference clock for pulse decay. fs = 44.056kHz: 14.31818MHz, fs = 44.1kHz: 14.3325MHz. 40 to 60% duty is recommended.
24	DTIN	I	P		Input data obtained from playback video signals
25	DTZN	I	P		Indicates that DTIN data is present (H).

Figure 6-42 CX23073 Pin Descriptions

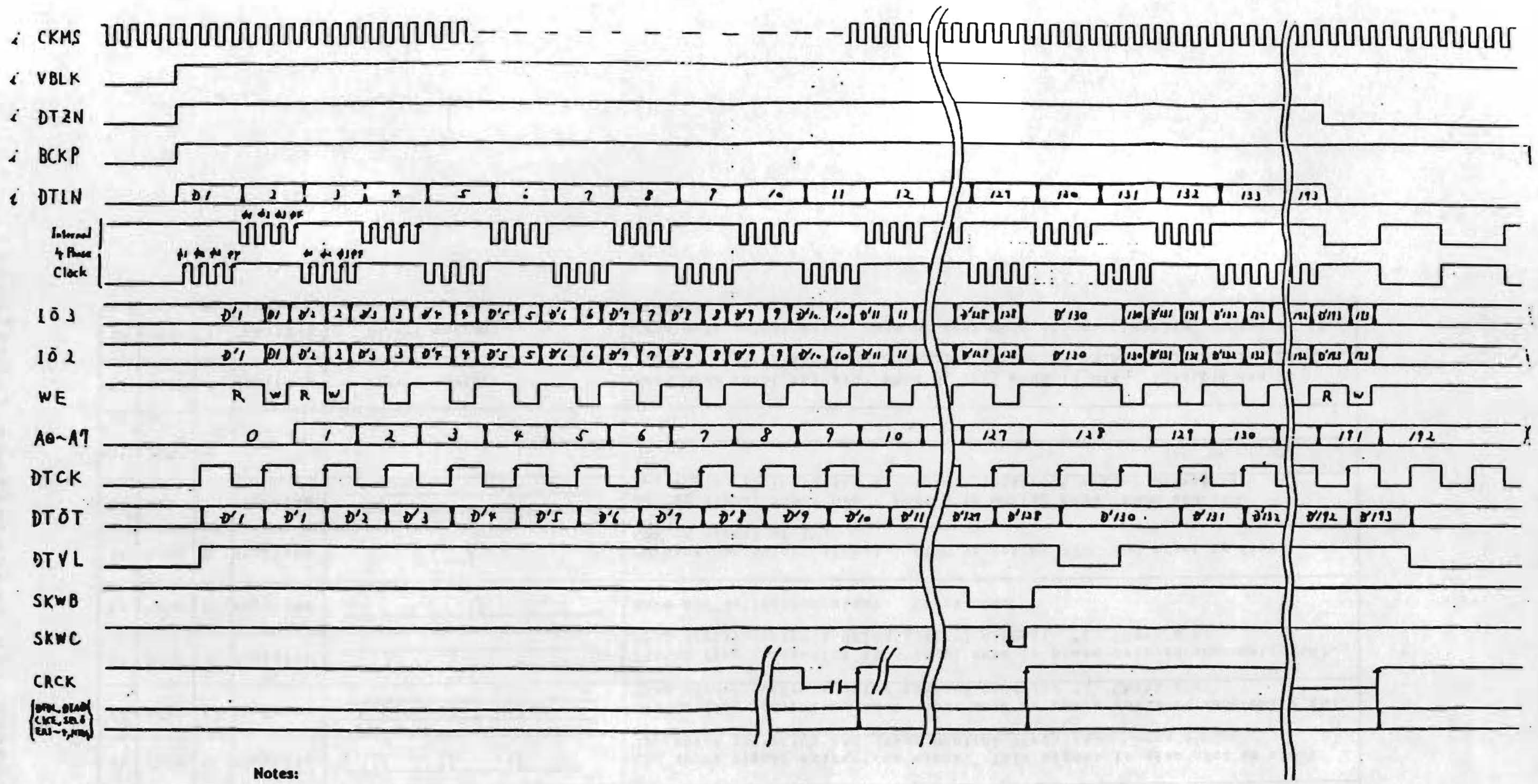
Figure 6-42 CX23073 Pin Descriptions (continued)

No.	Name	I/O	Polarity	Waveform	Description
26	BCKP	I	N	H	Back porch signal used to control control pulse generation block
27	SKWB	I	N	H	1-bit wide signal indicating skew bit position (129th bit of 1H)
28	STSC	I	N	V	Indicates start point of data zone during the V period. Sets SYND signal.
29	VBLK	I	N	V	Indicates V blanking (non-data zone).
30	EINT	I	N		1H-wide signal indicating interleave block
31	DVBL	I	N	V	1H-delayed VBLK signal
32	NC	–			
33	MSEL	I		Direct current	Muting signal generation process select pin (H: 1610 method, L: New method) *2
34	MTA	I		Direct current	Sets muting time. 8 time values are available, using three bits, MTA, MTB, and MTC. *3
35	MTB	I		Direct current	〃 〃
36	MTC	I		Direct current	〃 〃
37	MSD	I		Direct current	Sets sensitivity level (number of CRC errors). When level is reached, a muting signal is generated. A level from 2H to 30H can be set using four bits MSA through MSD. *4
38	MSA	I		Direct current	〃 〃
39	MSB	I		Direct current	〃 〃
40	VSS	–			GND
41	MSC	I		Direct current	Sets sensitivity level (number of CRC errors). *4
42	MSW	I		Direct current	Muting signal generation on/off signal. When H, no muting signal is generated regardless of sensitivity and time. *3
43	EMPH	O	P	Direct current	Indicates emphasis bit (skew bit of 1st 1H in each interleave block) extraction on input data. H indicates that emphasis is on. This pin is protected from errors.
44	FSID	O		Direct current	Indicates sampling frequency bit (skew bit of 2nd 1H in each interleave block) extraction on input data.
45	SKW3	O	P	Direct current	Indicates skew bit of 3rd 1H in each interleave block extraction on input data (undefined signal).
46	SKW4	O	P	Direct current	Indicates skew bit of 4th 1H in each interleave block extraction on input data (undefined signal).
47	VDD	–			+5 V
48	FSHD	O		Direct current	Outputs sampling frequency information like FSID. While FSID is not protected from errors, FSHD is protected from errors.
49	DTCK	O	P		Output data (DTOT) clock signal. Reference clock for pulse rise. Reference signal.
50	SELO	O			Indicates selected phase of output data (DTOT). H indicates 3rd phase and L indicates 2nd phase.

No	Name	I/O	Polarity	Waveform	Description
51	SELS	I		Direct current	Sets data selection method. H indicates single-phase selection and L double-phase selection. *1
52	MTRG	O	Negative		Muting start signal. L indicates start. This signal is controlled in units of interleave blocks.
53	MUT2	O	Negative		Muting signal. L indicates muting. Whenever MSW is H, this signal is also H.
54	VSS	-			GND
55	CRCK	O	Negative		CRC error signal extraction clock. This signal is also used as clock for phase selection and delay control circuits. Check pin.
56	DTAD	O	Positive		Status flag indicating that input data is phase-advanced abnormally (H). This signal controls delay control circuit. *1 Check pin.
57	DTDL	O	Positive		Status flag indicating that input data is phase-delayed abnormally (H). This signal controls delay control circuit. *1 Check pin.
58	SKWC	O	Negative		Skew bit extraction clock. Check pin.
59	SYND	O	Negative		OK syndrome output signal. SYND is set by STSC and reset by first CRC OK signal of 1V.
60	MIN	I	Negative		Muting signal input pin. When L in muting mode, EMPH and FSHD extraction is inhibited to prevent incorrect signal detection.
61	VDD	-			+ 5V
62	NC				
63	RSET	I	Positive	Direct current	Test mode reset signal. When H, test mode is off. This pin can be used for initialization. Usually, connected to ground.
64	TEST	I	Positive	Direct current	Test mode set signal. When H, test mode is on. Usually, connected to ground.

Figure 6-42 CX23073 Pin Descriptions (continued)

3-4. TIMING CHART



Notes:

. DTVL is also L while DVBL is L.

. See the Timing Chart section for the CX23074 for information on relationship between STSC and SYND.

. MUT2 is set at the leading edge of CRCK and reset at the trailing edge of DVBL.

. DSA, DSB, and DSC changes at the trailing edge of the first CRCK after DVBL goes L.

Figure 6-43 CX23073 Timing Chart

*1) Data select, error states, and data delay control

Error states				Output						PCM-1610 System			
						SELS = '0'		SELS = '1'					
ER4	ER3	ER2	ER1	DTDL	DTAD	CRCE	SELO	CRCE	SELO	DTDL	DTAD	CRCE	SELO
1	1	1	1	0	0	1	0	1	0	0	0	1	0
1	1	1	0	0	0	1	0	1	0	0	0	1	0
1	1	0	1	0	0	1	0	1	0	0	0	1	0
1	1	0	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	0	0	1	1	1	1	0	0	1	1
1	0	1	0	0	0	0	0	1	1	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	1	0	0	0
0	1	1	1	0	1	1	0	1	0	0	1	1	0
0	1	1	0	0	0	1	0	1	0	0	0	1	0
0	1	0	1	0	0	0	1	1	0	0	0	0	1
0	1	0	0	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	1	1	1	1	0	1	1	1
0	0	1	0	0	0	0	0	1	1	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	0	0

'0' = Error — Status flag '1' = Advance, Delay — '0' = Error — '0' = ϕ_3, '1' = ϕ_2 — '0' = Error — '0' = ϕ_3, '1' = ϕ_2 — Status flag — '0' = Error — '0' = ϕ_3, '1' = ϕ_2

Reference

***2. MSEL function**

In the **PCM-1610**, an error state is not cancelled until eight continuous CRC blocks are normal after error recovery. In the new system (**PCM-1630**), an error state is canceled when two continuous CRC blocks are normal after error recovery. A muting state, however, is not canceled until eight CRC blocks are processed. This applies for both systems.

***3. Muting time setting**

MTA	MTB	MTC	MSW	Muting Time
x	x	x	1	Muting OFF
1	1	1	0	0.02 sec = 1 V
0	1	1	0	0.03 〃 = 2 V
1	0	1	0	0.07 〃 = 4 V
0	0	1	0	0.13 〃 = 8 V
1	1	0	0	0.27 〃 = 16 V
0	1	0	0	0.53 〃 = 32 V
1	0	0	0	1.07 〃 = 64 V
0	0	0	0	2.13 〃 = 128 V

***4. Muting sensitivity setting**

MSD	MSC	MSB	MSA	Muting Sensitivity	
1	1	1	1	2.7 H = [illegible] 2~3 H	Nominal
1	1	1	0	〃	
1	1	0	1	5.3 H = 〃 5 H	
1	1	0	0	8 H = 〃 7~8 H	
1	0	1	1	10.7 H = 〃 10 H	
1	0	1	0	13.3 H = 〃 12~3 H	
1	0	0	1	16 H = 〃 15 H	
1	0	0	0	18.7 H = 〃 17~8 H	
0	1	1	1	21.3 H = 〃 20 H	
0	1	1	0	24 H = 〃 22~3 H	
0	1	0	1	26.7 H = 〃 25 H	
0	1	0	0	29.3 H = 〃 27~8 H	
0	0	1	1	32 H = 〃 30 H	
0	0	1	0	〃	
0	0	0	1	〃	
0	0	0	0	〃	

Notes: 1. Nominal MSD = 0 : 20 H
MSC = 0 : 10 H
MSB = 0 : 5 H
MSA = 0 : 2-3 H

2. The lowest sensitivity level is 32H and the highest sensitivity level is 2H is 2H to 3H.

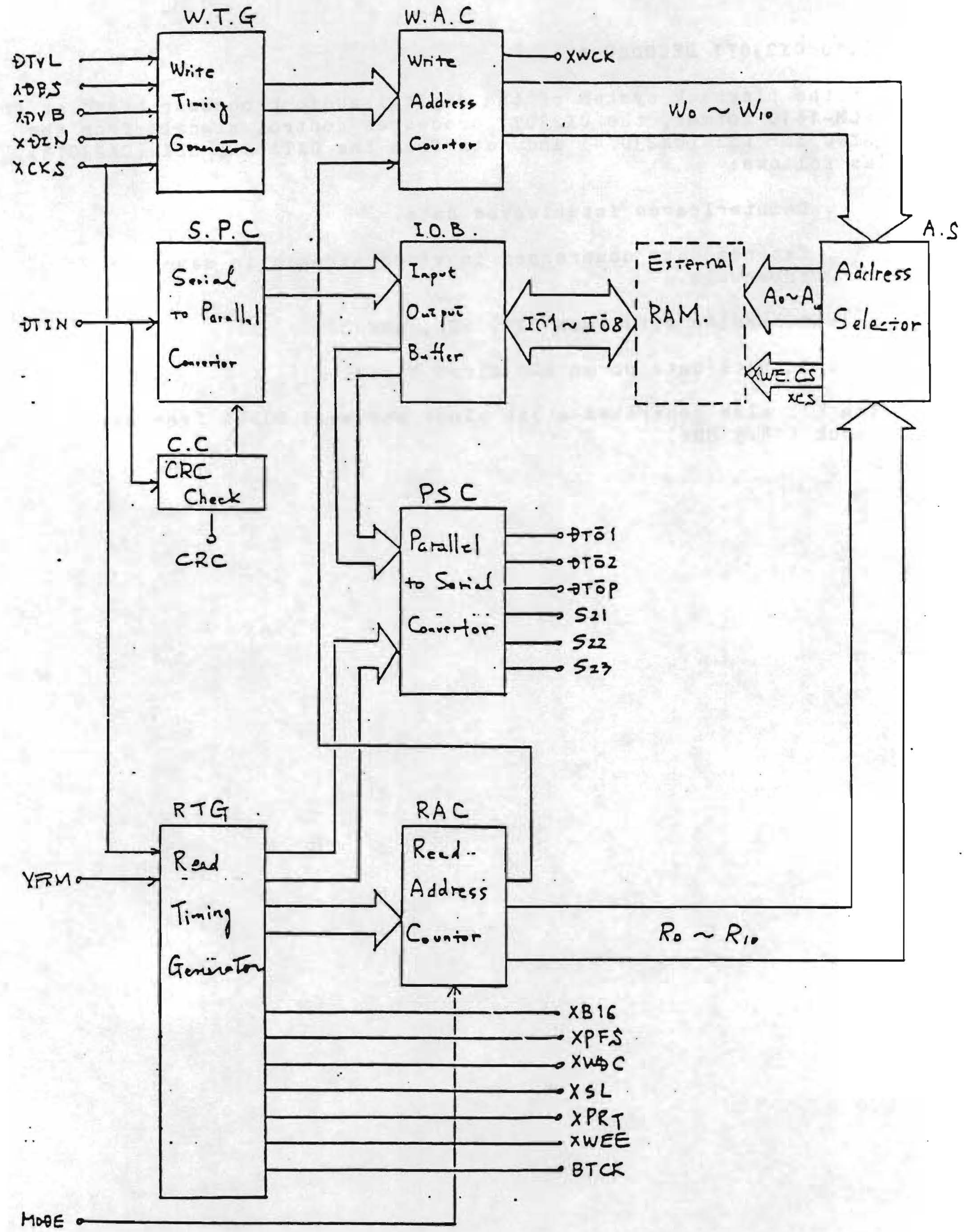
6.10 CX23071 DECODER A

In the playback system of the digital audio processor based on the **PCM-1610** format, the CX23071 processes control signals from the SYNC SEP LSI (CX23074) and data from the DATA SEP LSI (CX23073), as follows:

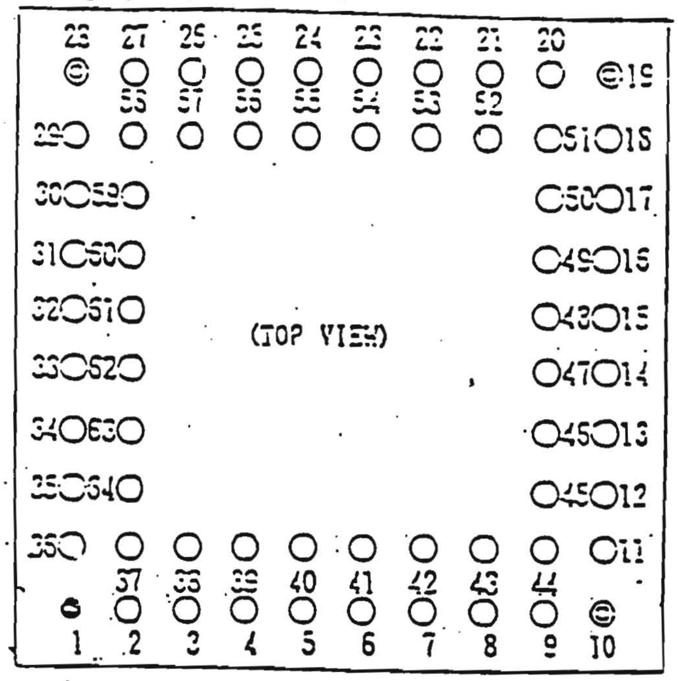
- Deinterleaves interleaved data.
- Extends data compressed in video signals in sampling intervals.
- Generates syndromes S21, S22, and S23.
- Outputs data on an LSB first basis.

The LSI also generates a bit clock and word clock from master clock (14.3 MHz).

BLOCK DIAGRAM



CX23071 (DEC - A)



Pin no.	I/O	Pin name	Pin no.	I/O	Pin name	Pin no.	I/O	Pin name	Pin no.	I/O	Pin name
1	I/O	IO2	17	O	DTO2	33	I	TE05	49	O	S21
2	I/O	IO4	18	O	DTOP	34	I	TE03	50	O	S22
3	I/O	IO6	19	O	ETCK	35	I	TE01	51	O	S23
4	I/O	IO8	20	O	XB16	36	I/O	IO1	52	O	XMDC
5	O	A0	21	O	XPFS	37	I/O	IO3	53	O	XSL
6	O	A2	22	O	XPET	38	I/O	IO5	54	—	VSS
7	O	A4	23	—	N.C	39	I/O	IO7	55	I	XCKS
8	O	A6	24	—	N.C	40	—	VSS	56	—	N.C
9	O	A8	25	I	XFRM	41	O	A1	57	—	N.C
10	O	A10	26	I	XDIN	42	O	A3	58	I	XDBS
11	O	A9	27	I	DTIN	43	O	A5	59	O	XKCK
12	O	XWE	28	I	DTVL	44	O	A7	60	—	N.C
13	O	CS	29	I	XDVB	45	O	XCS	61	—	VDD
14	—	N.C	30	O	CRCC	46	—	N.C	62	—	N.C
15	O	XWEE	31	I	MODE	47	—	VDD	63	I	TE04
16	O	DTO1	32	—	N.C	48	—	N.C	64	I	TE02

Fujitsu CMOS Gate Array "VH" Version Pin Assignment

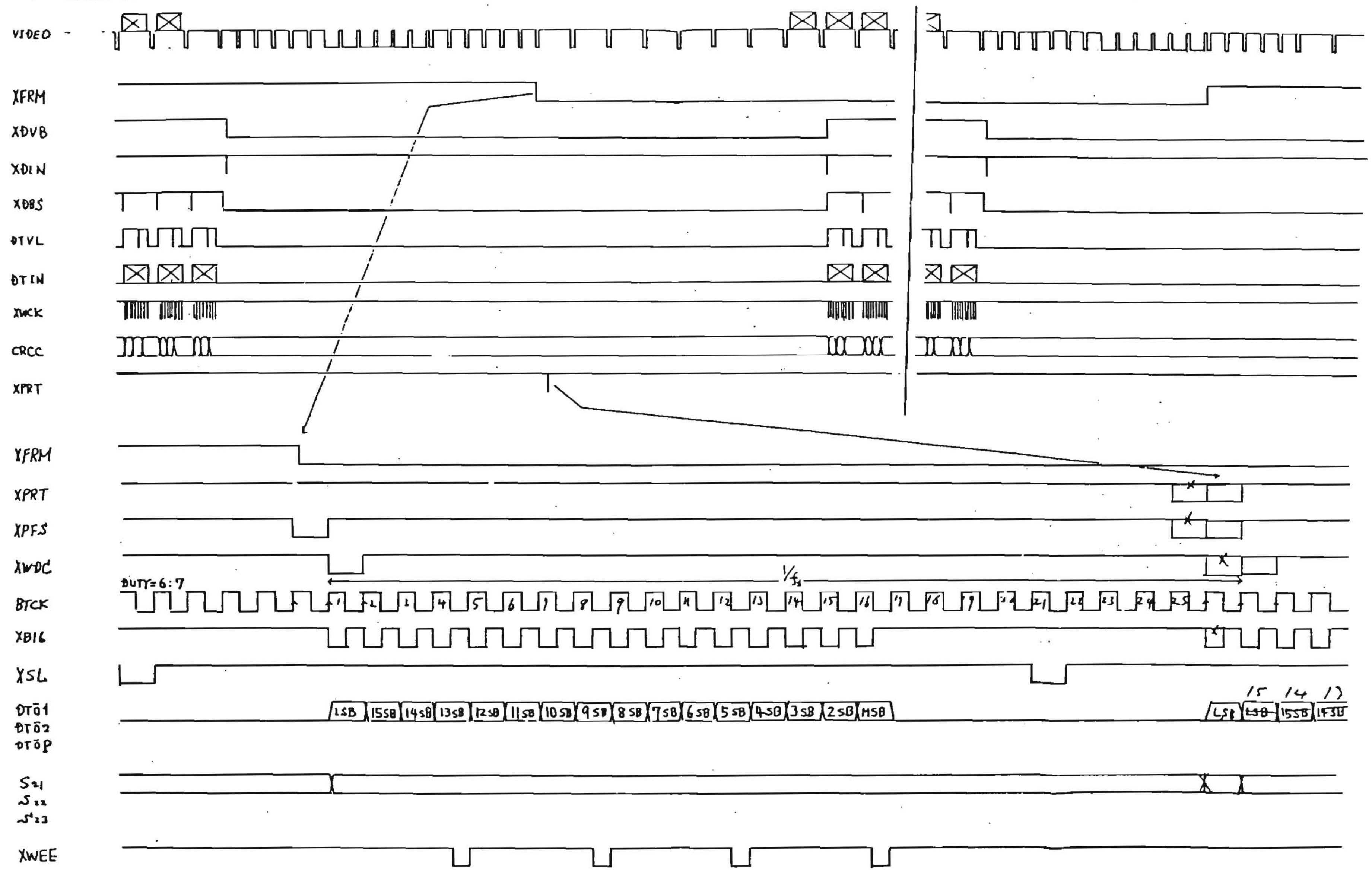
PIN DESCRIPTION

NO.	Name	I/O	Polarity	Waveform	Description
1	IO2	I/O	Posi		External memory I/O data signal.
2	IO4	I/O	Posi		"
3	IO6	I/O	Posi		"
4	IO8	I/O	Posi		"
5	A0	O	Nega		External memory address signal
6	A2	O	Nega		"
7	A4	O	Nega		"
8	A6	O	Nega		"
9	A8	O	Nega		"
10	A10	O	Nega		"
11	A9	O	Nega		"
12	XWE	O	Nega		External memory WE signal
13	CS	O	Nega		External memory chip select signal. During MODE=L, only CS is active and XCS=H.
14	N.C	—			
15	XWEE	O	Nega		Encoder signal which generates 25-bit slot of data four times in units of : four bits
16	DTO1	O	Posi		16-bit-per-word PCM signal. When XWDC=L, LSB, 2SB, . . . , and MSB occur. CH1
17	DTO2	O	Posi		" CH2
18	DTOP	O	Posi		" PARITY
19	BTCK	O	Posi		Bit clock. Each word consists of 25-bit clock cycle. DTO1, DTO2, and DTOP signals are output at the leading edge of this clock.
20	XB16	O	Nega		Clock generated only for 16 bits of each word which contains a PCM signal. This clock is 180 degrees out of phase with bit clock.
21	XPFS	O	Nega		Timing signal for each word. This signal leads XWDC one bit of phase.
22	XPRT	O	Nega		Timing signal generated for each frame and used to adjust encoder bit phase
23	N.C.	—			
24	N.C	—			

No	Name	I/O	Polarity	Waveform	Description
25	XFRM	I	N		Frame signal
26	XDIN	I	N		Timing signal indicating 35H interleave block (delayed 1H)
27	DTIN	I	P		Input PCM signal (delayed 1H)
28	DTVL	I	P		Indicates data field of input PCM signal (delayed 1H).
29	XDVB	I	N		V blanking signal (delayed 1H)
30	CRCC	O	P		Flag indicating CRC checking result (monitor output)
31	MODE	I		Direct current	External memory (2K x 8 bits) select signal. When H, two memories are used. When L, one memory is used.
32	N.C	—			
33	TE05	I		Direct current	Input pin for LSI testing. Usually L.
34	TE03	I		Direct current	〃 〃
35	TE01	I		Direct current	〃 〃
36	IO1	I/O	P		External memory I/O data signal
37	IO3	I/O	P		〃
38	IO5	I/O	P		〃
39	IO7	I/O	P		〃
40	VSS	—			GND
41	A1	O	N		External memory address signal
42	A3	O	N		〃
43	A5	O	N		〃
44	A7	O	N		〃
45	XCS	O	N		External memory chip select signal. Valid only when MODE= H.
46	N.C	—			
47	VDD	—			+5V
48	N.C	—			

No	Name	I/O	Polarity	Waveform	Description
49	S21	O	P	1wd	Syndrome signal indicating CH1 error status
50	S22	O	P	1wd	Syndrome signal indicating CH2 error status
51	S23	O	P	1wd	Syndrome signal indicating parity error status
52	XWDC	O	N	1wd	Timing signal whose leading edge indicates start of one word
53	XSL	O	N	1wd	Timing signal which leads XWDC 5-bit clock
54	VSS	—			GND
55	XCKS	I	N		Master clock $f_s = 44.1$ kHz : 14.3325 MHz $f_s = 44.056$ kHz : 14.3181 MHz.
56	N.C	—			
57	N.C	—			
58	XDBS	I	N	1V	Blanking sync signal (delayed 1H)
59	XWCK	I	N	1H	Address counter clock used to write input PCM signals to external memory (monitor output)
60	N.C	—			
61	VDD	—			+5V
62	N.C	—			
63	TE04	I		Direct current	Input pin for LSI testing. Usually L.
64	TE02	I		Direct current	" "

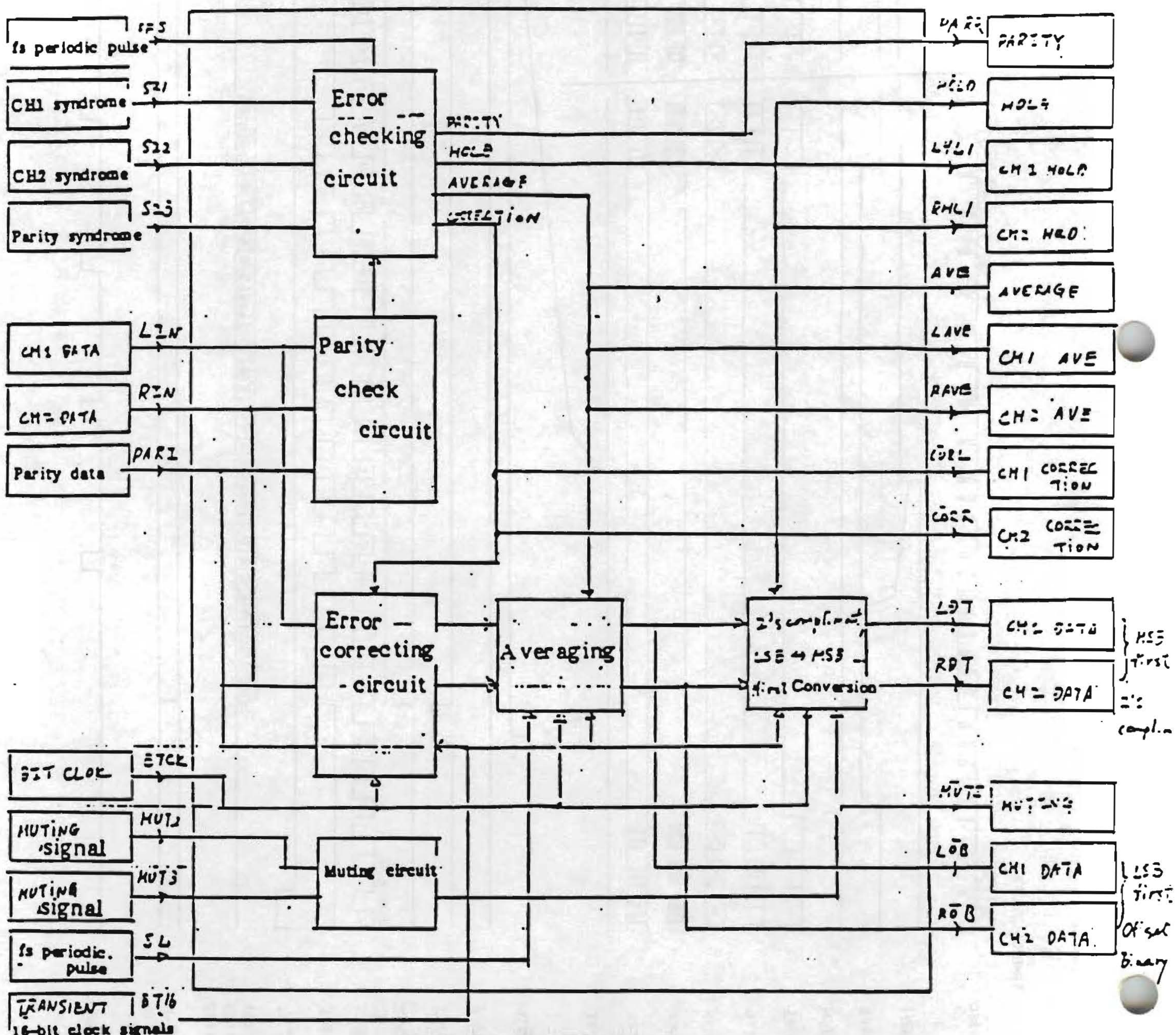
TIMING CHART



6.11 CX23072 ERROR CORRECTION

The CX 23072 is one of the four LSIs (CX23071 to CX23074) developed to decode **PCM-1610** format audio signals.

This LSI is placed in the last stage of the decoder system. That is, it processes deinterleaved PCM audio signals and CRC error information (syndrome) from the CX23071 and makes error correction. The LSI also has the capability to mute data when an abnormal state may occur because of out-of-phase external sync or many CRC errors.



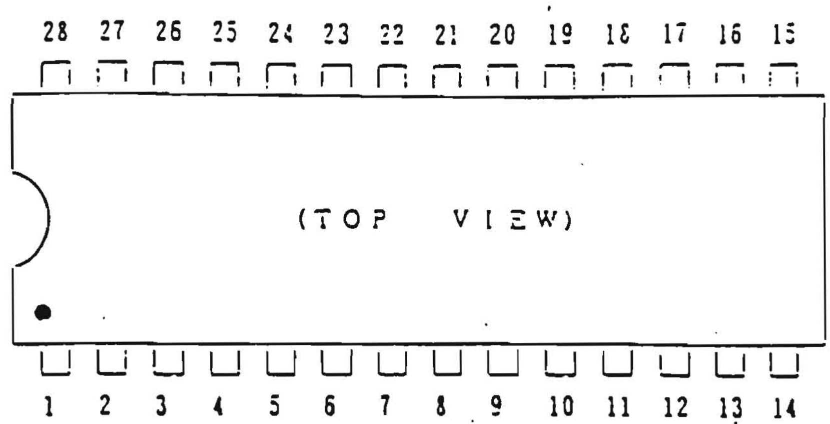
CX23072 Block Diagram

PIN ASSIGNMENT ILLUSTRATION

PIN ASSINGNMENT MB63H126 (CX23072)

Note: Number of Fujitsu

·Pin Assignment (28-pin DIP)

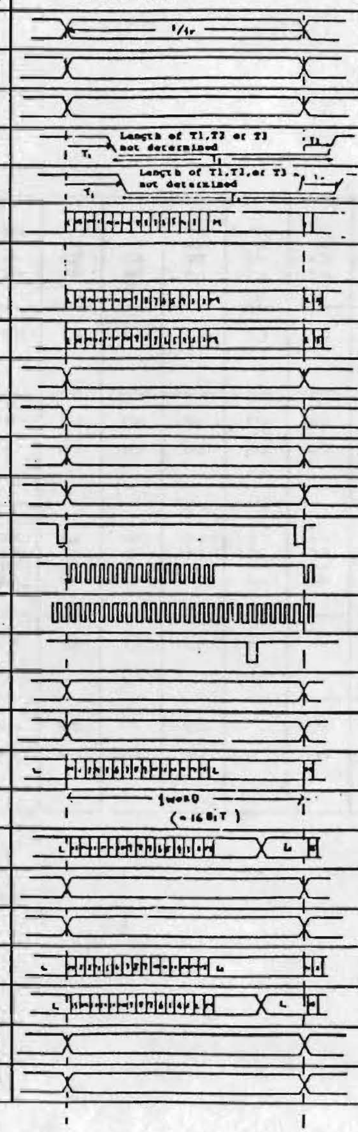


Pin no	I/O	Pin name	Pin no	I/O	Pin name
1	I	S21	15	I	BT16
2	I	S22	16	I	BTCK
3	I	S23	17	I	SL
4	I	MUT2	18	O	AVE
5	I	MUT3	19	O	HOLD
6	I	LIN	20	O	LDT
7	–	VSS	21	–	VDD
8	I	PARI	22	O	LOB
9	I	RIN	23	O	LAVE
10	O	MUTS	24	O	LHL1
11	O	PARR	25	O	RDT
12	O	CORL	26	O	ROB
13	O	CORR	27	O	RAVE
14	I	PFS	28	O	RHL1

Fujitsu CMOS Gate Array "H" Version Pin Assignment

PIN DESCRIPTION

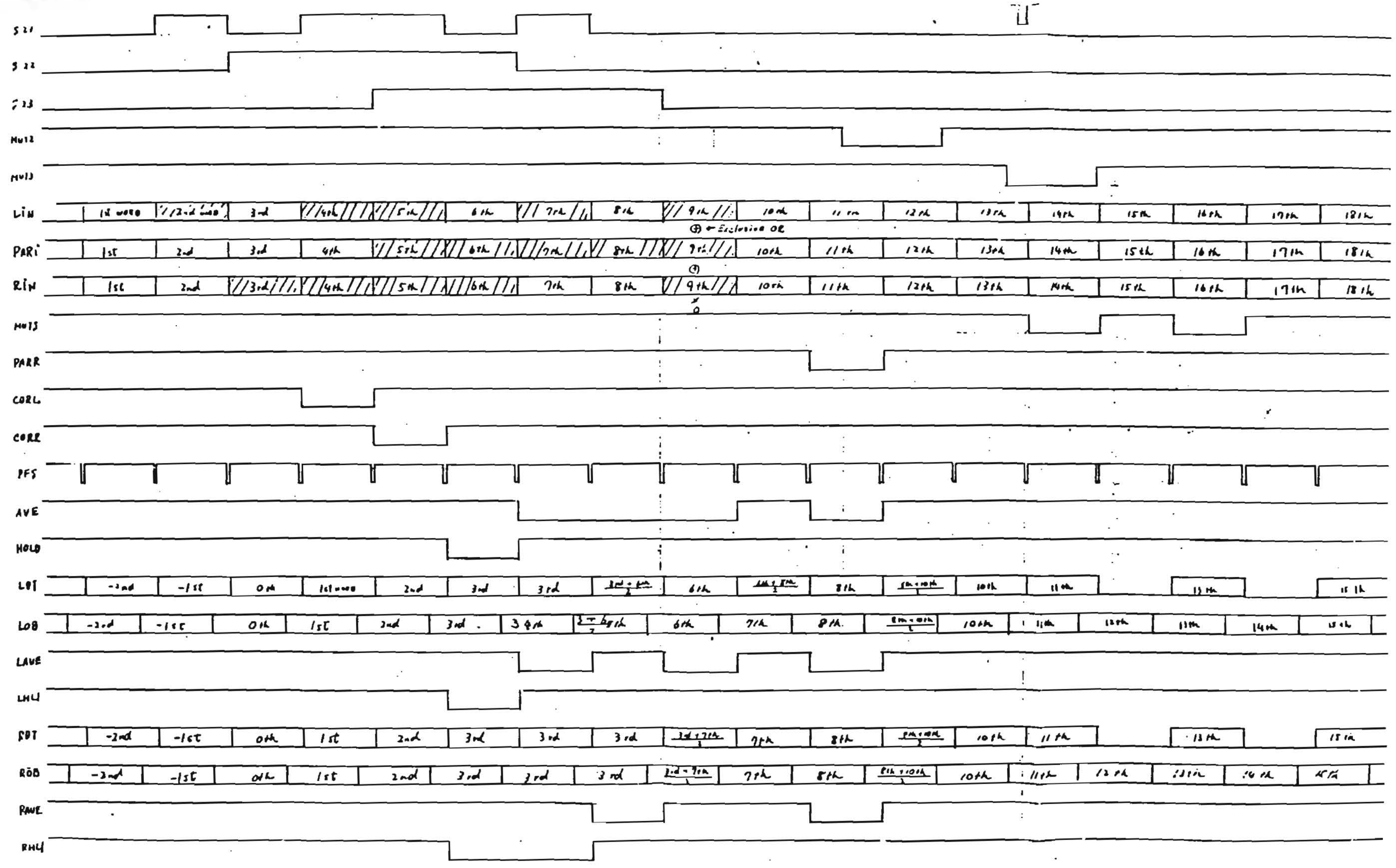
PIN	Name	I/Ō	POLARITY	Waveform	Description
1	S21	I	Posi		Syndrome signal (fs cycle). S21=H indicates that CH1 data error occurs. S21=L indicates that no CH1 data error occurs.
2	S22	I	Posi		Syndrome signal (fs cycle). S22=H indicates that CH2 data error occurs. S22=L indicates that no CH2 data error occurs.
3	S23	I	Posi		Syndrome signal (fs cycle). S22=H indicates that parity error occurs. S22=L indicates that no parity error occurs.
4	MUT2	I	Nega		When L, PCM audio signals are muted.
5	MUT3	I	Nega		Length of T1, T2, or T3 not determined (synchronized with master clock)
6	LIN	I	Posi		16-bit-per-word serial PCM audio signal input from CH1. Trailing edge of BT16 is synchronized with change in BIT.
7	VSS	—	—		Ground
8	PARI	I	Posi		16-bit-per-word serial PCM signal indicating CH1 and CH2 odd parity. Trailing edge of BT16 is synchronized with change in BIT.
9	RIN	I	Posi		16-bit-per-word serial PCM audio signal input from CH2. Trailing edge of BT16 is synchronized with change in BIT.
10	MUTS	Ō	Nega		Synchronized with leading edge of PFS. MUTS=L indicates that word following LDT or RDT is to be muted.
11	PARR	Ō	Nega		Synchronized with leading edge of PFS. PARR=L indicates that word following LDT or RDT contains parity error.
12	CORL	Ō	Nega		Synchronized with leading edge of PFS. CORL=L indicates that error in word following LDT was corrected.
13	CORR	Ō	Nega		Synchronized with leading edge of PFS. CORL=L indicates that error in word following RDT was corrected.
14	PFS	I	Nega		Timing signal
15	BT16	I	Nega		Rises and falls 16 times during the Fs period. First trailing edge is synchronized with leading edge of PFS. This signal has opposite polarity with respect to BTCK.
16	BTCK	I	Posi		Clock input. 1.1025MHz when Fs=44.1kHz and 11.01398MHz when Fs=44.0561kHz.
17	SL	I	Nega		Timing signal leading PFS 5 BTCK cycles.
18	AVE	Ō	Nega		Synchronized with leading edge of PFS. AVE=L indicates that average value has been interpolated for word following LDT or RDT.
19	HOLD	Ō	Nega		Synchronized with leading edge of PFS. HOLD=L indicates that previous value has been held for word following SDT or RDT.
20	LDT	Ō	Posi		Outputs LIN input signals. 16-bit-per-word PCM audio signal. MSB first. 2's complement.
21	VDD	—	—		Power (+5V)
22	LOB	Ō	Posi		Outputs LIN input signals. 16-bit-per-word PCM audio signal. LSB first. first Offset binary. This signal is not muted.
23	LAVE	Ō	Nega		Syncronized with leading edge of RFS. LAVE=L indicates that average value has been interpolated for word following LDT.
24	LHLI	Ō	Nega		Synchronized with leading edge of PFS. LHL1=L indicates that previous value has been for word following LDT.
25	RDT	Ō	Posi		Outputs RIN input signals. 16-bit-per-word PCM audio signal. MSB first. 2's complement.
26	ROB	Ō	Posi		Outputs RIN input signals. 16-bit-per-word PCM audio signal. LSB first. Offset binary. This signal is not muted.
27	RAVE	Ō	Nega		Synchronized with leading edge of PFS. RAVE=L indicates that average value has been interpolated for word following RDT.
28	RHLI	Ō	Nega		Synchronized with leading edge of RFS. PHL1=L indicates that previous value has been held for word following RDT.



Synchronized with leading edge of PFS.

TIMING CHART

This timing chart is a word basis.



SECTION 7

DAE-1100 CIRCUIT DESCRIPTIONS

SECTION 7

DAE-1100 CIRCUIT DESCRIPTIONS

7.1 MAIN UNIT

7.1.1. Digital Signal Interface Circuit (I/O, CON board)

This is an interface block for PCM data between the digital audio processor and the editor.

1 **PCM data input block.....Refer to Figure 7-1**

- o In the case of parallel input, PCM data input via the external connector is stored in the "parallel in FF" via the static protection circuit (CON board).

- o In the case of serial input, PCM data input via the external connector passes through the static protection circuit (CON board), and word sync is extracted in the sync separator. Serial PCM data is converted into parallel data and stored in the "serial in FF".

  The data stored in each FF is output to the data bus by the bus control circuit (SC-B board).

2 **PCM data output block....Refer to Figure 7-2**

PCM data in the data bus is further stored into the ENC FF or D/A FF by the bus control circuit (SC-B board).

The PCM data stored in each FF above is output to an external connector via the "parallel out FF", "P--->S converter", and the static protection circuit (CON board).

7.1.2. Digital Signal Processing Circuit (SC-A and SC-B boards)

This is a circuit for PCM signal processing in the search mode, in the cross fader or when fader is used. It also generates the control signal for such processing. Refer to Figure 7-3.

1 **Sync generator block (SC-A board)**

This locks the PLL circuit with a "ref word sync signal" sent from the PCM data input block (I/O board), and sends out clock and word sync signals to each block.

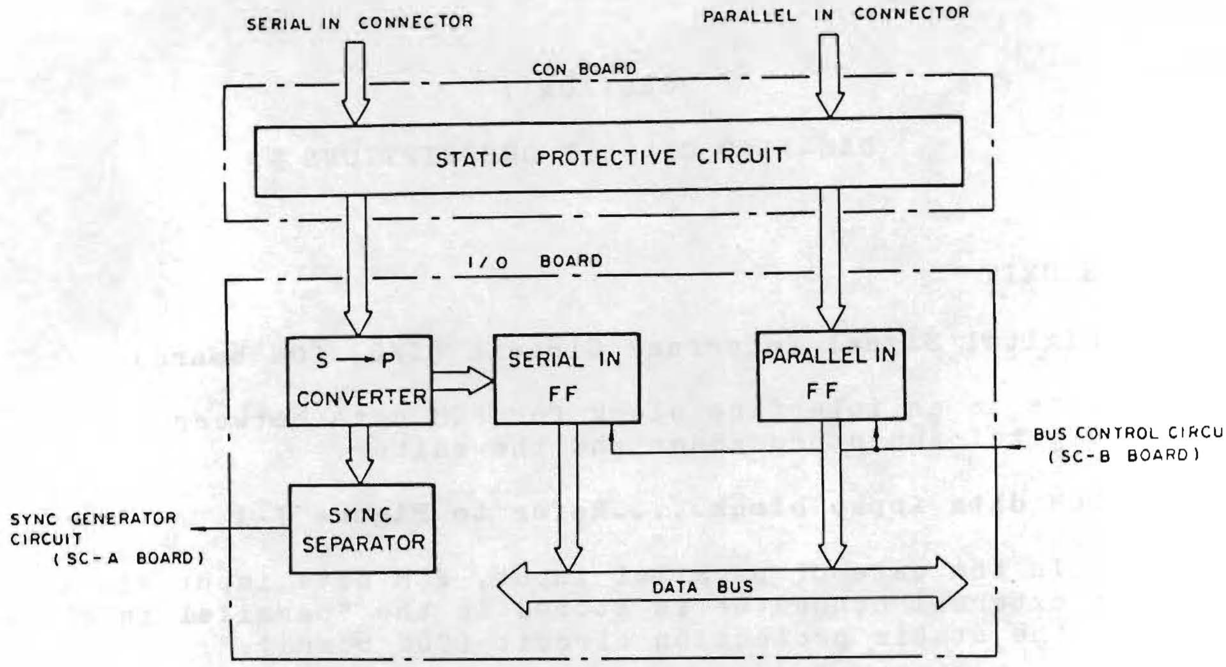


Figure 7-1

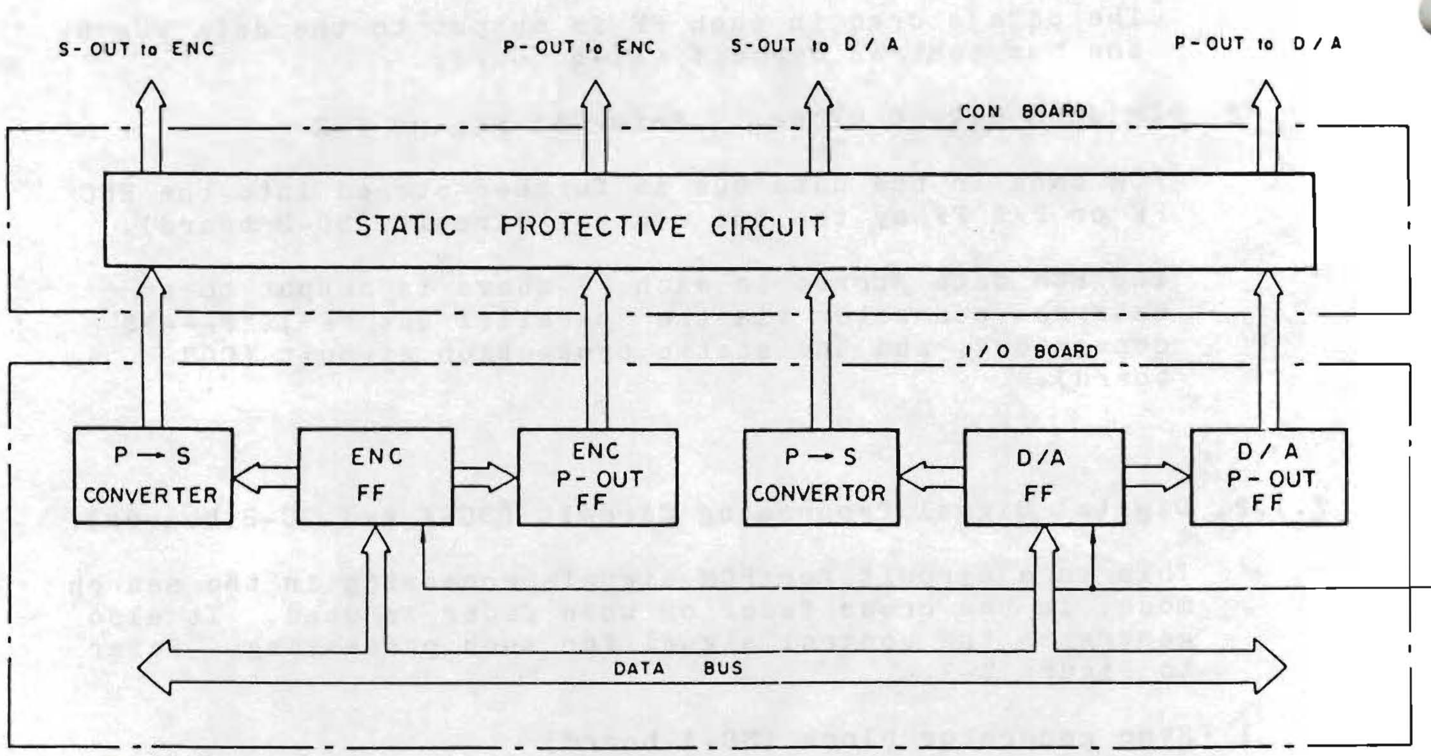


Figure 7-2

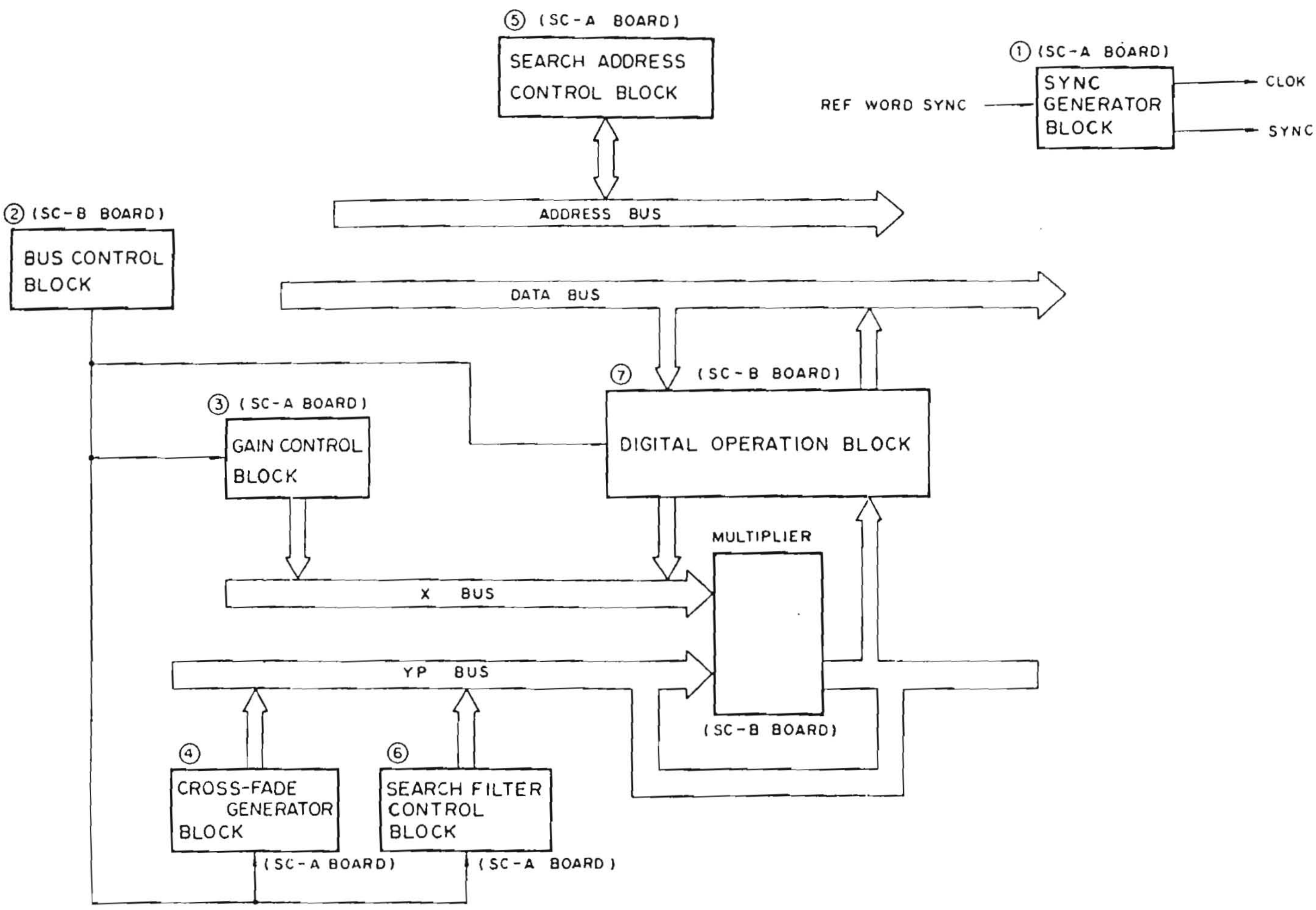

⑤ (SC-A BOARD)
SEARCH ADDRESS CONTROL BLOCK
① (SC-A BOARD)
REF WORD SYNC
SYNC GENERATOR BLOCK
CLOK
SYNC
② (SC-B BOARD)
BUS CONTROL BLOCK
ADDRESS BUS
DATA BUS
⑦ (SC-B BOARD)
DIGITAL OPERATION BLOCK
③ (SC-A BOARD)
GAIN CONTROL BLOCK
MULTIPLIER
X BUS
YP BUS
(SC-B BOARD)
④
CROSS-FADE GENERATOR BLOCK
⑥
SEARCH FILTER CONTROL BLOCK
(SC-A BOARD)
(SC-A BOARD)

Figure 7-3

2 **Bus control block (SC-B board)**

This decodes edit mode signals sent from the edit timing control block (EDT board), and controls the four bus control ROMs (Bus out, FF clock, Filter CTL and Cross Fade ROMs). In accordance with the ROM control, each block inputs/outputs data from/to the PCM data bus of X/YP bus of the multiplier.

3 **Gain control block (SC-A board)**

This decodes parallel fader data sent from the system control block (SYS board) so as to supply it to the digital processing circuit (SC-B board) and outputs it to the X bus.

4 **Cross fade coefficient generator block (SC-A board)**

This generates cross fade coefficients A and B in accordance with a cross fade time signal sent from the system control block (SYS board). The coefficients A and B are output to the YP bus by the bus control block (SC-B board), and supplied to the digital processing circuit (SC-B board).

5 **Search address control block (SC-A board)**

When straight mode is set, it generates an address used for writing "compressed PCM data" to the Memory circuit (MEM board), and outputs it to the address bus.

When search mode is set, it outputs address data to the address bus by operating the address counter (up or down), which is prepared for reading the compressed PCM data according to the search clock (01,02) sent from the keyboard.

6 **Search filter control block (SC-A board)**

When straight mode is set, it reads out the "W filter coefficient", which is necessary for writing the compressed PCM data to the Memory circuit (MEM board), from the W FIL COE ROM, and outputs it to the TP bus.

When search mode is set, it reads out the "R filter coefficient", which is necessary for reading-out the compressed PCM data from the R FIL COE ROM, and outputs it to the YP bus.

7 **Digital processing block (SC-B board)**

It processes PCM signal through the 16-bit multiplier.

It stores PCM data (including compressed PCM data) from the data bus into their respective FF's, and further outputs the data to the X bus.

In addition to PCM data, fader data sent from the gain control block (SC-A board) is also output to the X bus. Data sent from the cross fade coefficient generator block or search control filter block is output to the YP bus. The data output to the X bus and TP bus is subjected to 16 x 16 Bit Parallel Multiplication with the help of the multiplier. The accumulation result is output to the data bus again through the level clipper.

Control of data input/output to and from each bus depends on the bus control block (SC-B board), and data accumulation necessary in each mode are performed.

7.1.3. Memory Circuit (MEM board)

This circuit (1M bit-configuration) is used as a search memory or a cross fade and synchronize memory for editing. Since the search memory and the memory for editing will never be used at the same time, this circuit can be used for a double purpose....Refer to Figure 7-4.

1 **Search memory**

o (Write)

PCM data necessary for the search mode is output to the data bus after being compressed as follows by the digital signal processing control circuit (SC-B board) to reduce the memory capacity.

fs-->fx/2, 16-bit linear quantization -->8-bit non-linear quantization, 2ch -->1ch

The compressed data is written into the memory with the input data latch. For the RAM address, an address which is generated in he search control address block (SC-A board) when straight mode is set is accessed to the memory with the address latch.

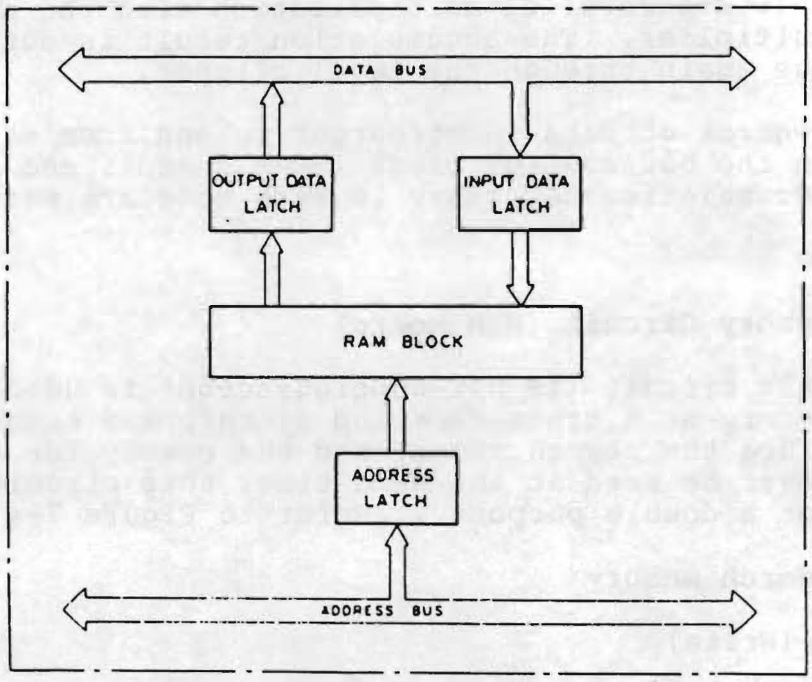

DATA BUS
OUTPUT DATA LATCH
INPUT DATA LATCH
RAM BLOCK
ADDRESS LATCH
ADDRESS BUS

Figure 7-4

o (Read)

An address which is generated in the search control address block (SC-A board) when search mode is set is accessed to the memory with the address latch. Read data is output to the data bus with the output data latch.

2 **Memory for Editing**

This memory is used for the PCM data necessary for preview and auto editing. Address allocation is as follows:

REC RAM	0000 - 4500 H	12 Frame (17665WD)
DELAY RAM	4501 - 47FF H	0.52 (767)
PB RAM	4800 - 51FF H	1.74 (2560)
SYNC RAM	5200 - 7FFF H	8.0 (11776)

3 **o (Write)**

PCM data in the data bus is written into the memory with the input data latch in each mode.

For the RAM address, an address which is output to the address bus from each mode counter of the edit mode address control block (EDT board) is accessed to the memory with the address latch.

o (Read)

An address from each mode counter is accessed to the memory with the address latch in the same way as for a write operation.

Read data is output to the data bus with the output data latch.

Each latch used for the search memory and the memory for editing are controlled by the bus control block (SC-B board).

7.1.4 Timecode Generator/Reader Circuit (TLC board)

This is a SMPTE timecode generator/reader circuit for absolute addressses used for editing, auto locate. For the generator output (one generator is built-in), either "drop frame" or "full frame" can be selected. Three readers are built-in, which also perform correction for dropout, etc. Operation accompanying such correction, or auto locate control depends on (TLC board) having 4K byte-software.... Refer to Figure 7-5.

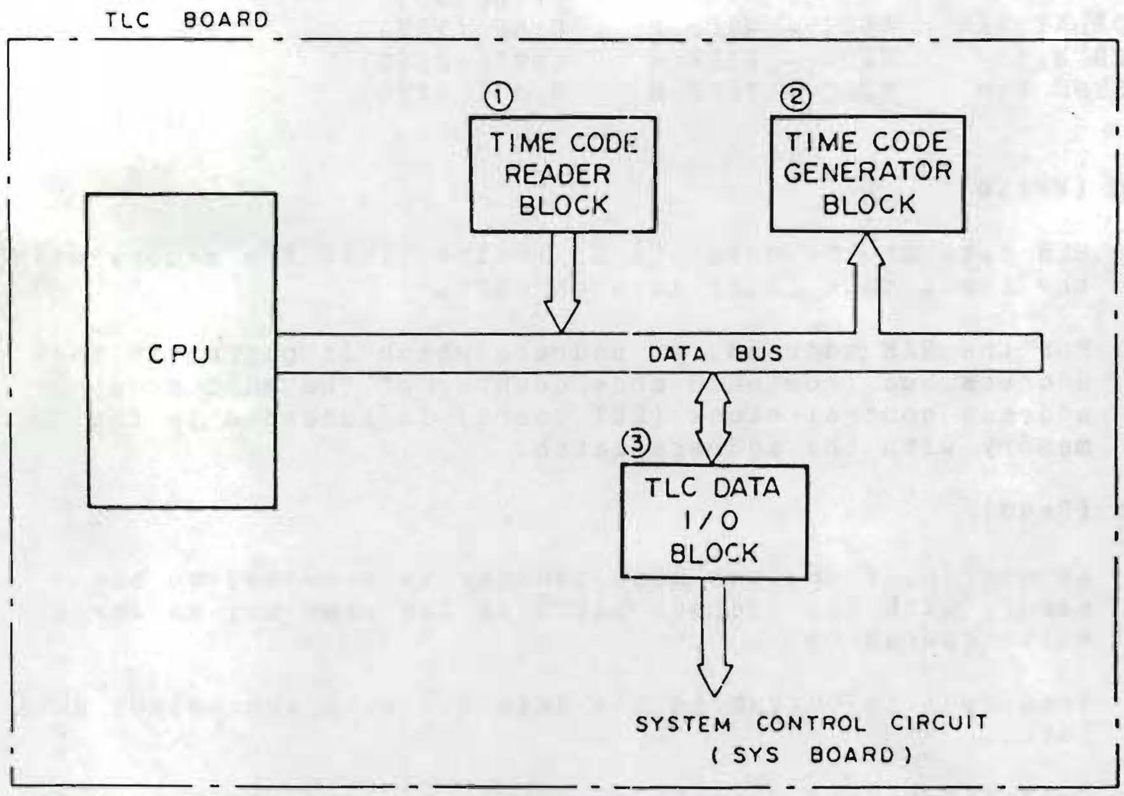

TLC BOARD
①
TIME CODE
READER
BLOCK
②
TIME CODE
GENERATOR
BLOCK
CPU
DATA BUS
③
TLC DATA
I/O
BLOCK
SYSTEM CONTROL CIRCUIT
(SYS BOARD)

Figure 7-5

1 **Timecode Reader Block**

A signal (balanced: 0dB 600 ohms, unbalanced: 0dB 10K ohms), which is input from the VTR to the "timecode in connector", is converted into TTL level in the comparator (EDT board), and output to the timecode reader block (TLC board). Timecode data and user's bit data are extracted in the data separator in the timecode reader block. They are stored in the timecode data RAM for a time, and then input to the CPU (TLC board).

2 **Timecode Generator Block**

This generates timing by locking the PLL according to a reference frame clock sent from the frame separate block (EDT board). The timecode to be output from the CPU (TLC board) according to this timing, is converted into SMPTE format and after undergoing level conversion in the output buffer (EDT board) is output to the "timecode out connector".

3 **TLC data I/O Block**

This transmits or receives data, such as timecode data used for timecode display, editing, auto locate, etc., VTR status data, or VTR command data, to and from the system control circuit CPU (SYS board).

7.1.5 Edit Timing Control Circuit (EDT board)

Since a "frame" is used as a basic unit in the system control block (SYS board), a control signal necessary for precision when a "word" unit is used, or a control signal necessary for video signal xchange is genereated in this circuit....Refer to Figure 7-6.

1 **Edit Mode Control Block**

This changes a frame unit control signal sent from the system control block (SYS board) to a word unit edit mode signal, and controls the bus out control block (SC-B board).

2 **Edit Timing Control Block**

This controls the edit mode address counter and word counter used for editing.

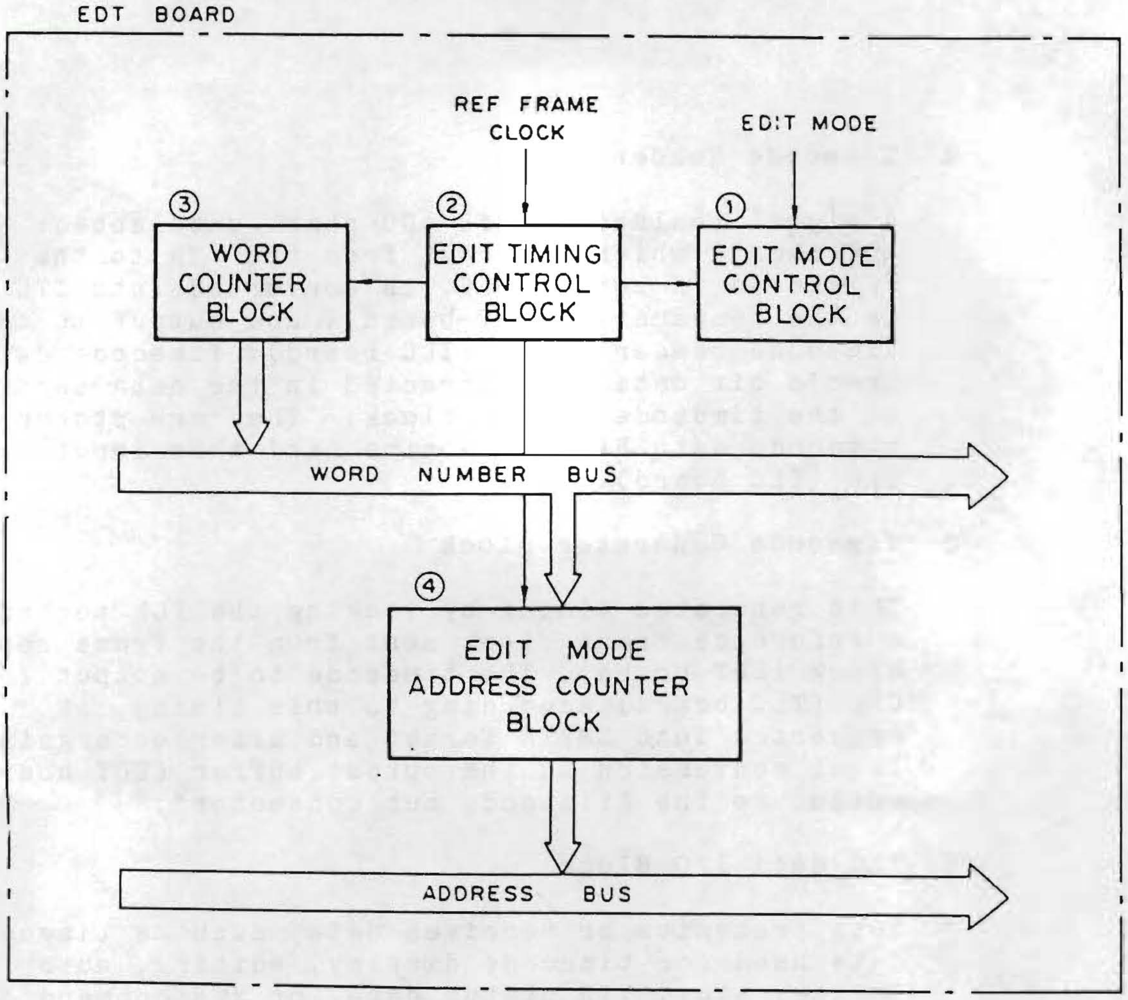


Figure 7-6

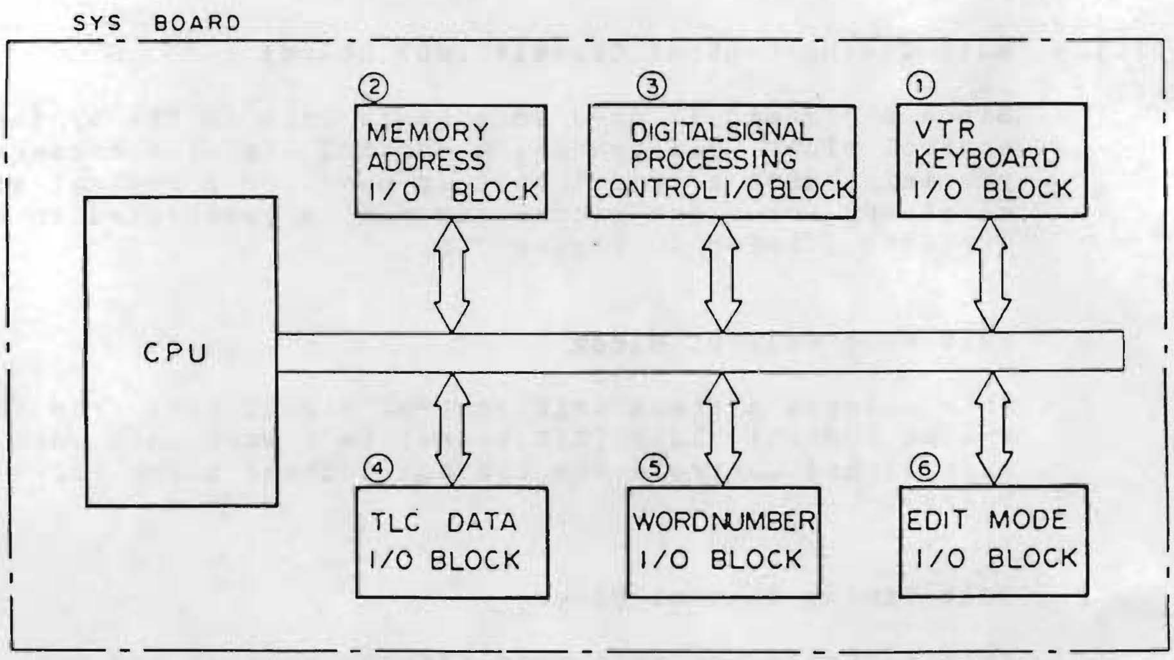


Figure 7-7

3 **Word Counter Block**

Word data, which is counted by a word counter to count the number of words in a frame for edit point setting, or a delay word counter used for preview and auto edit, or a cross fade start word counter block, is transferred to the system control block CPU (SYS board) via the word number bus.

4 **Edit Mode Address Counter Block**

This is a counter block prepared for the memory used for preview and auto edit. Address data generated under the control of the edit timing control block (EDT board) is output to the address bus by a control signal sent from the bus control block (SC-B board).

7.1.6. System Control Circuit

This generates a control signal for each block in accordance with keyboard input, and at the same time generates display data for the keyboard.

Also, it controls the VTR, memory block and signal system for editing in frame unit, and arithmetic operations for editing.

The control and the operation are performed by the CPU (SYS board) with 12K byte-software. Each signal is input/output via the I/O port...Refer to Figure 7-7. Since synchronization is required for TLC data transfer to and from the TLC board CPU, CPU block is supplied from the timecode generator/reader block (TLC board).

Each I/O port is as follows:

1 **VTR, keyboard I/O block**

I/O port for VTR remote, keyboard interface block.

2 **Memory Address I/O Block**

I/O port for address data transfer to and from the search control address block (SC-A board).

3 **Digital Signal Processing Control I/O**

I/O port for transmitting such data as cross fade signals, search control signals or parallel fader data to and from the digital signal processing control circuit (SC-A SC-B board).

4 **TLC Data I/O Block**

I/O port for transmitting such data as timecode data (used for timecode display, editing, auto locate, etc.) VTR status or VTR command data to and from the timecode generator/reader circuit CPU (TLC board).

5 **Word Number I/O Block**

I/O port for transmitting word data necessary for editing to and from the word counter block (EDT board).

The word data is composed of 14 bits.

6 **Edit mode I/O Block**

I/O port for transmitting a frame unit control signal to and from the edit mode control block (EDT board).

7.1.7. Video Signal Circuit (EDT Board)

Transfers video signals between the player/recorder VTR and the digital audio processor...Refer to 7-8.

1 **Video Analog Block**

Video signals from each VTR and the digital audio processor are selected by the video selector and become video out signals via the video amplifier.

Select signals are input from the system control block (SYS board). Since frame synchronization is produced in the edit timing control block (EDT board), a video signal at VTR change-over is changed-over in a frame unit.

2 **Frame Separator Block**

This generates a reference frame clock, which will be a reference signal or each block control, based on a video signal from the digital audio processor.

The reference frame clock is supplied to the edit timing control block (EDT board) or the timecode generator block (TLC board) and becomes a frame unit control signal or a CPU interrupt signal.

7.1.8. VTR Remote, Keyboard Interface Circuit (SYS Board)

This is an interface circuit between the keyboard and the CPU (SYS board), or between the VTR and the CPU (SYS board).

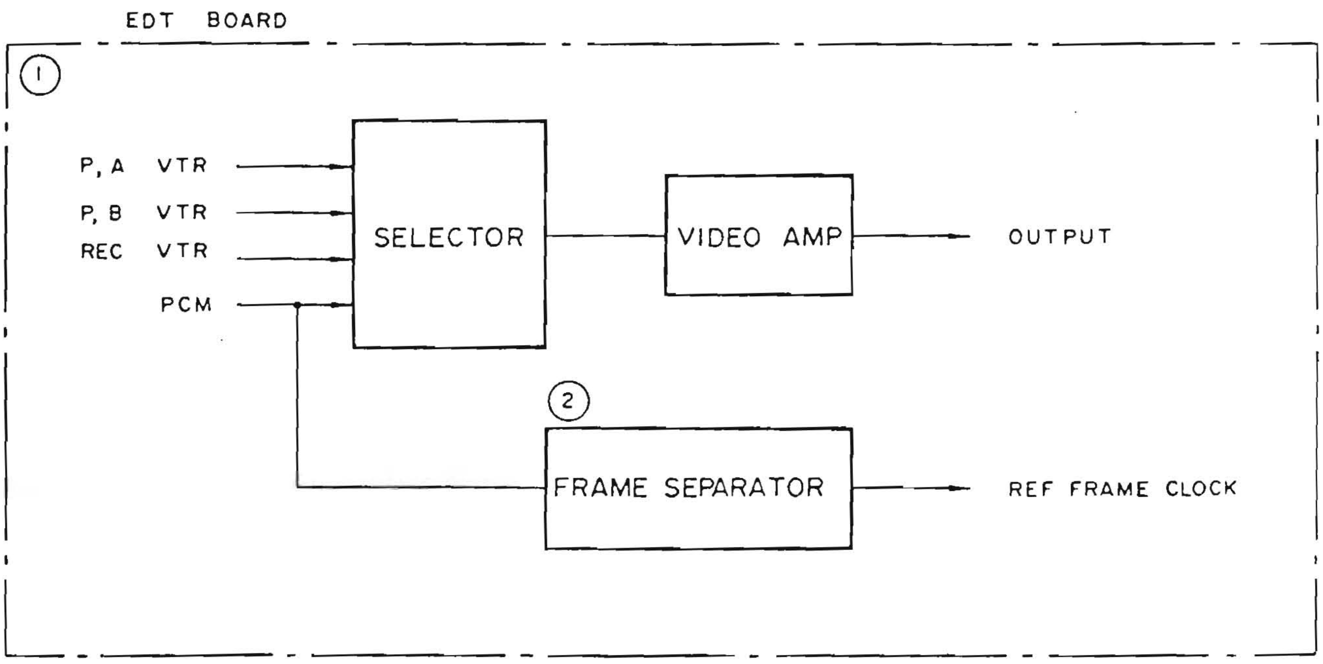

EDT BOARD
1
P, A VTR
P, B VTR
REC VTR
PCM
SELECTOR
VIDEO AMP
OUTPUT
2
FRAME SEPARATOR
REF FRAME CLOCK

Figure 7-8

1 **Keyboard Interface Block**

This interrupts the CPU (SYS board) with key data (synchronized with transmission clock and sync) sent from the keyboard. At the same time, it latches the key data and supplies it to the keyboard I/O (SYS board). Also, it converts fader data (S P) and supplies it to the gain control block (SC-A board).

Display data from the keyboard I/O (SYS board) is written into the display RAM and output to a specified slot in sync.

2 **VTR Interface Block**

This inputs a VTR status signal, or outputs a VTR command signal according to the VTR I/O (SYS board).

This signal is sent to the remote connector or each VTR through the static protection circuit (I/O board). The CTL signal among the remote signals is supplied to the timecode reader block (TLC board).

7.1.9. Power Supply Circuit (PLPS Board)

This outputs the following rated voltage and max output current for an input voltage of AC 90.0 - 132V (AC 198 - 264V by voltage select operation), and input frequency 47Hz - 63Hz.

Rated Voltage	Max. Output Current
DC + 5 ±0.15V	25A
+12 ±0.3	2A
-12 ±0.3	1A
+15 +4.0 / -0	2A UNREG.

Voltage is supplied to each board as follows:

+12V output: Supplied to the sync generator block (SC-A board), Memory circuit (MEM board) and Video Signal circuit (EDT board).
-12 output: Supplied to the Memory circuit (MEM board).
+15V output: Supplied to the keyboard.
+ 5V output: Supplied to all circuits

7.2 KEYBOARD UNIT

7.2.1 Keyswitch, display matrix circuit outputs (SW-1 and SW-2 boards).

The SW-1 board consists of REC VTR remote key, edit key, ten-key and the display, and the SW-2 board consists of player A, player B VTR remote key and the display.

Since many keys are provided and many display operations are performed, each circuit employs a matrix structure. Generate the key data or display are performed on a timesharing basis.

7.2.2. Key Data Encode/Display Data Decode Circuit (CNT Board)

In the key data encode block, an address generated by the counter of the timing generator block (CNT board) is scanned as a row/column selector. Key data from the key switch matrix block is converted into 256 slot transmission format, and sent to the DAE-1100 unit synchronized with transmission clock.

The display data decode block also converts transmission format display data sent from the DAE-1100 unit to the parallel data, and stores the converted data in the display data memory cicuit. The data is read-out by the timing control block (CNT board), and displayed in timesharing mode by driving the cathode and anode of each LED.

7.2.3. Timing Generator Circuit (CNT Board)

This controls the key data encode block and the display data decode block (CNT board) in accordance with a transmission clock and transmission synchronizing signal sent from the **DAE-1100** unit, and generates transmission serial format data and matrix format data.

7.2.4. Search Clock Generator Circuit (SD Board)

This generates search clock signals 01 and 02, and sends them to the waveform shaping cirucit. There is a 90° phase difference between 01 and 02, and the frequency is proportional to the rotational frequency of the search dial.

7.2.5. Search Clock Waveform Shaping Circuit (SR-PW Board)

This generates a rectangular waveform without jitter based on the search clock signals 01 and 02 sent from the search clock generator circuit, and sends it out to the DAE-1100 unit.

7.2.6. Fader Data Encode Circuit (CNT Board)

This converts 8-bit digital data sent from the fader into transmission serial format data, and sends to the DAE-1100 unit in sync with transmission clock, under control of the timing generator block (CNT board).

7.2.7. Power Supply Circuit (SR-PW Board)

This outputs the following rated voltage and max output current for an input voltage of DC15 +4 -1V from the DAE-1100 unit.

Rated Voltage	Max. Output Current
DC + 5V	3A
DC +12V	40mA
DC -12V	40mA

Voltage is supplied to each board as follows:

±12V Output: Supplied to the search clock generator circuit and the search clock waveform shaping circuit.

+ 5V: Supplied to all circuits

7.3 SIGNAL FLOW FOR VARIOUS MODES

The **DAE-1100** has the following modes of operation:

7.3.1. RAM CLEAR MODE
7.3.2. STRAIGHT MODE (REC STRAIGHT)
(PB STRAIGHT)
7.3.3. SEARCH MODE (REC STRAIGHT)
(PB STRAIGHT)
7.3.4. MUTE OUTPUT MODE
7.3.5. REC RAM WRITE MODE
7.3.6. PB RAM WRITE MODE
7.3.7. DELAY MEASURE MODE
7.3.8. EDIT MODE
7.3.8-1. EDIT 1
7.3.8-2. EDIT 2
7.3.8-3. EDIT 3
7.3.8-4. EDIT 4

Here the signal flow through the **DAE-1100** in various modes will be explained with reference to Figure 7-9.

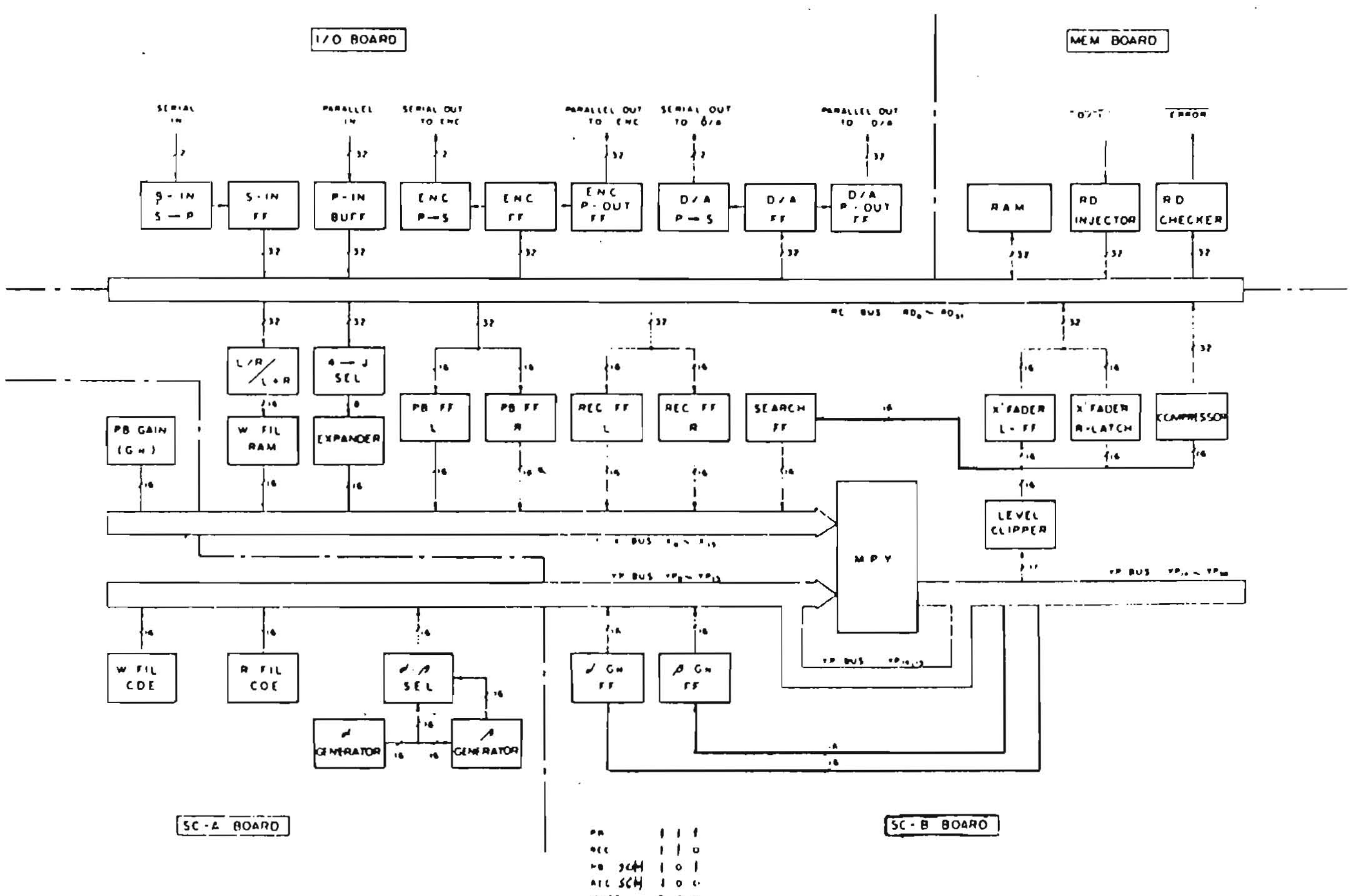


Figure 7-9 DAE-1100 SIGNAL FLOW

For details of each block, refer to the descriptions for the respective circuit boards.

The **RAM** of the **MEM** board is used as the **SEARCH RAM** in the **STRAIGHT** mode (2) and the **SEARCH** mode (3), and as the **REC RAM**, **D/A RAM**, **PB RAM**, and **SYNC RAM** in the **REC RAM WRITE** mode (6), **PB RAM WRITE** mode (7), and **EDIT** mode (9).

7.3.1. RAM CLEAR MODE

This mode must be selected at least once whenever shifting to the **STRAIGHT** mode from another. This mode prevents the appearance of carry-over noise in the **SEARCH** mode created by the **SEARCH RAM** from its use as **RAM** for other functions.

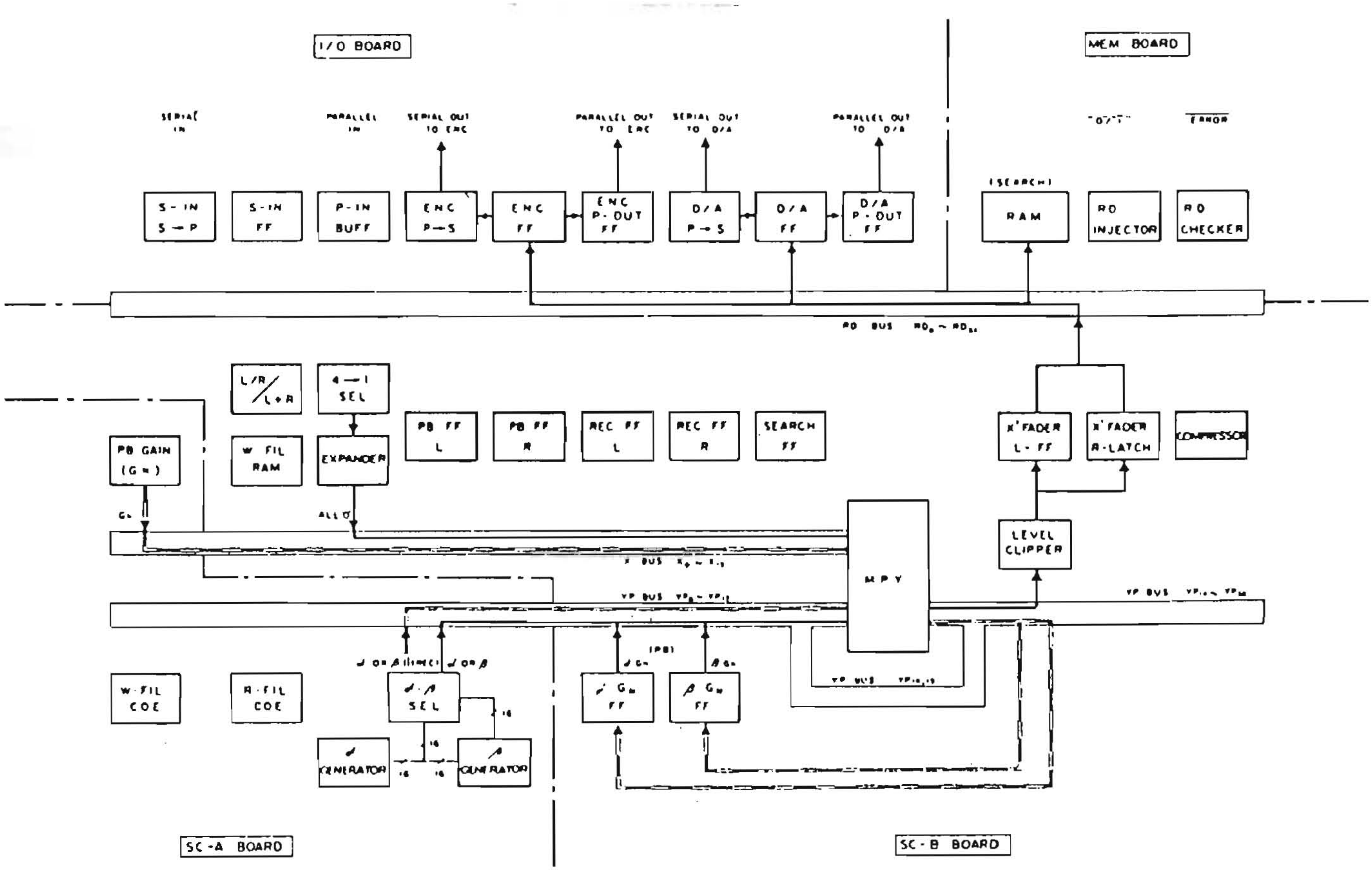


Figure 7-10 RAM CLEAR MODE

While the **REC VTR** is being selected, 16 "0" bits output from the (4 -->1) SEL, **EXPANDER** to the **X BUS**, and a or B output from the a, B **SEL** to the **YP BUS** are input to the **MPY**, and it output "0" is written in the **RAM** and simultaneously output to the **D/A FF**, and **ENC FF**.

While **PLAYER VTR** is being selected, a **GN** and B **GN** are used as the coefficients, instead of a and B, but the result is the same.

7.3.2. STRAIGHT MODE

In this mode, 1) data which has been compressed for use in the **SEARCH** mode is written in the **SEARCH RAM**, 2) the inputted data is returned as it is while **REC VTR** is being selected, and 3) data controlled by the **FADER** is sent back, while **PB VTR** is being selected.

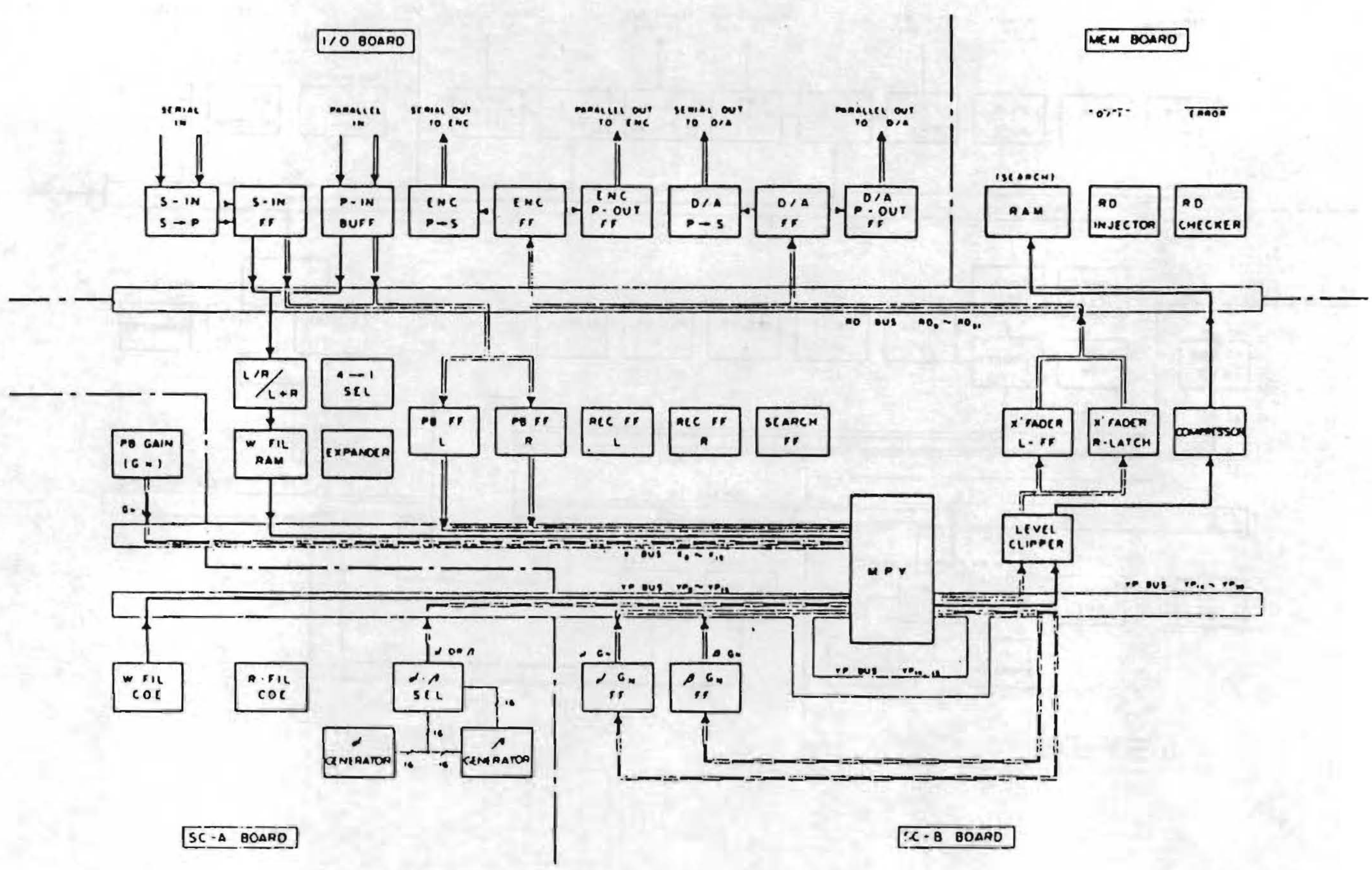


Figure 7-11 STRAIGHT MODE

(1) -->Writing into **SEARCH RAM**
(2) -->Data is output (instead of a GN and B GN, a and B are used).
(3) -->Calculation of a GN or B GN and data is output through --->.

7.3.3. SEARCH MODE

In this mode, the compressed data stored in the **SEARCH RAM** in the **STRAIGHT** mode is read, expanded, interpolated, and multilplied by coefficients before being output to the I/O board. The coefficients are a and B for **REC VTR** data, and a GN and B GN for **PB VTR** data.

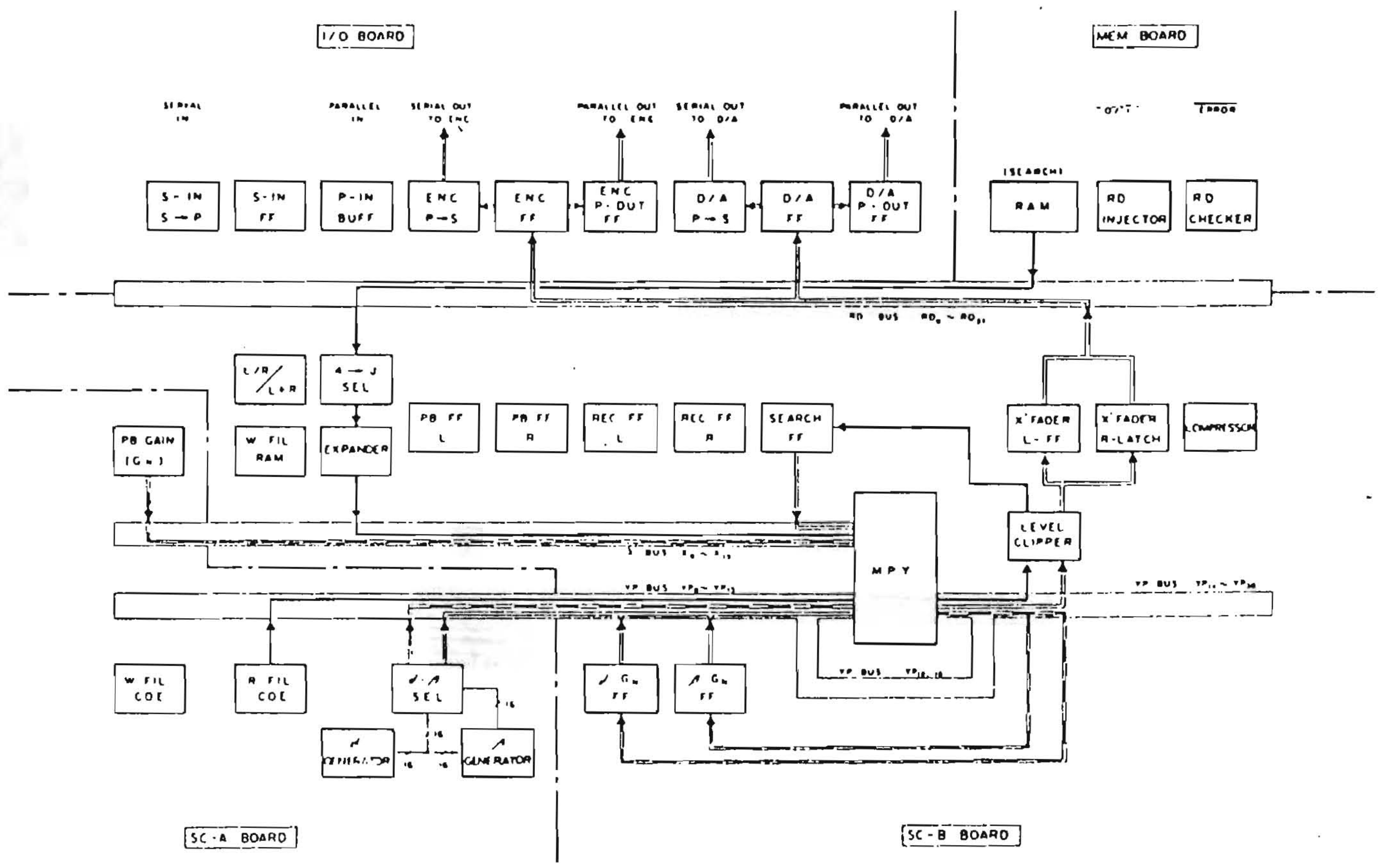


Figure 7-12 SEARCH MODE

The compressed data read-out from the **SEARCH RAM** is converted into 16-bit data in the (4-->1) **SEL** and **EXPANDER**, input to the MPY together with the R. **FIL** coefficient interpolated and stored in the **SEARCH FF.** Then they are again input to the **MPY** together with the coefficients (a, B, a GN, B GN), and are output to the I/O board.

Coefficients a GN and B GN are formed from GN and a or B in advance, and stored in the a GN FF and B GN FF.

7.3.4. MUTE OUTPUT MODE

This is the mode where the **VTR** is in the output status, but not in X1 **FWD** status. In this mode nothing is being performed except that **MUTE** data (all "0"'s) is output to the I/O board.

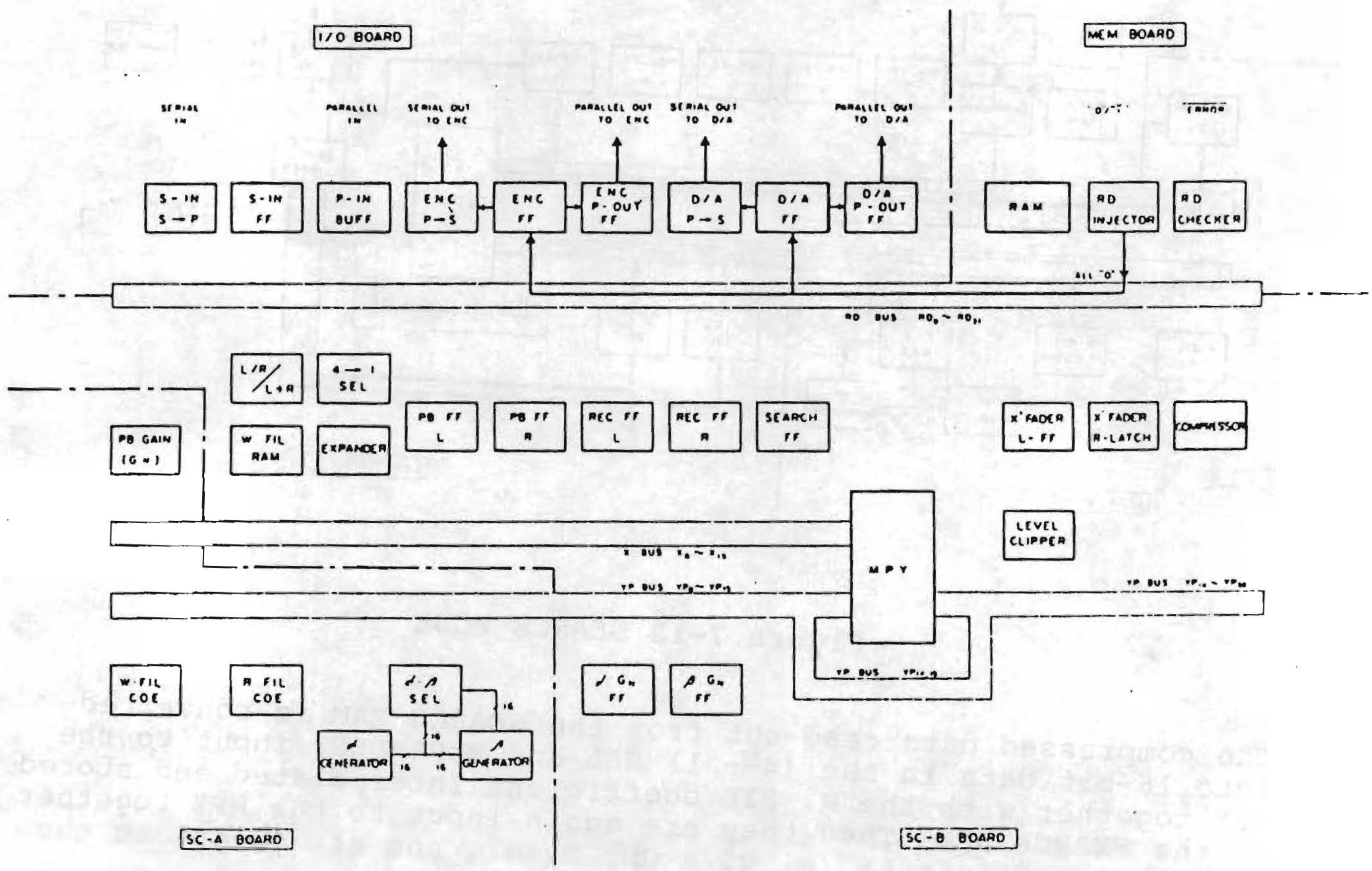


Figure 7-13 MUTE OUTPUT MODE

7.3.5. REC RAM WRITE MODE

See the description below for the REC RAM WRITE mode as these modes are very similar with the exception of the source VTR.

7.3.6. PB RAM WRITE MODE

In these modes, data is written into the **REC RAM** and **PB RAM** for use in the **EDIT** mode. In these modes, **MUTE** data is output as monitor sound.

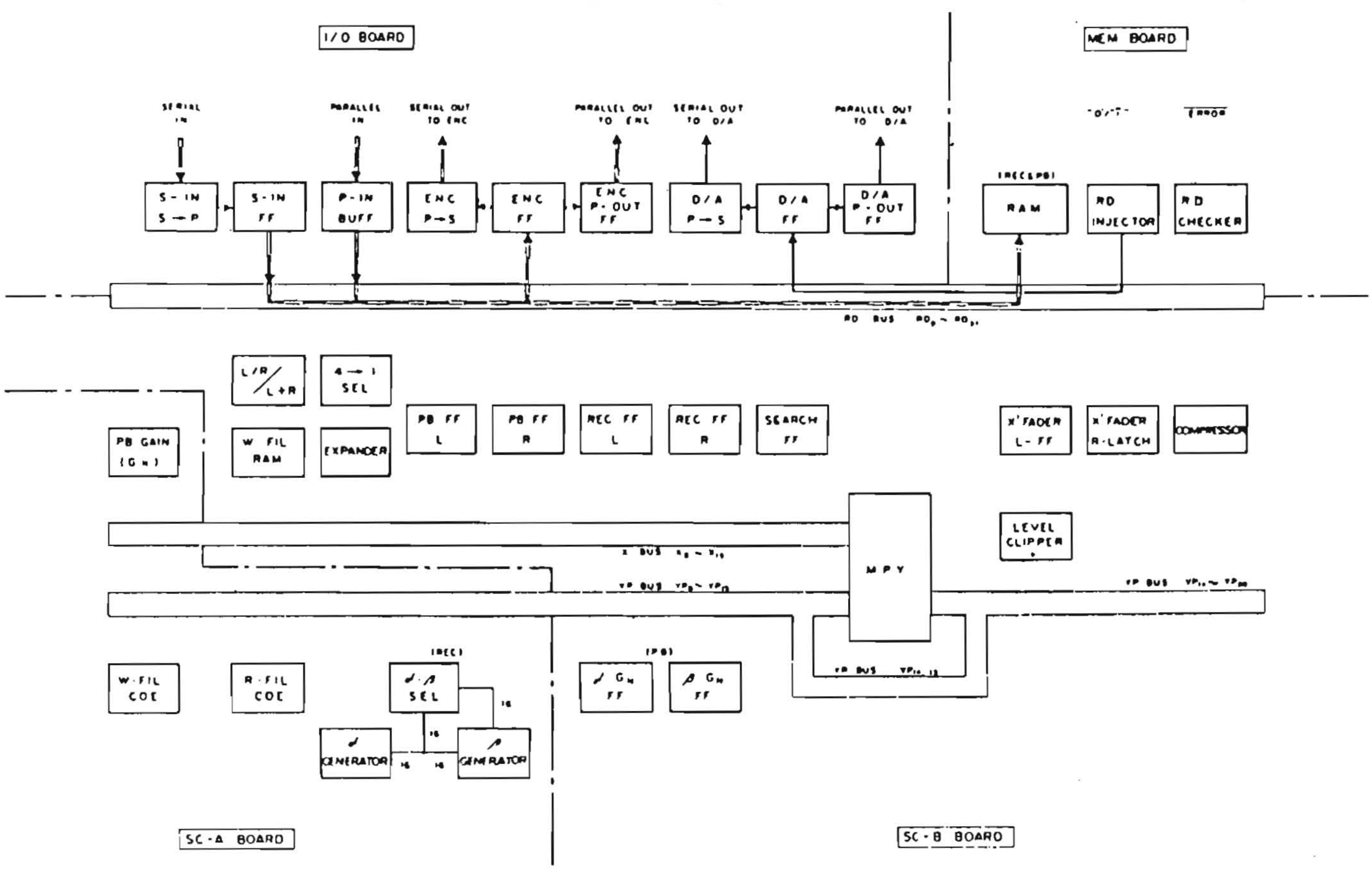


Figure 7-14 REC RAM/PB RAM WRITE MODE

7.3.7. DELAY MEASURE MODE

In this mode, the **PCM** processor data delay is measured for use in the **EDIT** mode.

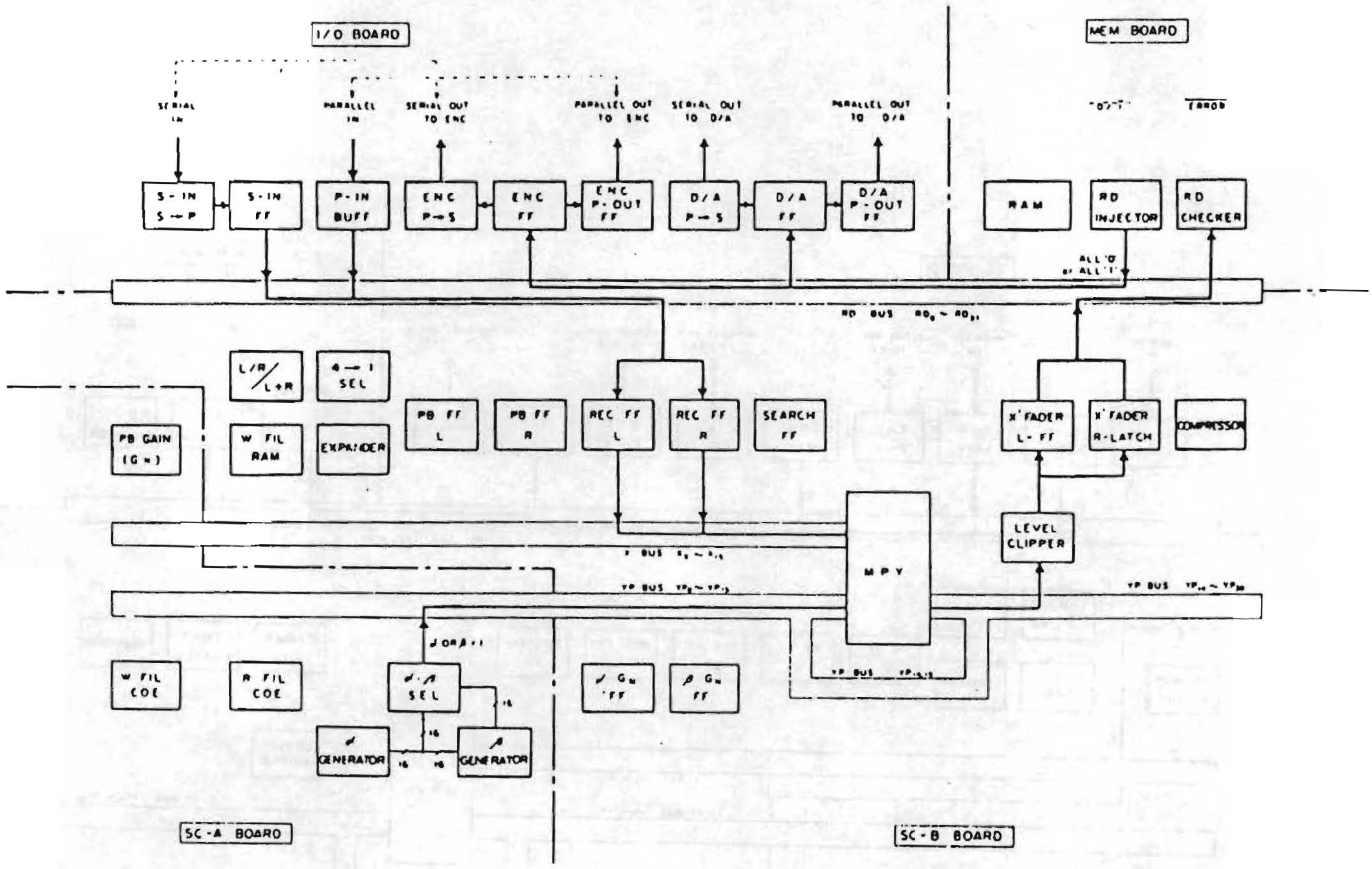


Figure 7-15 DELAY MEASURE MODE

The all "0"'s or all "1"'s data output from the **RD INJECTOR** of the **MEM** board to the **RD BUS** are sent to the **PCM** processor via the **ENC FF**, returned to the **RD BUS** via the S-IN FF or P-IN Buffer, and output to the **X BUS** of the **MPY** via the **REC FF**. At this time since the **YP BUS** data (a or B) is 1, the output from the **MPY** is equal to the **X BUS** input data.

Therefore, when it is output to the RD BUS via the **LEVEL CLIPPER**, **X'FADER L-FF**, and **X'FADER R-LATCH** and sent to the **RD CHECKER** on the **MEM** board, the data delay time between the **PCM** processor and the **EDITOR** can be measured.

7.3.8. EDIT MODE

The **EDIT** mode is for editing. The **EDIT** mode comprises four modes: **EDIT** 1 through **EDIT** 4, and they are executed in the sequence **EDIT** 1 - **EDIT** 2 - **EDIT** 3 - **EDIT** 4 - **EDIT** 3. For details refer to the description of the **EDIT** board.

8-1 EDIT 1 MODE

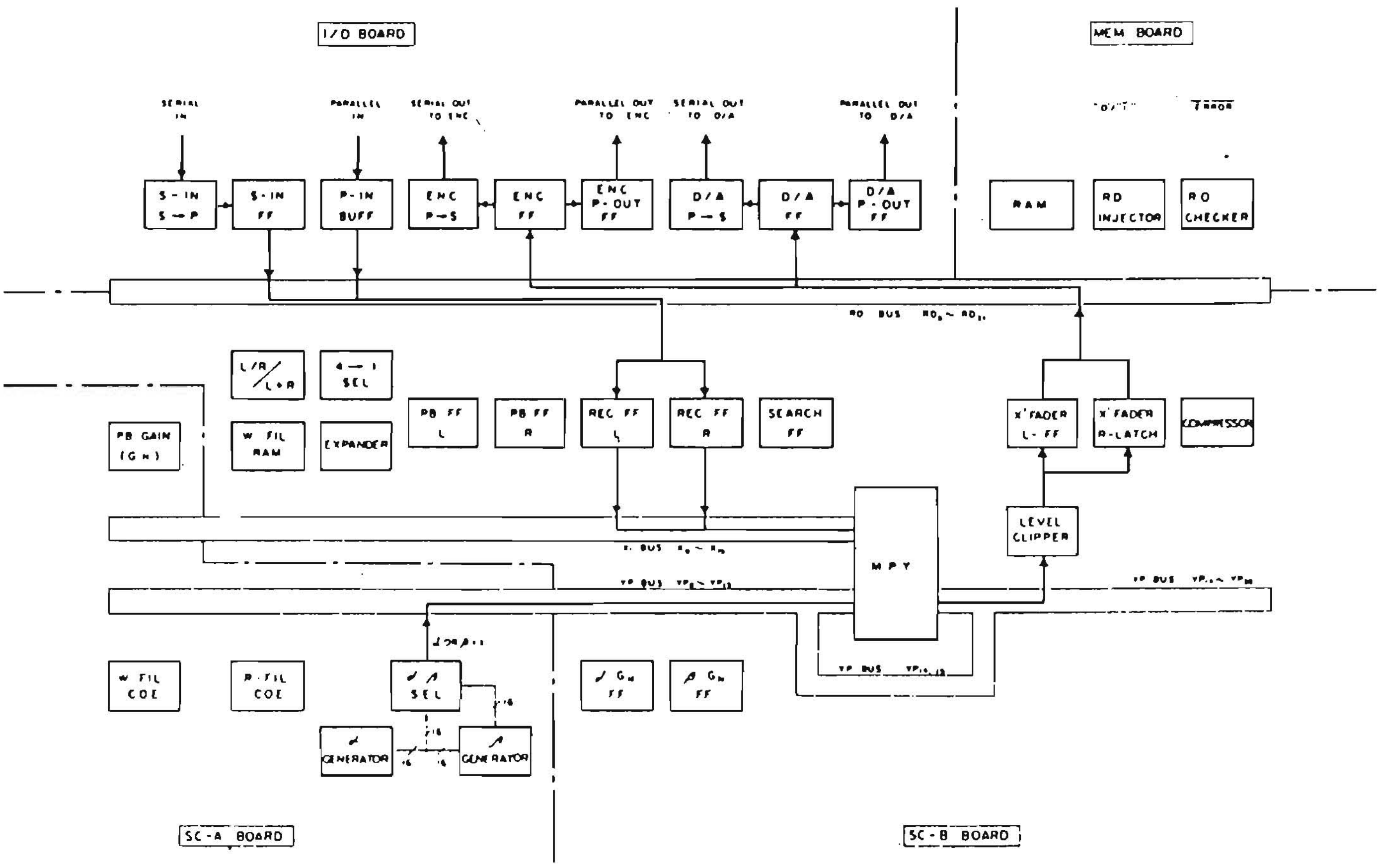


Figure 7-16 EDIT 1 MODE

The input data (RECORDER) from the I/O board is output to the X BUS bia the REC FF and is input to the MPY together with a or B (=1) on the YP BUS. The same input data is output to the ENC FF and the D/A FF.

7.3.8.2 EDIT 2 MODE

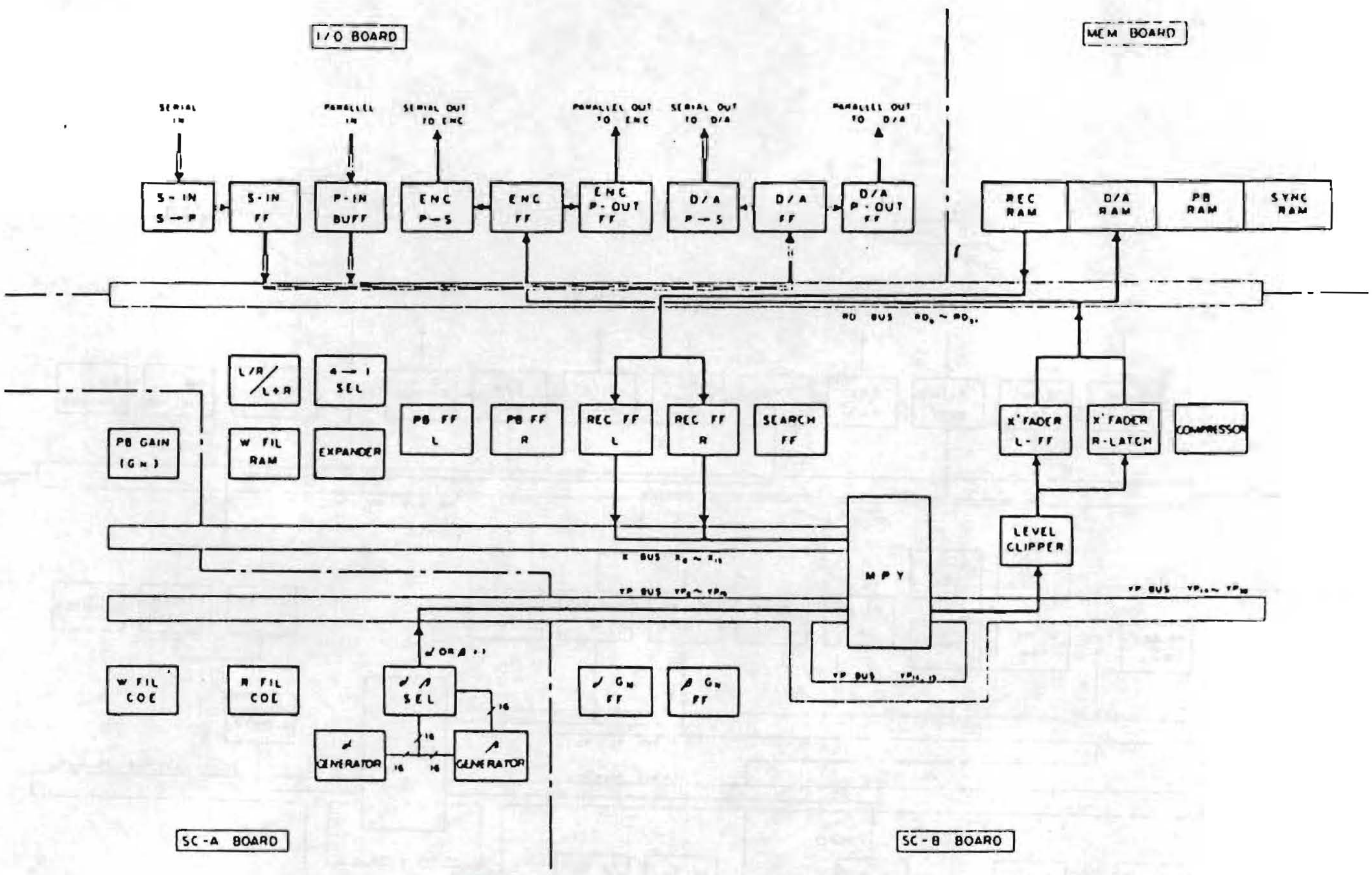


Figure 7-17 EDIT 2 MODE

The data read out of the REC RAM goes through the REC FF is multiplied by coefficient 1 in the MPY and written in the D/A RAM. At the same time, it is output to the ENC FF. At this time, the input data is selected as the input data for the D/A FF.

7.3.8.3 EDIT 3 MODE

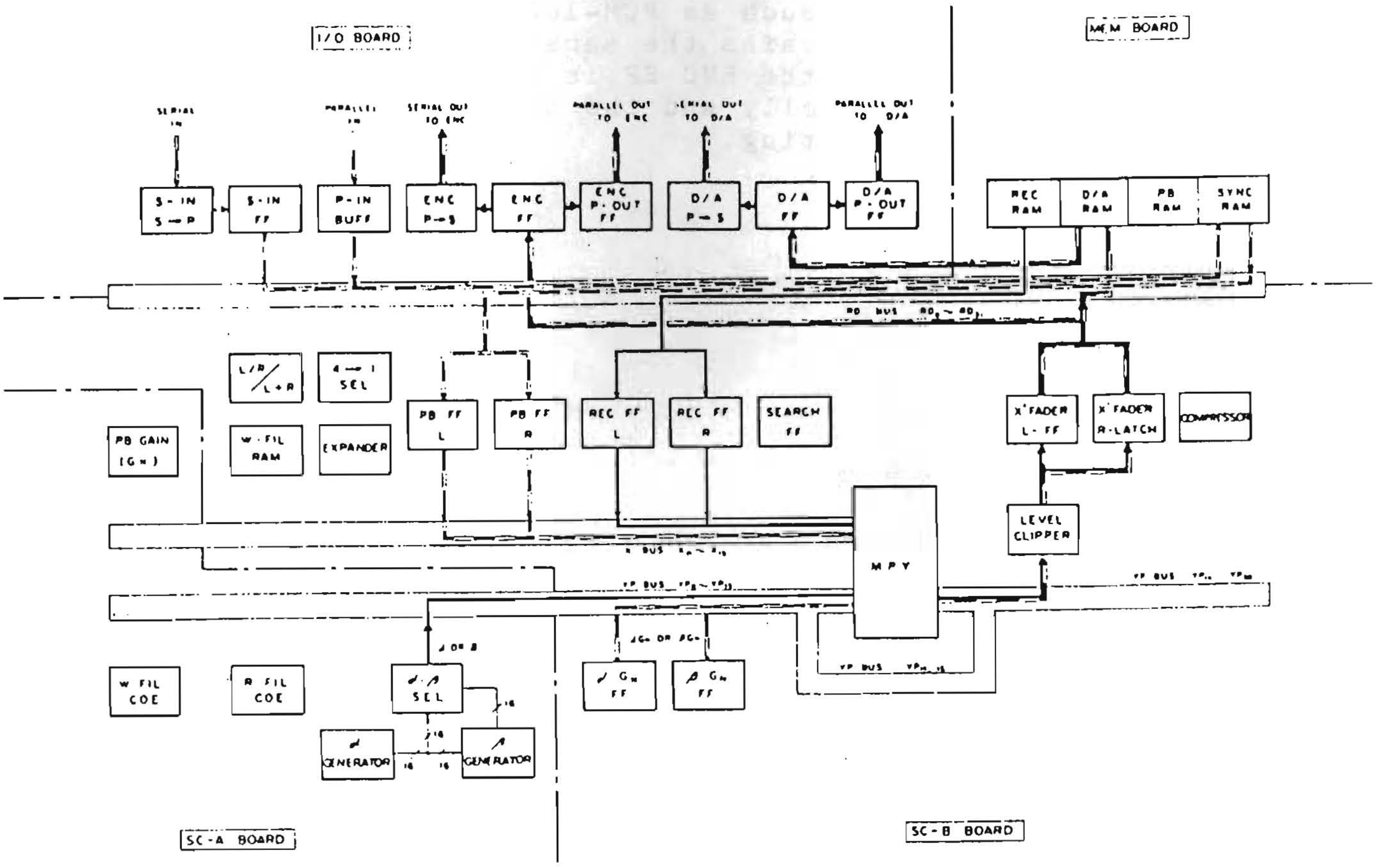


Figure 7-18 EDIT 3 MODE

The data read out from the REC RAM goes through the REC FF and is multiplied by coefficient a or B in the MPY.

On the other hand, the PB VTR dat input is written first into the SYNC RAM delayed by a time corresponding to the SYNC WORD, goes through the PB FF, and is multiplied by a GN or B GN in the MPY.

Both these values are added in the Accumulator of the MPY and are output to the ENC FF. At the same time, they are written in the D/A RAM, delayed for the DELAY WORD time, and output to the D/A FF for monitoring.

When a is selected as the coefficient for REC, the coefficient for PB is B GN. In this way, at first REC VTR data is output with a = 1 and B BN = 0, but as Cross-fading starts, a changes from 1 to 0 and B GN from 0 to GN, Cross-fading to PB VTR data.

7.3.8.4 EDIT 4 MODE

This mode is used as a means of eliminating errors caused by the use of convolution codes such as PCM-100. In this mode, with the Monitor (output to D/A remains the same as with EDIT 3) remaining unchanged, the output to the ENC FF is changed from X'FADE (EDIT 3) to PB RAM output digitally and the processor is set to the E-to E mode to prevent muting.

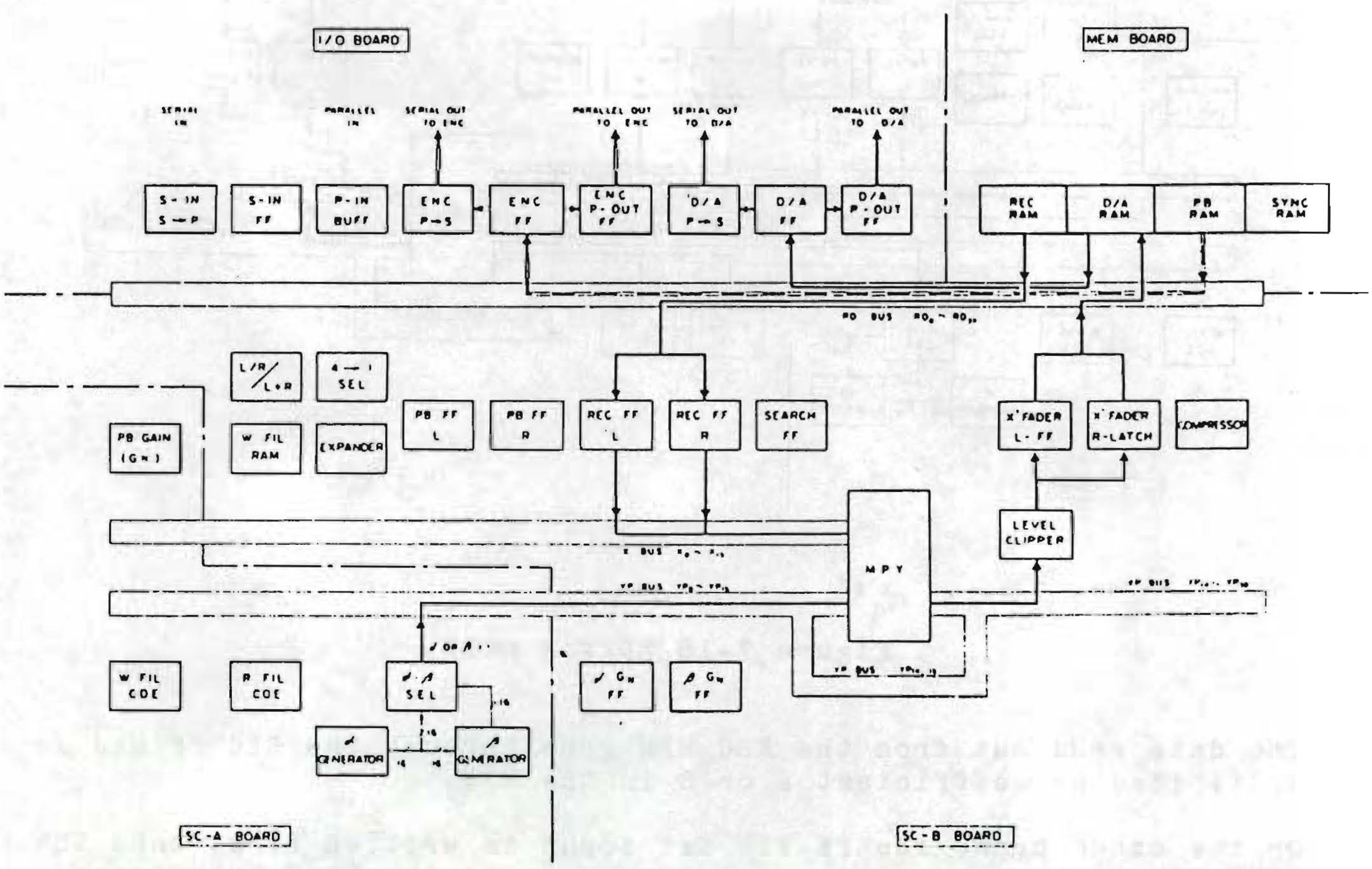


Figure 7-19 EDIT 4 MODE

7.4 SC-A BOARD

This board, working together with the SC-B board, receives the 2-channel main digital data (16 bits x 2) from the I/O board, processes in various editing modes, and returns it to the I/O board.

With the STRAIGHT mode, main digital data is output to the I/O board as it is if it is RECORDER VTR data, and output to the I/O board after being controlled by the FADER if it is PLAYER-VTR data. In this mode, 6 second compressed data, required in the SEARCH mode, is also written in to RAM on the MEM board.

In the SEARCH mode, the data written in the STRAIGHT mode is read at clock rate from the SEARCH DIAL, expanded, and output to the I/O board.

On this board, the REF WORD SYNC, input from the I/O board generates phase-locked clock with PLL.

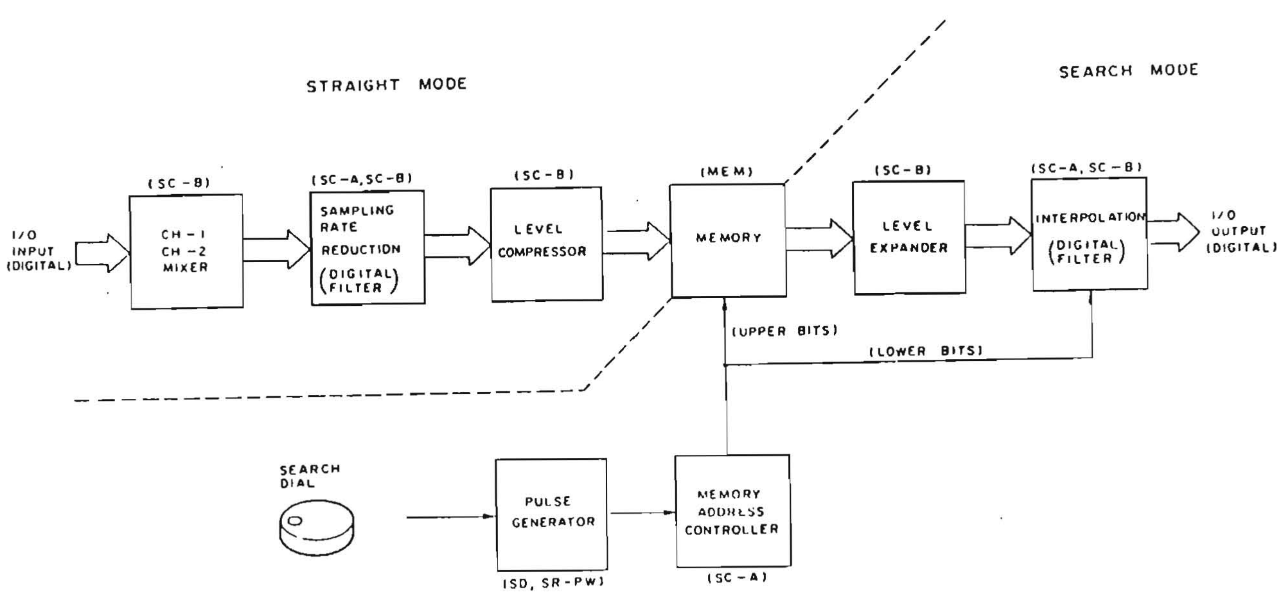


Figure 7-20 STRAIGHT MODE/SEARCH MODE

7.4.1 CONFIGURATION

A block diagram of the SC-A board is shown in Figure 7.21. As can be seen, the SC-A board comprises four major blocks from 1) through 4) as follows:

1) This block comprises PLL (1) for synchronizing the REF WORD SYNC from the I/O board, and a CLOCK REF WORD SYNC from the I/O board, and a CLOCK DIVIDER (inc. SYNC GENERATOR) (2) for dividing the 11.3 mHz master clock to obtain the system clock.

2) This block comprises the CROSS-FADE SPEED ROM (3) for determining the cross fade time from the signal received from the SYS board, the cross-fade coefficient (a) GENERATOR (4), the a a FLIP FLOP (5), the B (=1-a) GENERATOR (6), and the a, B SELECTOR (7).

3) This block comprises GAIN (LOG -->$\overline{\text{LIN}}$) (8) for converting Fader data (GAIN) received from the SYS board, and the PB GAIN FILTER (9) for eliminating noise generated when the gain is changed.

4) This block comprises an UP/DOWN DETECTOR (10) for discriminating forward and reverse rotations from the SEARCH DIAL clock received from the keyboard, a FLIP FLOP (11) which counts clock intervals by storing the counts of the FG PERIOD counter, a DIGITAL VCO (12) for generating pulses with frequencies proportional to the SEARCH DIAL clock, a SEARCH ADDRESS counter (13) for controlling the addresses in the SEARCH RAM, a SEARCH ADDRESS scanner (14) a SEARCH ADDRESS buffer (15), a scanning generator (16), a W-filter coefficient generator (17) for writing data in the SEARCH RAM, and R-filter coefficient generator (18) for reading from the SEARCH RAM.

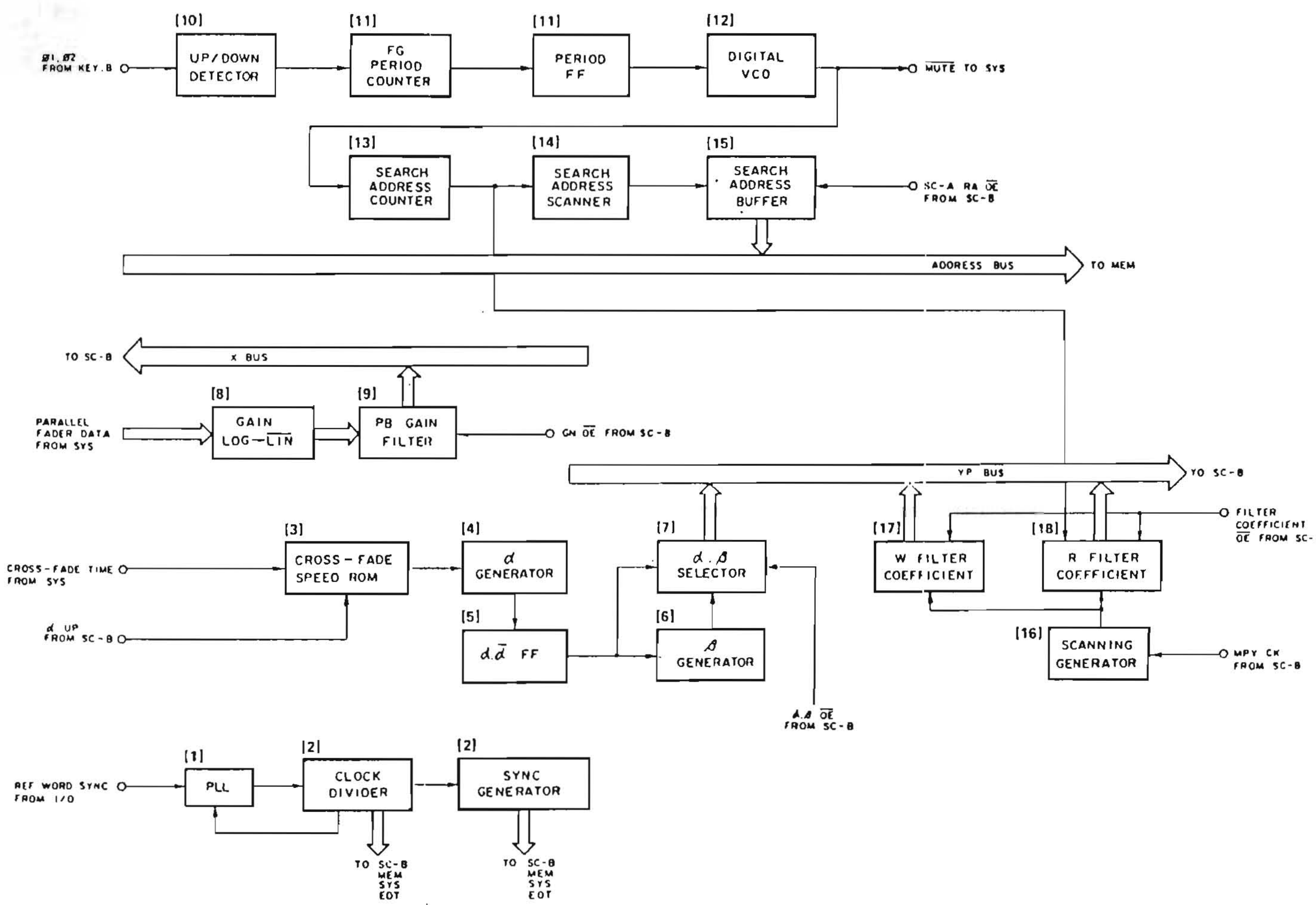


Figure 7-21 BLOCK DIAGRAMS (SC-A)

7.4.2. CIRCUIT DESCRIPTION

7.4.2.1. WORD CLOCK PLL

This is a phase-locking circuit for WORD clock synchronization in processing and transferring data in synchronization with a digital audio processor, i.e., PCM-1600, 1610, 1630 or 100. This circuit generates a master clock with a frequency of 11.3MHz which is 256 times the WORD clock frequency of 44.1kHz. The master clock frequency is divided by 256 and is phase-locked with the input REFERENCE WORD SYNC. Refer to Figures 7-22A and 7-22B.

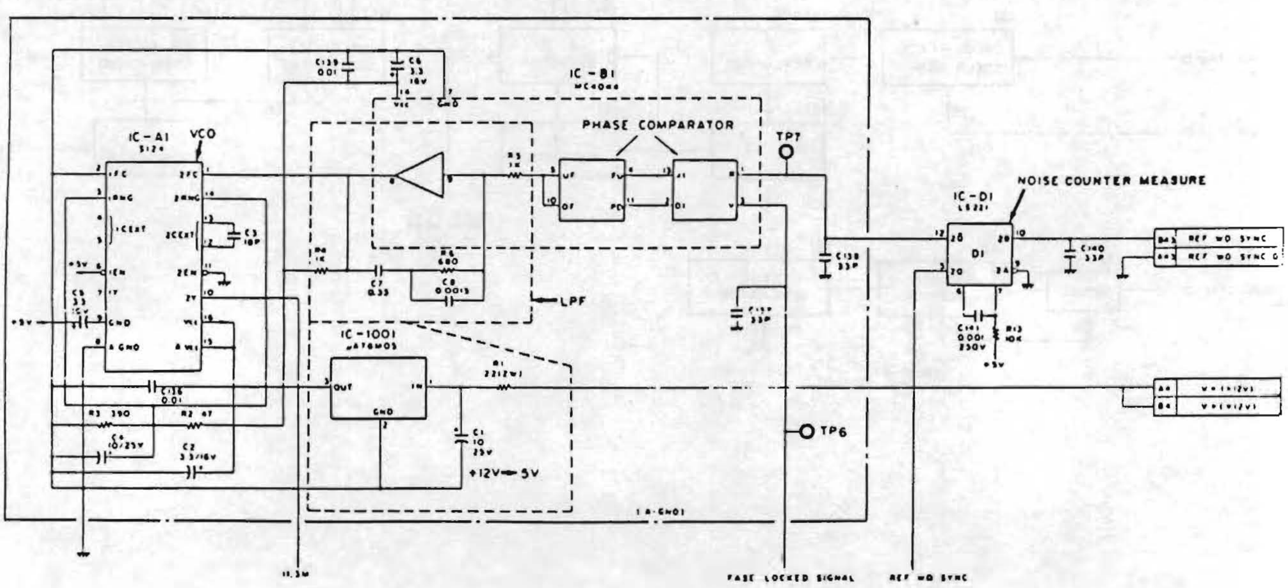


Figure 7-2A Word Clock PLL Circuit

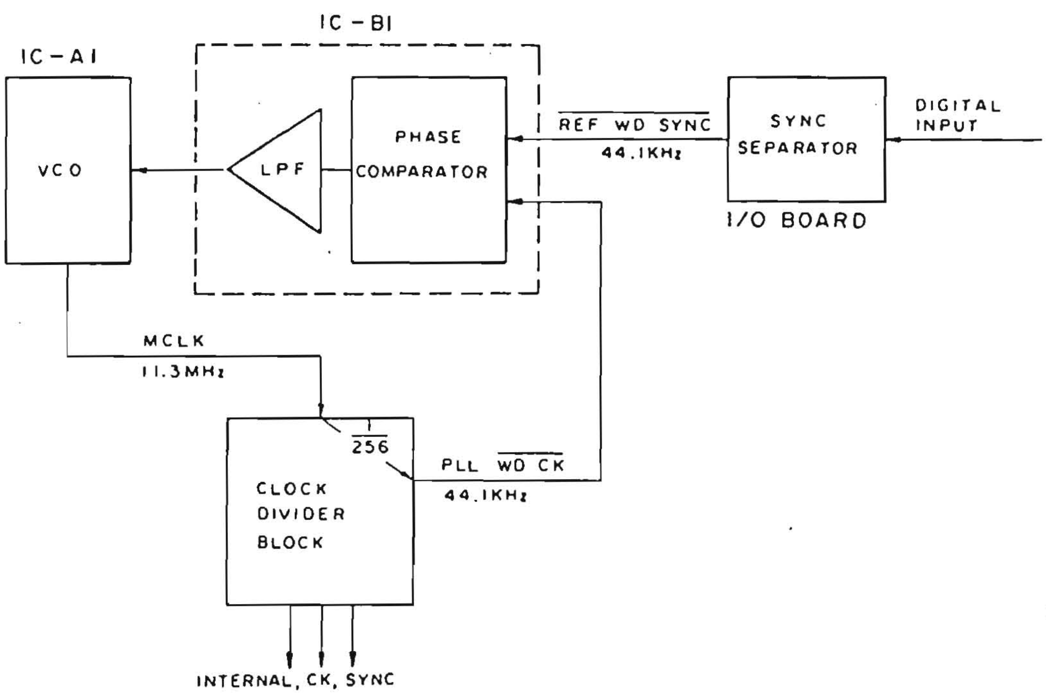


Figure 7-22B Word Clock PLL Diagram

7.4.2.2. CLOCK DIVIDER & SYNC GENRATOR BLOCK

In this block, 11.3mHz from the master clock PLL is divided to obtain the basic clocks for the respective boards. Refer to Figures 7-23A, 7-23B, 7-23C.

When the REF WORD SYNC is not phase-locked at PLL, noise may be produced. When failure to lock at PLL is detected, UNLOCK is output to the I/O board.

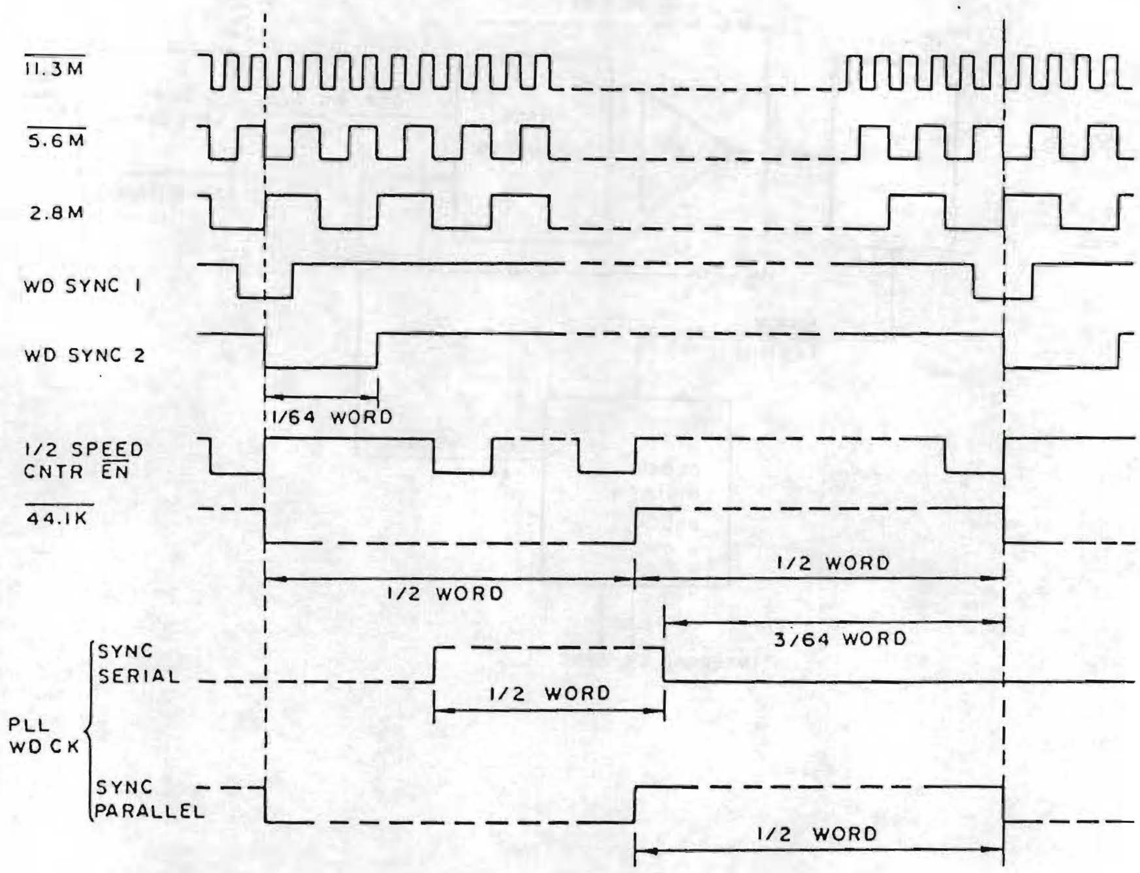


Figure 7-23A Basic clock

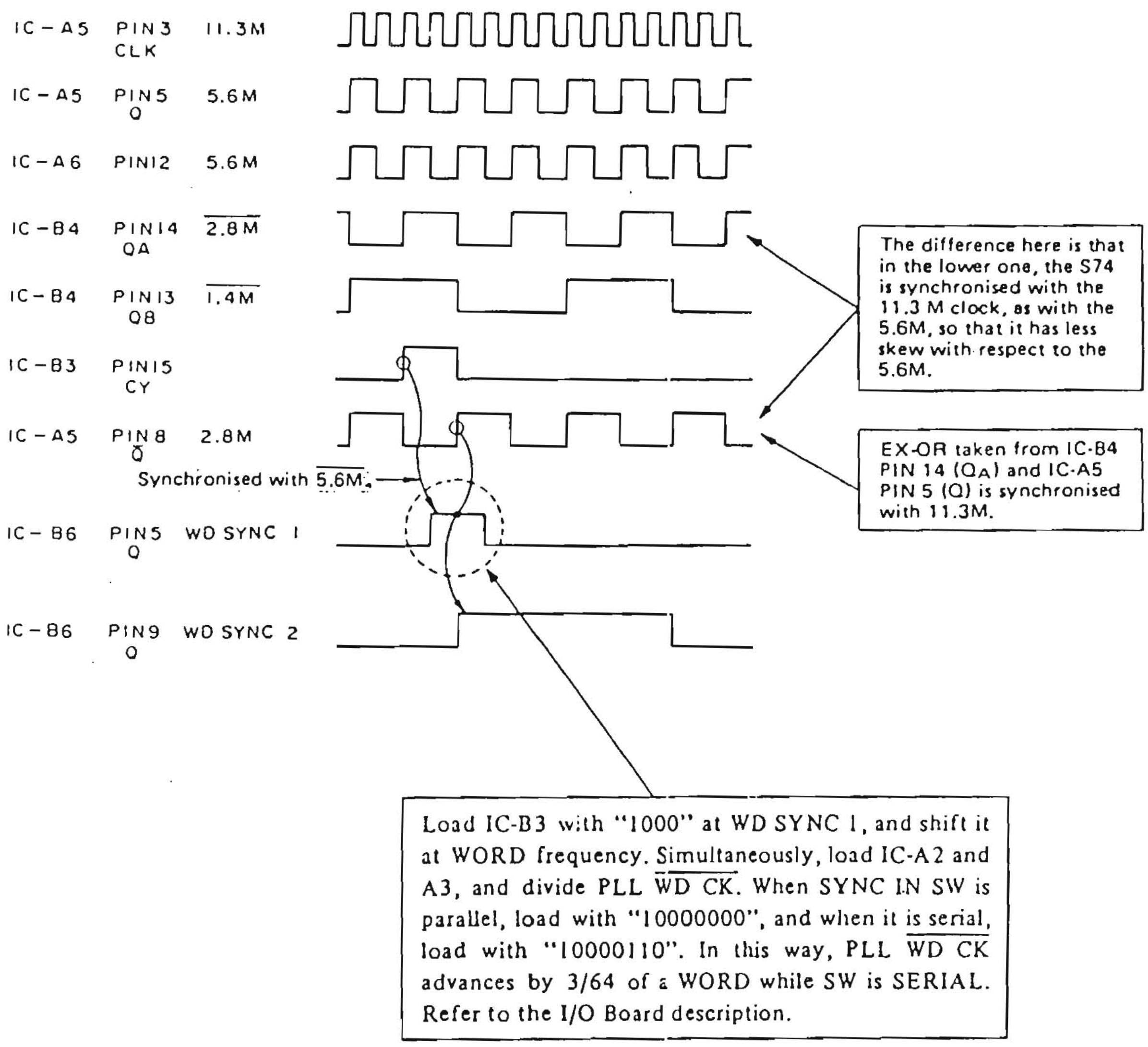


Figure 7-23B Frequency Dividing Process

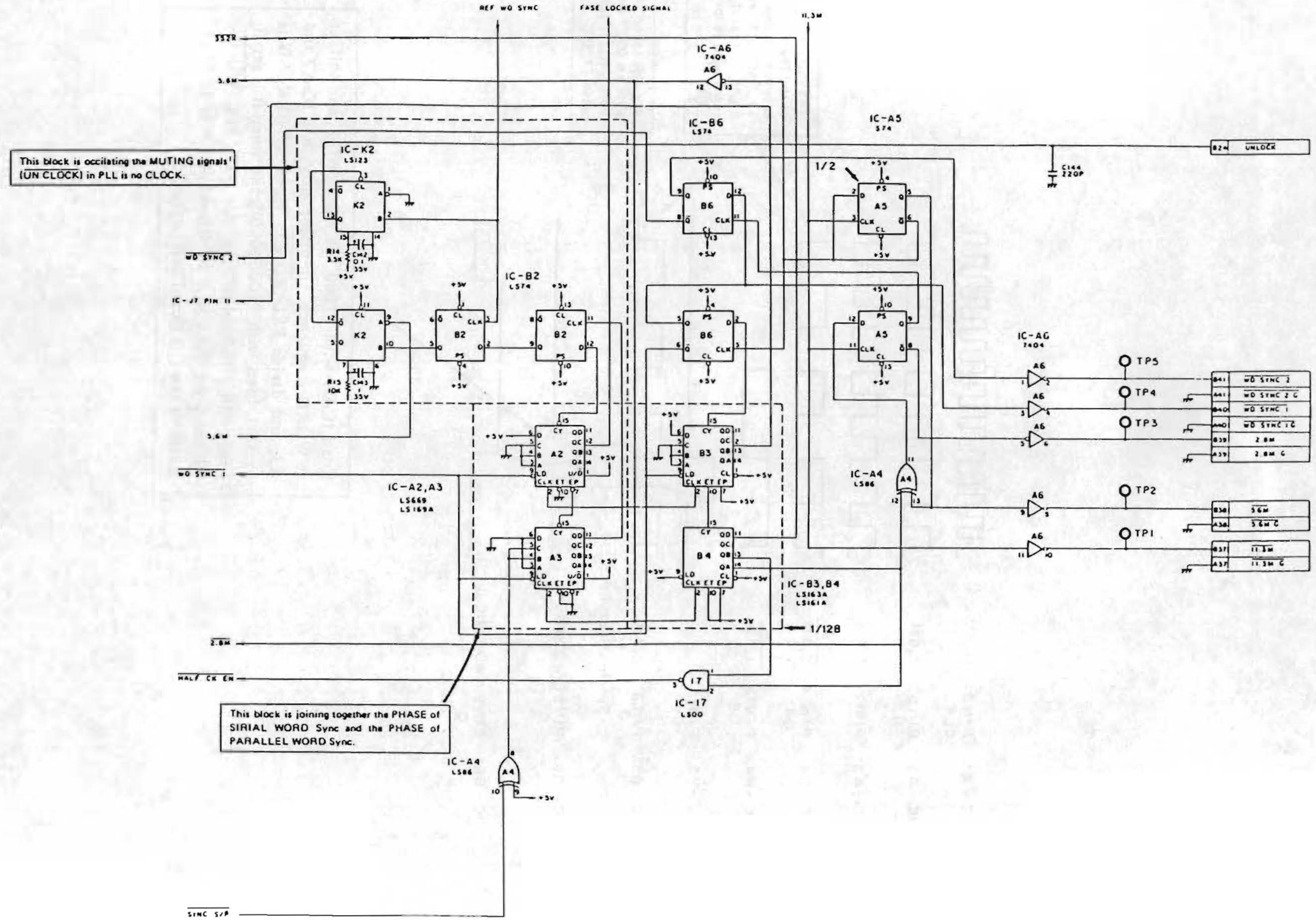


Figure 7-23C Clock Dividers & SYNC Generator Circuit

7.4.2.3. CROSS-FADING SPEED ROM

5-bit signals consisting of a 4-bit CROSS-FADING TIME SELECT signal form the SYS board and a 1-bit a UP signal are converted to bipolar CROSS-FADING SPEED signal each containing 9 significant bits in a total word length of 16 bits (2's complement). Each of them corresponds to a 1 word increment a for the cross-fader coefficient a.

Table 7-4-1 X'FADE SPEED ROM (IC-K7 S288)

ADRS	DATA (MOD 10)	DATA (MOD 16)	DATA BIT								X' FADE TIME	
	X		07	06	05	04	03	02	01	00	Y (msec)	Y' (msec)
0 0	186	B A	1	0	1	1	1	0	1	0	UP 1	(1.0)
0 1	93	5 D	0	1	0	1	1	1	0	1	UP 2	(2.0)
0 2	46	2 E	0	0	1	0	1	1	1	0	UP 4	(4.0)
0 3	26	1 A	0	0	0	1	1	0	1	0	UP 7	(6.9)
0 4	19	1 3	0	0	0	1	0	0	1	1	UP 10	(9.8)
0 5	12	C	0	0	0	0	1	1	0	0	UP 15	(15.5)
0 6	6	6	0	0	0	0	0	1	1	0	UP 30	(31.0)
0 7	4	4	0	0	0	0	0	1	0	0	UP 50	(46.4)
0 8	3	3	0	0	0	0	0	0	1	1	UP 70	(61.9)
0 9	2	2	0	0	0	0	0	0	1	0	UP 99	(92.9)
0 A	1	1	0	0	0	0	0	0	0	1		
0 B												
0 C												
0 D												
0 E												
0 F			0	0	0	0	0	0	0	1		
1 0	69	4 5	0	1	0	0	0	1	0	1	DOWN 1	(1.0)
1 1	162	A 2	1	0	1	0	0	0	1	0	DOWN 2	(2.0)
1 2	209	D 1	1	1	0	1	0	0	0	1	DOWN 4	(4.0)
1 3	229	E 5	1	1	1	0	0	1	0	1	DOWN 7	(6.9)
1 4	236	E C	1	1	1	0	1	1	0	0	DOWN 10	(9.8)
1 5	243	F 3	1	1	1	1	0	0	1	1	DOWN 15	(15.5)
1 6	249	F 9	1	1	1	1	1	0	0	1	DOWN 30	(31.1)
1 7	251	F B	1	1	1	1	1	0	1	1	DOWN 50	(46.4)
1 8	252	F C	1	1	1	1	1	1	0	0	DOWN 70	(61.9)
1 9	253	F D	1	1	1	1	1	1	0	1	DOWN 99	(92.9)
1 A	254	F E	1	1	1	1	1	1	1	0		(186)
1 B												
1 C												
1 D												
1 E												
1 F			1	1	1	1	1	1	1	0		

in UP $\frac{2^{14}}{2 \times 44100Y} \fallingdotseq \frac{0.37152}{2Y} \xrightarrow{\text{to near}} X$

in DOWN $Y' = \frac{2^{14}}{2 \times 44100X} \fallingdotseq \frac{0.37152}{2X}$

$X = 255 -$ in UP X

7.4.2.4. a GENERATOR

This generates the cross-fader coefficient an +1 for the next word by adding a output from the CROSS-FADING SPEED ROM and the current CROSS-FADER coefficient an.

7.4.2.5. a.$\bar{a}$FF

This circuit stores the output of the GENERATOR for the duration of 1 word and further clips the GENERATOR output with an.

upper limit of 0100000000000000 and
lower limit of 0000000000000000

The sequence is keep the output of thE GENERATOR at the upper limit value by learing all he bits in the lower 14 positions to 0. When the output increases so that the upper two bits reach 01, hold the upper two bits as 01 and keep the output at the lower limit value. When it decreases to the extent that the upper two bits reach 11, change the upper two to 00 and clear all the 14 _ lower bits to 0. These clear pulses are obtained from Pin 6 (1Q) of IC17 and are reset by WD SYNC 2 into Pin 1 of IC17 after the lower 14 bits are cleared.

7.4.2.6. GENERATOR

This circuit generates another_CROSS-FADER coefficient B by subtracting output a of the a.aFF from the upper limit "0100000000000000" of the CROSS-FADER coefficient. This subtraction is actually performed by the address using a as follows:

Upper limit value +$\bar{a}$ + 1

is Complement of a (all bits inverted)	Preset 1 on "Carry" input (o(Pin 7) of IC-411

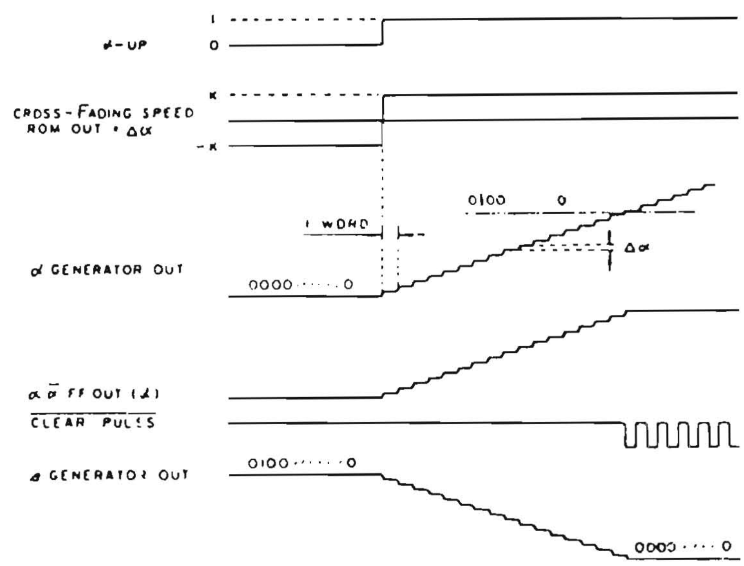


Figure 7-24 Operation from the CROSS-FADING SPEED ROM to the B GENERATOR

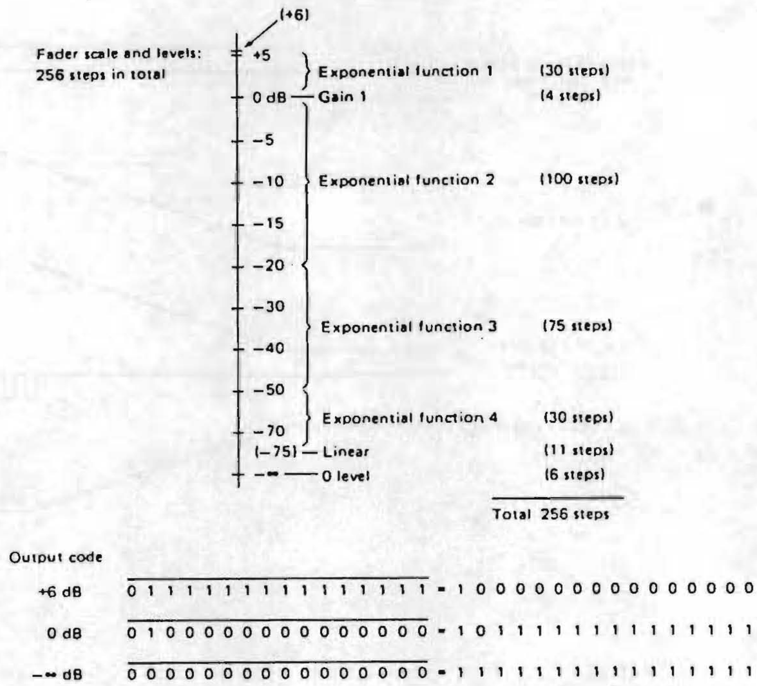
7.4.2.7. SELECTOR

The circuit outputs a and B to the Y-BUS in accordance with a/B signal and a, B, OE, received from the SC-B board.

7.4.2.8. GAIN LOG -->$\overline{\text{LIN}}$

This circuit converts 8-bit fader position data received from the GAIN OFFSET FADER via the SYS board into 16-bit LINEAR PB GAIN data in the PB GAIN ROM.

Input data on fader position is received in Gray code. The output signal is in 1's complement form which is linearly proportional to the gain which changes exponentially with fader position.



For OdB, "1" is output to 8Q (pin 19) of IC-C8 to drive the OdB display LED.

Among the 16 bits of PB GAIN $\overline{\text{LIN}}$, the MSB is always "1". Therefore, the lower 15 bits are added to the bit for the OdB display signal, and the total of 16 bits are written in 256 steps in the ROM IC-A8 (2716). As the ROM (2716) outputs 8-bit data, each of the 16 bit data are divided into two 8 bit data and are written in 512 addresses.

On fading latching, first "1" is input to the A8 address input of the ROM as a switching signal for MXP/LSP, and the OdB signal and the upper 7 bits are read out. Then, while storing them in the 8-bit FF IC-C8, "0" is input to the A8 address input to readout the lower 8 bits. Finally, the 15-bit gain signal is sent to the PB GAIN FILTER.

Table 7-4-2 PB gain (GN) ROM IC-A8 2716

STEP (DEC)	ADRS (HEXA) X□□	DATA (HEXA)	DATA (DEC)	GAIN (dB)	STEP (DEC)	ADRS (HEXA) X□□	DATA (HEXA)	DATA (DEC)	GAIN (dB)	STEP (DEC)	ADRS (HEXA) X□□	DATA (HEXA)	DATA (DEC)	GAIN (dB)	STEP (DEC)	ADRS (HEXA) X□□	DATA (HEXA)	DATA (DEC)	GAIN (dB)
0	00	7FFF	0	−∞	64	60	7F8E	113		128	C0	78A6	1881		192	A0	5FEC	8211	−6
1	1	7FFF	0	−∞	65	61	7F88	119		129	C1	787A	1925		193	A1	5F2C	8403	
2	3	7FFF	0	−∞	66	63	7F83	124		130	C3	784D	1970		194	A3	5E69	8598	−5.8
3	2	7FFF	0	−∞	67	62	7F7D	130	−42	131	C2	781F	2016		195	A2	5DA0	8799	−5.4
4	6	7FFF	0	−∞	68	66	7F77	136		132	C6	77F0	2063	−18	196	A6	5CD3	9004	−5.2
5	7	7FFF	0	−∞	69	67	7F70	143	−41.2	133	C7	77C0	2111		197	A7	5C02	9213	−5
6	5	7FFE	1	−84	70	65	7F6A	149	−40.8	134	C5	778F	2160		198	A5	5B2B	9428	−4.8
7	4	7FFE	1	−84	71	64	7F63	156	−40.4	135	C4	775D	2210		199	A4	5A4F	9648	−4.6
8	C	7FFE	1	−84	72	6C	7F5B	164	−40	136	CC	7729	2262		200	AC	596F	9872	−4.4
9	D	7FFE	1	−84	73	6D	7F53	172	−39.6	137	CD	76F5	2314	−17	201	AD	5889	10102	
10	F	7FFD	2	−78	74	6F	7F4B	180	−39.2	138	CF	76BF	2368		202	AF	579D	10338	−4
11	E	7FFD	2	−78	75	6E	7F43	188	−38.8	139	CE	7688	2423		203	AE	56AD	10578	
12	A	7FFD	2	−78	76	6A	7F3A	197		140	CA	764F	2480		204	AA	55B6	10825	
13	B	7FFD	2	−78	77	6B	7F31	206	−38	141	CB	7615	2538		205	AB	54BA	11077	
14	9	7FFC	3	−75	78	69	7F27	216		142	C9	75DA	2597	−16	206	A9	53B8	11335	
15	8	7FFC	3	−75	79	68	7F1D	226		143	C8	759E	2657		207	A8	52B0	11599	−3
16	18	7FFC	3	−75	80	78	7F12	237		144	D8	7560	2719		208	B8	51A2	11869	
17	19	7FFC	3	−75	81	79	7F07	248		145	D9	7521	2782		209	B9	508D	12146	
18	1B	7FFB	4	−72	82	7B	7EFB	260	−36	146	DB	74E0	2847		210	BB	4F72	12429	
19	1A	7FFB	4	−72	83	7A	7EEF	272		147	DA	749D	2914	−15	211	BA	4E51	12718	
20	1E	7FFB	4	−72	84	7E	7EE2	285		148	DE	745A	2981		212	BE	4D29	13014	−2
21	1F	7FFA	5	−70	85	7F	7ED5	298		149	DF	7414	3051		213	BF	4BFA	13317	
22	1D	7FFA	5	−70	86	7D	7EC7	312		150	DD	73CD	3122		214	BD	4AC3	13628	
23	1C	7FF9	6	−69.2	87	7C	7EB8	327	−34	151	DC	7384	3195		215	BC	4986	13945	
24	14	7FF9	6	−68.4	88	74	7EA9	342		152	D4	733A	3269	−14	216	B4	4841	14270	
25	15	7FF8	7	−67.6	89	75	7E99	358		153	D5	72EE	3345		217	B5	46F5	14602	−1
26	17	7FF8	7	−66.8	90	77	7E88	375		154	D7	72A0	3423		218	B7	45A1	14942	
27	16	7FF7	8	−66	91	76	7E76	393		155	D6	7250	3503		219	B6	4445	15290	
28	12	7FF6	9	−65.2	92	72	7E63	412	−32	156	D2	71FF	3584		220	B2	42E0	15647	−0.4
29	13	7FF5	10	−64.4	93	73	7E51	430		157	D3	71AB	3668	−13	221	B3	4174	16011	−0.2
30	11	7FF4	11	−63.6	94	71	7E3C	451	−31.2	158	D1	7156	3753		222	B1	BFFF	16384	0
31	10	7FF3	12	−62.8	95	70	7E26	473	−30.8	159	D0	70FE	3841		223	B0	BFFF	16384	0
32	30	7FF2	13	−62	96	50	7E10	495	−30.4	160	F0	70A5	3930		224	90	BFFF	16384	0
33	31	7FF1	14		97	51	7DF9	518	−30	161	F1	7049	4022		225	91	BFFF	16384	0
34	33	7FEF	16		98	53	7DE0	543	−29.6	162	F3	6FEC	4115	−12	226	93	3E81	16766	+0.2
35	32	7FEE	17		99	52	7DC7	568	−29.2	163	F2	6F8C	4211		227	92	3CFB	17156	+0.4
36	36	7FEC	19		100	56	7DAC	595	−28.8	164	F6	6F2A	4309		228	96	3B68	17556	
37	37	7FEA	21	−58	101	57	7D90	623		165	F7	6EC5	4410		229	97	39D2	17965	
38	35	7FE8	23		102	55	7D73	652	−28	166	F5	6E5E	4513		230	95	3830	18383	+1
39	34	7FE6	25		103	54	7D54	683		167	F4	6DF6	4617	−11	231	94	3684	18811	
40	3C	7FE4	27		104	5C	7D34	715		168	FC	6D8A	4725		232	9C	34CD	19250	
41	3D	7FE1	30	−54.8	105	5D	7D12	749		169	FD	6D1C	4835	−10.6	233	9D	330D	10698	
42	3F	7FDE	33	−54	106	5F	7CEF	784		170	FF	6CAB	4948	−10.4	234	9F	3142	20157	
43	3E	7FDB	36	−53.2	107	5E	7CCA	821	−26	171	FE	6C38	5063	−10.2	235	9E	2F6D	20626	+2
44	3A	7FD8	39	−52.4	108	5A	7CA3	860		172	FA	6BC2	5181	−10	236	9A	2D8C	21107	
45	3B	7FD4	43	−51.6	109	5B	7C7B	900		173	FB	6B49	5302	−9.8	237	9B	2BA1	21598	
46	39	7FD0	47	−50.8	110	59	7C50	943		174	F9	6ACE	5425	−9.6	238	99	29AA	22101	
47	38	7FCB	52	−50	111	58	7C24	987		175	F8	6A4F	5552	−9.4	239	98	27A7	22616	
48	28	7FC9	54		112	48	7BF5	1034	−24	176	E8	69CE	5681		240	88	259B	23143	+3
49	29	7FC6	57		113	49	7BC5	1082		177	E9	694A	5813	−9	241	89	237D	23682	
50	2B	7FC4	59		114	4B	7B92	1133		178	EB	68C2	5949		242	8B	2155	24234	
51	2A	7FC1	62		115	4A	7B5C	1187		179	EA	6838	6087		243	8A	1F21	24798	
52	2E	7FBE	65	−48	116	4E	7B24	1243		180	EE	67AA	6229		244	8E	1CDF	25376	
53	2F	7FBB	68		117	4F	7AEA	1301	−22	181	EF	6719	6374		245	8F	1A90	25967	+4
54	2D	7FB7	72		118	4D	7AAC	1363		182	ED	6684	6523	−8	246	8D	1833	26572	
55	2C	7FB4	75		119	4C	7A6C	1427	−21.2	183	EC	65EC	6675		247	8C	15C8	27191	
56	24	7FB1	78		120	44	7A29	1494	−20.8	184	E4	6551	6830		248	84	134F	27824	4.6
57	25	7FAD	82	−46	121	45	79E2	1565	−20.4	185	E5	64B2	6989		249	85	10C7	28472	4.8
58	27	7FA9	86		122	47	7999	1638	−20	186	E7	640F	7152		250	87	0E30	29135	+5
59	26	7FA5	90		123	46	7973	1676	−19.8	187	E6	6369	7318	−7	251	86	0B8A	29813	+5.2
60	22	7FA1	94		124	42	794B	1716	−19.6	188	E2	62BE	7489		252	82	08D3	30508	+5.4
61	23	7F9C	99		125	43	7923	1756	−19.4	189	E3	6210	7663		253	83	060C	31219	+5.6
62	21	7F98	103	−44	126	41	78FB	1796		190	E1	615D	7842		254	81	0335	31946	+5.8
63	20	7F93	108		127	40	78D1	1838	−19	191	E0	60A6	8025		255	80	0	32767	+6

7.4.2.9. PB GAIN FILTER

The 15-bit linear gain signal after the GAIN LOG--->LIN conversion is in 265-step discontinuous value form, and therefore produces step noise at each changes of level. To eliminate this noise, it is smoothed in a digital LPF.

In order to make step noise inaudible, the clock frequency should be selected at integer multiples of 44.1kHz (including 1) and the ripple caused by step level changes should be attenuated sufficiently. If for this purpose a clock frequency of 44.1kHz is selected and the time constant is selected around 100 msec for a linear IIR type LPF, the circuit will become very large. To avoid the use of extensive circuits, a 5-segment approximately linear time-constant doubling circuit is used here. Refer to Figure 7-25A.

The output side counter is moved towards the input in a direction determined by the difference between the input and the output of the PB GAIN FILTER.

The difference between the input and the output is calculated by the ADDER (IC-E10, D10, C10, B10), is level is detected by the EX-OR (IC-E8) and OR (IC-E7) gates and the 4 output of the IC-E10 becomes the same polarity.

The slope control counter is self-running at a rate determined by this level and outputs the carry. This carry, together with the previous output polarity, drives the output counter (IC-E11, D11, C11, B11) gradually towards the input. When the input and the output are equal, the output of the ADDER becomes all "1"'s. The comparator gates (IC-D8, C7, E7) detect it, the counting and carry output of the slope control counter is stopped, and the output counter is stopped. In his way, each time the fader is moved, the output counter follows the movement automatically. the output of the output counter is stored in FF (IC-A10, A11) and output to the X-BUS by control signal GN-OE from the SC-B board. Refer to Figure 7-25B.

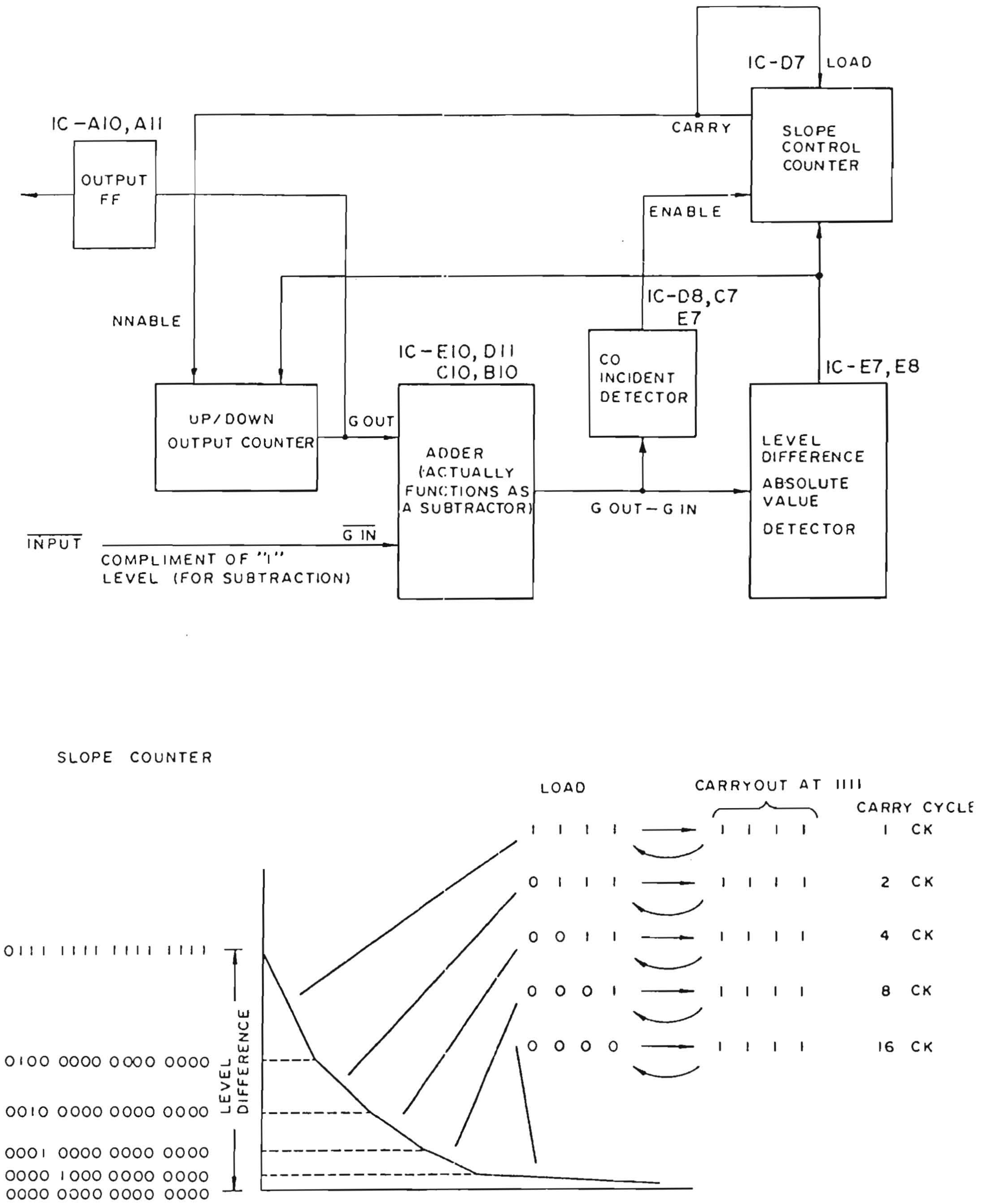


Figure 7-25A PB Gain Filter Circuit block diagram and slope counter operation

7.5 SC-B Board

7.5.1. General

The SC-B board receives 2 channel main digital data (16 bits x 2) from the I/O board, sharing this data with the SC-A board, processes in the EDITOR mode and sends the processed data back to the I/O board. In the STRAIGHT mode and SEARCH mode, signals are processed as shown in Figure 7-26.

In the EDIT mode, signals are processed under the control signals from the EDIT board.

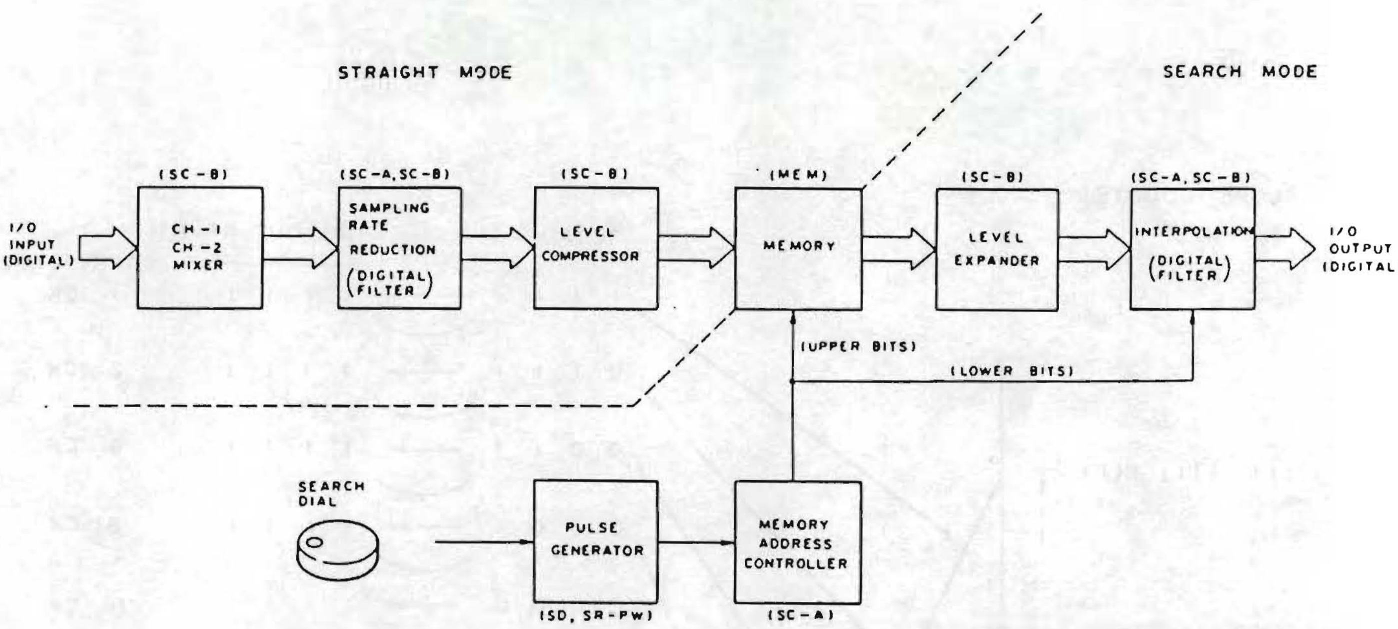


Figure 7-26 Straight mode/search mode

7.5.2. Configuration

The SC-B board consists of the (L + R) ADDER (1) for selecting the monitor channel in the SEARCH mode; SEARCH SELECTOR (2); W-FILTER RAM (3) required by the LPF (Low Pass Filter) the sampling rate; MULTIPLIER(4) for performing various operations Read/Write filter, FADER GAIN and CROSS Fade; LEVEL CLIPPER (5) for detecting and clipping MPY overflow; CROSS FADER FF (6) for storing the timeshared MPY output and outputting to the 32-bit Data Bus; COMPRESSOR (7) for compressing the continuous 4-sample data (64-bit) obtained at half the sampling rate to 32-bit data; (4-1) SELECTOR (8) and EXPANDER (9) for returning the compressed data written to the MEM board to original 16-bit linear data; a GN, B GN (10) for storing a GN and B GN values; MODE DECODER (11) for selecting modes; TIMING COUNTER (12) for creating time slots within individual words and creating 8-word cyclic timing; BUS OUT ROM (13) for controlling the output of each DATA BUS; FF CLOCK ROM (14) for outputtng the MEMORY ADDRESS, and for clocking the flip-flop which latches the main digital data; FILTER CTL ROM (15) for timing respective digital filters; CROSS FADER ROM (16) for timing the crossfading process; CROSS FADE CH SELECT (17) for setting cross-fading conditions; and PB FF, REC FF, SEARCH FF (18) for inputting data from the I/O to the MPY. The block diagram is shown in Figure 7-27.

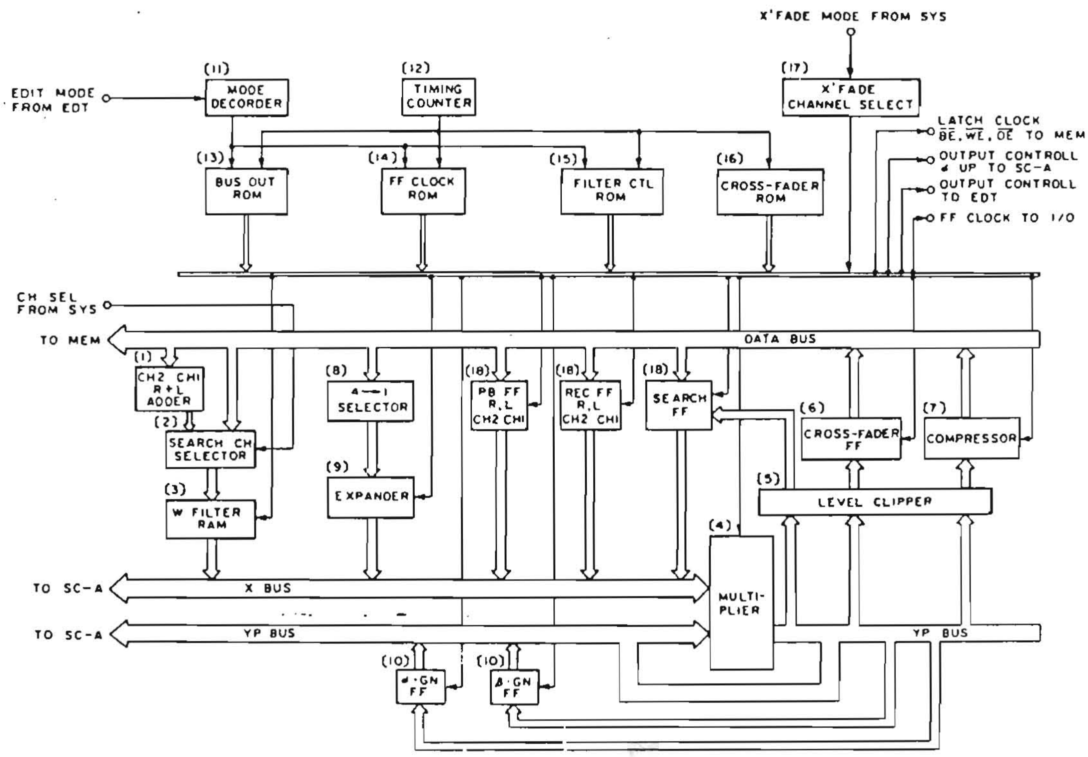


Figure 7-27 Block Diagram (SC-B)

7.5.3. Description of Circuit

7.5.3.1. (L + R) ADDER

In this adder, the right and left audio signals received from the processor via the I/O board and the RD BUS are mixed and converted into mono audio signals.

16 bits each from the right and left signals are added by IC-C11, I11, J11, K11 and K7, and of the resulting 17 bits, the upper 16 bits are used to calculate $\frac{L + R}{2}$.

7.5.3.2. SEARCH CH SELECTOR (IC-H9, H10, I9, I10, J9, J10, K9 and K10)

This **SELECTOR** selects one out of left (L) sound, right (R) sound mix ($\frac{L + R}{2}$) sound, or MUTE (16 0's) available for writing in mono to the MEM board. It is switched by 2-bit signals (SRC CH1, SRC CH2) from the SYS board as follows.

SELECTED OUTPUT / Input	MUTE	CH2 (R)	CH1 (L)	MIX
SRC CH1	0	0	1	1
SRC CH2	0	1	0	1

The monitor LED is turned on by 1 and turned-off by 0.

7.5.3.3. W FILTER RAM (WRITE FILTER RAM) (IC-A9, B9, C9, D9, D10)

This RAM is used as a substitute for a 16 bit X 16 word shift-register to make a FIR type DIGITAL LPF for reducing the sampling rate when writng audio search data to RAM to 22.05kHz. It reads 16 words to make one filtered data, and then in order to write a new word, shifts one address over 16 addresses, which advances to tally addresses.

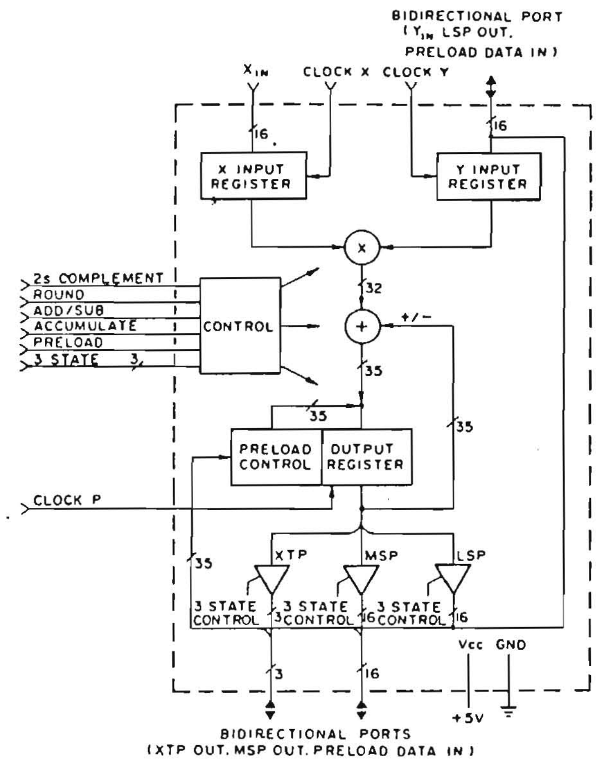
7.5.3.4. MULTIPLIER-ACCUMULATOR (TDC-1010J) (IC-H2)

This circuit outputs the cumulative sum of the products of the 16-bit X BUS input and the 16-bit Y BUS (YP BUS) input to the P BUS (YP BUS) as a 35-bit word.

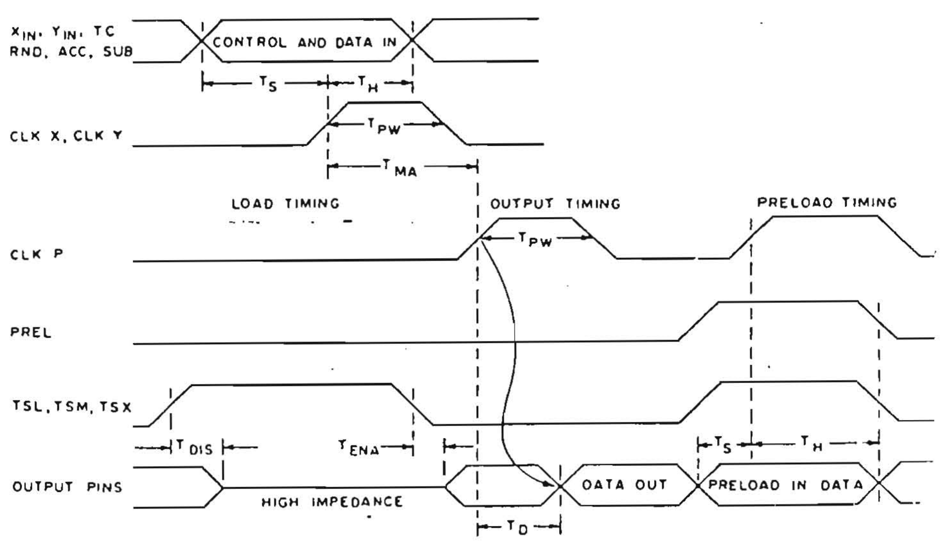
Since the P BUS and the Y BUS partly overlap, input and output are time-shared.

The following calculations are performed here:

MPY
MULTIPLIER-ACCUMULATOR
PARALLEL 16-BIT



TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

absolute maximum ratings over operating temperature range

Supply voltage	−0.5 to 7.0 V
Input voltage	0 to 5.5 V
Output voltage	0 to 5.5 V
Operating temperature range TDC1010J ($T_{ambient}$)	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature (10 seconds)	300°C
Junction temperature	175°C

recommended operating conditions

	TDC1010J			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5.0	5.25	V
High-level output current, I_{OH}			−0.4	mA
Low-level output current, I_{OL}			4.0	mA
Clock pulse width, t_{PW} (measured at 1.5 V level)	25			nsec
Input register setup time, t_S (see Fig. 9)	25			nsec
Input register hold time, t_H (see Fig. 9)	0			nsec
Operating temperature ($T_{ambient}$ for TDC1010J)	0		70	°C

electrical characteristics over recommended temperature range (except as otherwise noted)

PARAMETER	TEST CONDITIONS	TDC1010J			UNIT
		MIN	NOM	MAX	
V_{IH} High-level input voltage		2.0			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	V_{CC} = MIN, I_{OH} = −0.4 mA	2.4	2.7		V
V_{OL} Low-level output voltage	V_{CC} = MIN, I_{OL} = 4.0 mA		0.3	0.5	V
I_{IH} High-level input current	V_{CC} = MAX V_{IH} = 2.4			75	µA
I_{IL} Low-level input current	V_{CC} = MAX V_{IL} = 0.4			−0.4	mA
I_{IH} Clocks* high level input current	V_{CC} = MAX V_{IL} = 2.4			75	µA
I_{IL} Clocks* low level input current	V_{CC} = MAX, V_{IL} = 0.4			−1.0	mA
I_{CC} Supply current	V_{CC} = MAX.		680	900	mA

* NOTE Clock P is two equivalent clock loads.

switching characteristics across V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TYP**	MAX	UNIT
		TDC1010J	
Multiply-accumulate time, t_{MA} input register clock to output register clock	115	155	nsec
Output delay t_D	25	35	nsec
Three state output delay Output enable, t_{ENA}	25	35	nsec
Output disable, t_{DIS}	25	35	nsec

OPERATION DESCRIPTION

Data Input (X_0 to X_{15} and Y_0 to Y_{15})

X_0 and Y_0 are least significant bits and X_{15} and Y_{15} are most significant bits. Data inputs are loaded into the X register and Y register at the rising edge of CLK X and CLK Y, respectively. Note: the LSP (P_0 to P_{15}) outputs are time-shared with the Y data inputs (Y_0 to Y_{15}).

Data Output (P_0 to P_{34})

P_0 is the least significant bit and P_{34} is the most significant bit. The product is divided into Least Significant Product (LSP: P_0 to P_{15}), Most Significant Product (MSP: P_{16} to P_{31}) and Extended Product (XTP: P_{32} to P_{34}). The product generated is loaded into the outputs registers at the rising edge of CLK P.

Pre-Load Data (PD_0 to PD_{34})

Data applied externally to output pins, to initialize output register to a given value at the rising edge of CLK P.
PD_0 to PD_{34} are provided to output pins P_0 to P_{34} respectively, where PD_0 is least significant bit and PD_{34} is the most significant bit.

Two's Complement Control (TC)

When TC is high, the inputs are 16-bit two's complement numbers. When TC is low the inputs are 16-bit unsigned magnitude numbers. The TC signal is loaded into the TC register at the rising edge of either CLK X or CLK Y. The TC signal must be valid over the same period that the input data is valid.

Round Control (RND)

When RND is high, a "1" is added to the most significant bit of the LSP in the multiplier array (P_{15}) to round up the product in MSP and XTP rather than truncate it.

The RND signal is loaded into the RND register at the rising edge of either CLK X or CLK Y. The RND signal must be valid over the same period that the input data is valid.

Accumulation Control (ACC)

When ACC is high, the contents of the output registers are added to the next product generated and their sum is stored back into the output registers at the rising edge of the next CLK P.

When ACC is low, multiplication without accumulation is performed and the next product generated will be stored into the output registers directly.

The ACC signal is loaded into the ACC register at the rising edge of either CLK X or CLK Y. The ACC signal must be valid over the same period that the input data is valid.

Subtraction Control (SUB)

When ACC and SUB are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLK P.

When ACC is high and SUB is low, addition is performed instead of subtraction.

The SUB signal is loaded into the SUB register at the rising edge of either CLK X or CLK Y. The SUB signal must be valid over the same period that the input data is valid.

Pre-Load Control (PREL)

All output buffers are at high impedance (output disabled) when PREL is high. When TSL, TSM, or TSX are also high, the initial contents of their corresponding output register can be preset to the Pre-Load Data (PD_0 to PD_{34}) applied to the output pins at the rising edge of CLK P. If TSL, TSM, or TSX is low while PREL is high, the contents of the respective output register remain unchanged while the output drivers remain at high impedance.

Three State Least, Most and Extended Control (TSL, TSM, TSX)

The LSP, MSP, or XTP output buffers are at high impedance (output disabled) when TSL, TSM, or TSX is high, respectively. These are direct, non-registered control signals. The output drivers are enabled when TSL, TSM, or TSX are low, and PREL is low.

PRE-LOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	O	O	O
0	0	0	1	O	O	Hi Z
0	0	1	0	O	Hi Z	O
0	0	1	1	O	Hi Z	Hi Z
0	1	0	0	Hi Z	O	O
0	1	0	1	Hi Z	O	Hi Z
0	1	1	0	Hi Z	Hi Z	O
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

Note:

Hi Z = Output buffers at high impedance (output disabled).
O = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance or output disabled. Pre-Load Data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

- WRITE-FILTER calculation
  For limiting the band width, FIR operations are performed

$$[\text{W-FIL-OUT}] = \sum_{i=1}^{16} C_{wi} \quad X_{wi}$$

Y input W-FIL coeff out (SC-A)	X input W-FIL-RAM Read-out

- READ-FILTER calculation
  SEARCH OUT VARIABLE FIR operation

$$[\text{R-FIL-OUT}] = \sum_{i=1}^{8} C_{Ri} \quad X_{Ri}$$

Y input R-FIL coeff out (SC-A)	X input EXPANDER out

- FADER GAIN calculation
  Although the cross-fader gain on the Recorder is 1, the cross-fader gain on the Player can be varied with the GAIN OFFSET FADER.
  [PB CROSS-FADER coefficient α GN] $= \alpha \times$ GN
  [PB CROSS-FADER coefficient β GN] $= \beta \times$ GN

Y input from cross fade coefficient α,β selector (SC-A)	X input From GAIN OFFSET PB GAIN FILTER (SC-A)

- CROSS-FADE operation
  [CROSS FADE OUT L] $=(\alpha$ or α GN$) \times L\alpha + (\beta$ or β GN$) \times L\beta$
  [CROSS FADE OUT R] $=(\alpha$ or α GN$) \times R\alpha + (\beta$ or β GN$) \times R\beta$

a, B, a GN, and B GN are Y inputs.
When the multiplicants, Lx and Rx are on the Player (including SEARCH for Player sound), a GN and B GN are used, and for Recorder sound, a and B are used.

With MUTE, either can be used.
a and B are sent from the a, B SELECTOR, (SC-A), and a GN and B GN are sent from the a GN FF and B GN FF.

La, LB, Ra and RB are X inputs.
Any two outputs from (PB FL,R), (REC FFL, R), (SEARCH FF), and EXPANDER (MUTE) are selected as a and B and are output to the X BUS. They are output once each for L and R. For SEARCH and MUTE, the same one is output twice for L and R.

7.5.3.5. LEVEL CLIPPER

The results of the calculations in the MULTIPLIER-ACCUMULATOR (MPY) may overflow for some input signals. This CLIPPER detects overflow and clips the data to the maximum levels in positive and negative. The MSB of the used 16 bits of the MPY output is compared with the bit immediately above it by the EX-OR (IC-G8), and if they are different the data is treated as overflow and the maximum level is output by the SELECTOR LS157 (IC-F8, F9, E8, E9) and the INVERTER (IC-G10).

Positive maximum level: 0111111111111111
Negative maximum level: 1000000000000000

7.5.3.6. CROSS-FADER FF, BUFFER

(LEVEL CLIPPER OUTPUT) of the results of cross-fader calculation on the MPY output, the 16 bits L-CH data are stored in the FF, the 16 bits R-CH data are stored in the LATCH, then both the L-CH and R-CH data are output to the RD BUS simultaneously.

7.5.3.7 COMPRESSOR

The COMPRESSOR compresses the 64 bit output resulting from the WRITE-FILTER calculation in the MPY (LEVEL CLIPPER OUTPUT) made up of 4 samples of 16 bits (successive samples of 4 at 22.05kHz are taken in every other position from 44.1kHz samples) into a total of 32 bits consisting of the 7-bit x 4 word mantissa and 4-bit exponent, (common to all 4 samples). See Figure7-28.

In STRAIGHT PB/REC modes, the results of the W-FILTER calculation passing through the LEVEL CLIPPER are loaded in series in the four 16-bit shift registers IC-(C6, D6, F5, A1), (C5, E6, G5, B1), (C4, E5, G4, C1), and (C3, E4, D2, D1), at a rate of once every two words. Upon loading the four shift registers with 64 bits (once every 8 words) the four shift registers shift to the upper bits simultaneously. If the IC-D4 (LS85) detects any difference in state between MSB and 2SB in any of the four shift registers, (that is, the state immediately before overflow), or if the COUNTER (IC-C8) outputs a cassy after shifting 9 bits, the shifting is stopped. At this time, each upper 7 bits of the data remaining in the four shift registers is output as the mantissa to the RD BUS, and the remaining 4 bits in the counter are output to the RD BUS as the exponent part. These 32 bits are sent to the MEM board and are written in the SEARCH RAM.

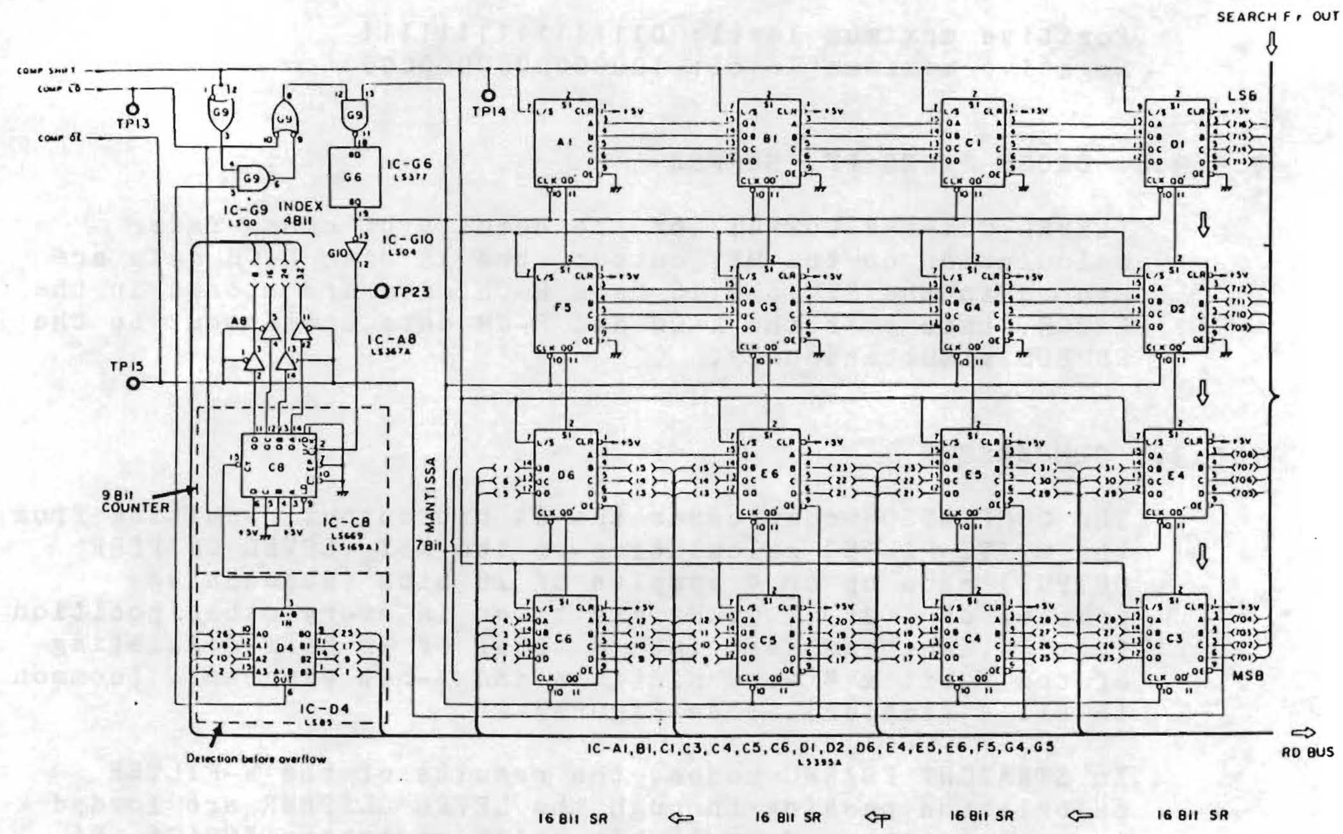


Figure 7-28 Compressor

7.5.3.8. 4-->1 SELECTOR

In the SEARCH mode, the output of the SEARCH RAM sent from the MEM board is in compressed form. This SELECTOR selects one 7-bit word from the 28-bit mantissa (4 words x 7 bit) in the compressed output from the address 2 bits below the SEARCH RAM address, and sends it to the EXPANDER. When MUTE output signal is input in any mode, this SELECTOR outputs all "0's"

7.5.3.9. EXPANDER

In the EXPANDER, in the SEARCH RAM output signals, an 11-bit word consisting of 7 mantissa bits that have passed through the 4 -->1 SELECTOR, and 4 exponent bits that have passed through the IC-C10-2, is brought back to 16-bit linear form in the ROM (IC-A10, B10). The IC-CIO-2 outputs "1's" for all 4 bits when it receives a MUTE output signal. This is combined with the all 0's 7-bit output from the 4 -->1 SELECTOR, and the resulting 11110000000 is given to the ROM. At this time, the ROM outputs all 0's 16-bit MUTE data to the X-BUS.

7.5.3.10. a GN FF, B GN FF

These FFs store a GN and B GN obtained from fader gain calculation among the MPY calculation results and outputs them to the X BUS as required during cross-fade calculation.

a GN FF	IC-F10, E10
B GN FF	IC-F11, E11

7.5.3.11.MODE DECODER

This decodes the 4-bit mode-select signal, MS-3 through MS-0 sent from the EDT board and outputs WRITE MODE (STRAIGHT MODE), RAM CLR MODE and RAM CHECK MODE (IC-K1, K2, 11).

It also displays the mode with LEDs and store them (one word) (K2) to supply them to addresses of the ROM which output mode control signals (G10, K5). The mode-select LEDs light in the following manner:

MODE SELECT LEDs (Lights for a 1)

MODE	MS-3	MS-2	MS-1	MS-0
RAM CLEAR	0	0	0	1
STRAIGHT	0	0	1	1
SEARCH	0	1	1	1
MUTE OUTPUT	1	0	0	0
REC RAM WRITE	1	0	1	1
PB RAM WRITE	1	0	1	0
DELAY MEASURE	1	0	0	1
EDIT	1	1	X	X

7.5.3.12. TIMING COUNTER

This counter is driven by $\overline{\text{5.6M}}$ and $\overline{\text{WD SYNC}}$ creates time slots within single words, and the timing for 8-word periods.

intra-word counter IC-13, J2
8 word counter IC-J1, I4

7.5.3.13. BUSS OUT ROM IC-K4 74S471

7.5.3.14. FF CLOCK ROM IC-14 74S472

7.5.3.15. FILTER CTL ROM IC-16 74S472

7.5.3.16. CROSS-FADER ROM IC-16 74S288

These decode the TIMING COUNTER outputs, and make control signals internal to the SC-A, I/O and EDT boards.

The control ranges of each of these ROMs are as follows:

7.5.3.13. BUS OUT ROM

Control of output to RD-BUS O_2 O_1 O_1

When O_2 O_1 O_0 are 0 through 7

000 0 - Nothing (High-Impedance)
001 1 - INPUT BUFFER (I/O BD)
010 2 - RAM (MEM BD)
011 3 - CHECK DATA OUT BUFFER (MEM BD)
100 4 - COMPRESSOR (SC-B)
101 5 - CROSS FADER FF BUFFER (SC-B)
110 6 - Nothing
111 7 - Nothing

Control of output to X-BUS O_4 O_3

Only in about the first 3/4 of the word slot
When O_4 O_3 are 0 through 3

00 0 - Nothing
01 1 - W-FILTER RAM (SC-B)
10 2 - EXPANDER (SC-B)
11 3 - Nothing

Control of output to Y-BUS (YP-BUS) O_6 O_5

Only in about the first 3/4 of the word slot
When O_6 O_5 are 0 through 3

00 0 - Nothing
01 1 - W-FILTER COEFFICIENT (SC-A)
10 2 - R-FILTER COEFFICIENT (SC-A)
11 3 - MPY (SC-B)

MEM BD R/$\overline{W}$ (READ/$\overline{WRITE}$) O_7

7.5.3.14. FF CLOCK ROM

Control of output to RA-BUS $0_2\ 0_1\ 0_0$

(RA-BUS = MEM BD ADDRESS BUS)

When $0_2\ 0_1\ 0_0$ are 0 - 7

000 0 - Nothing
001 1 - D/A RAM ADDRESS (EDT)
010 2 - SYNC RAM ADDRESS EDT)
011 3 - PB RAM ADDRESS (EDT)
100 4 - REC RAM ADDRESS (EDT)
101 5 - SEARCH RAM ADDRESS (SC-A)
110 6 - Nothing
111 7 - Nothing

- o SEARCH FF CK (SC-B) 0_3
- o PB FF CK (SC-B) 0_4
- o REC FF CK (SC-B) 0_5
- o D/A FF CK (I/O) 0_6
- o ECN FF CK (I/O) 0_7

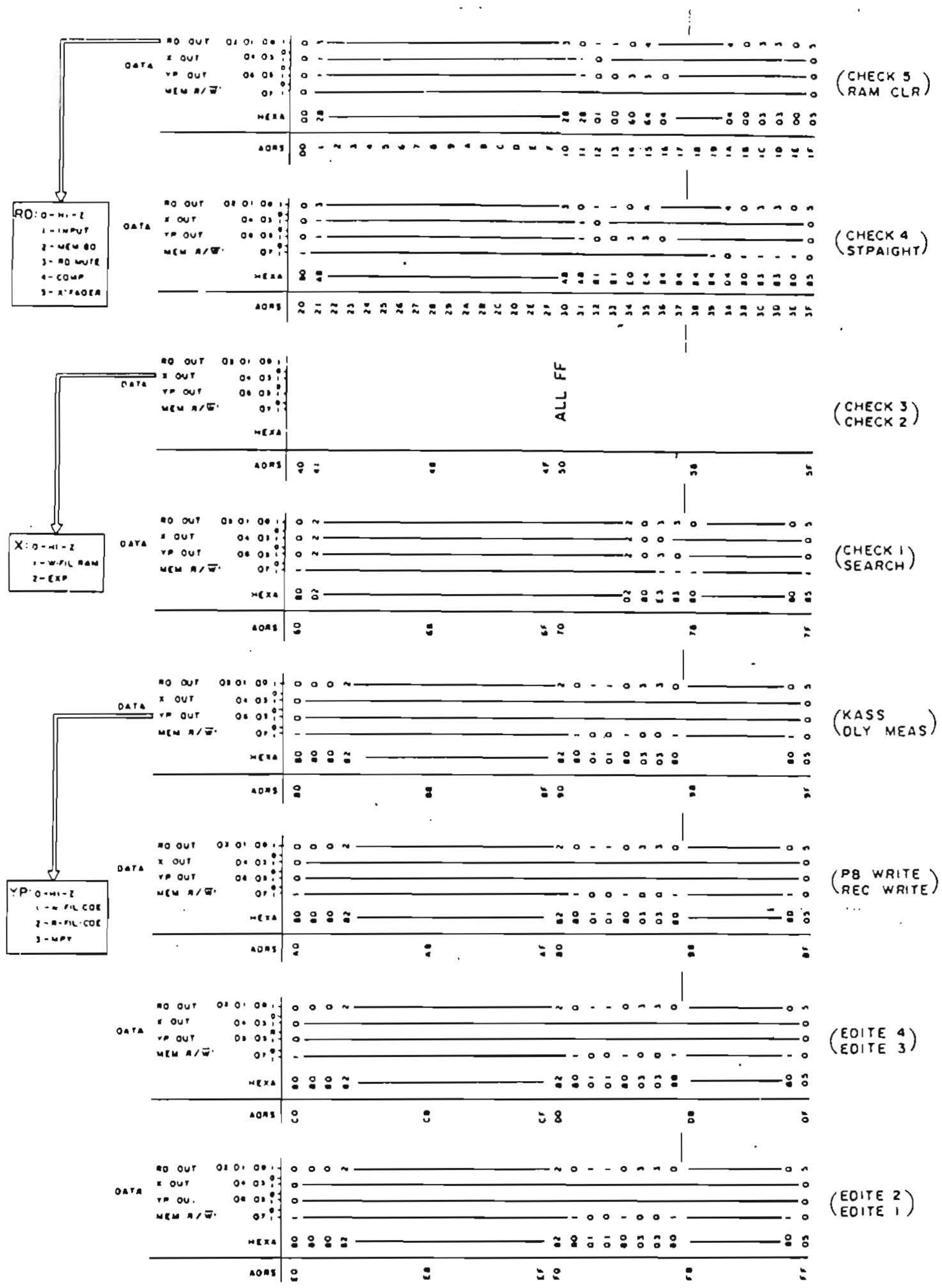
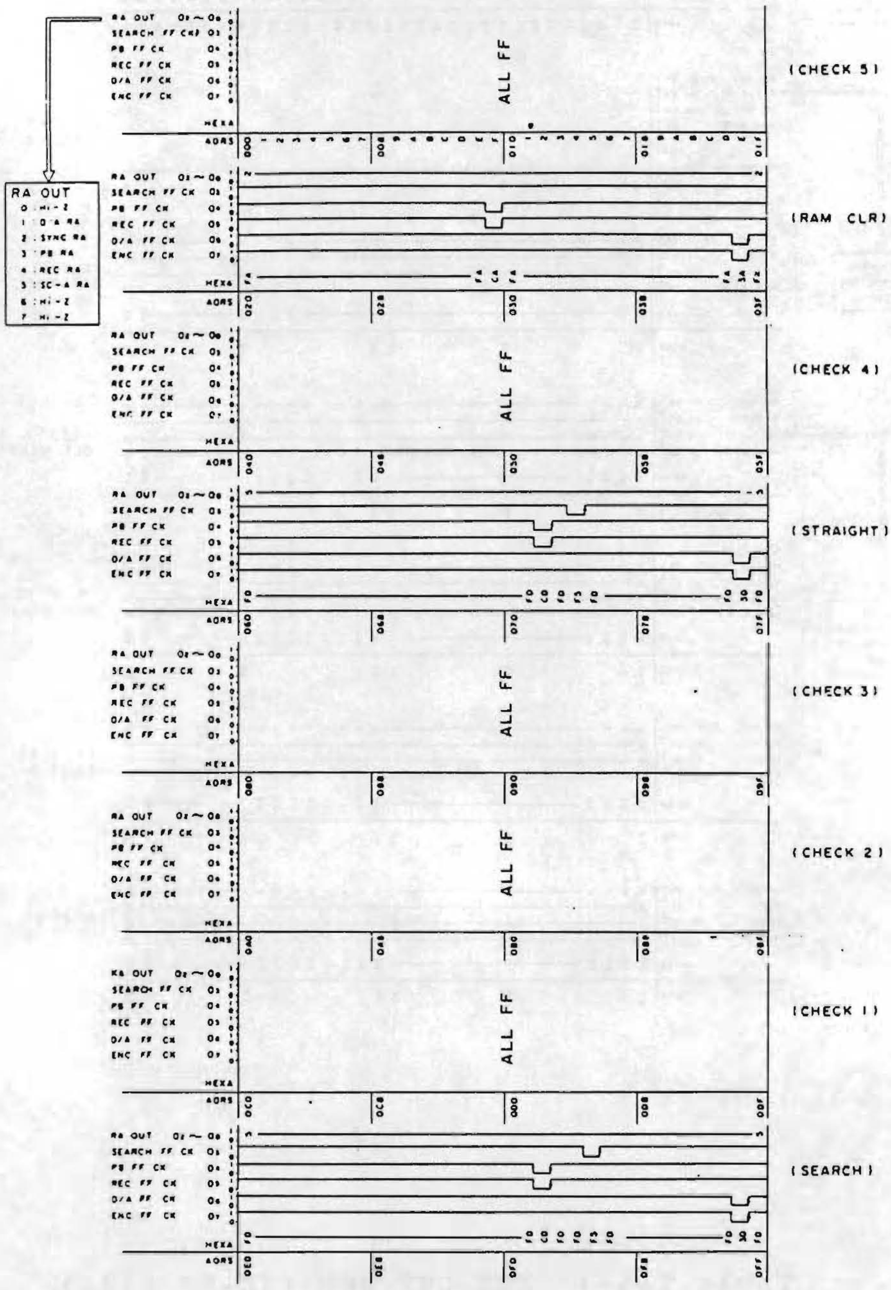


Table 7-5-1 BUS OUT ROM (IC-K4 S471)

FF CLOCK ROM (1/2) (ADDRESS 000-0FF)



FF CLOCK ROM (2/2) (ADDRESS 100-1FF)

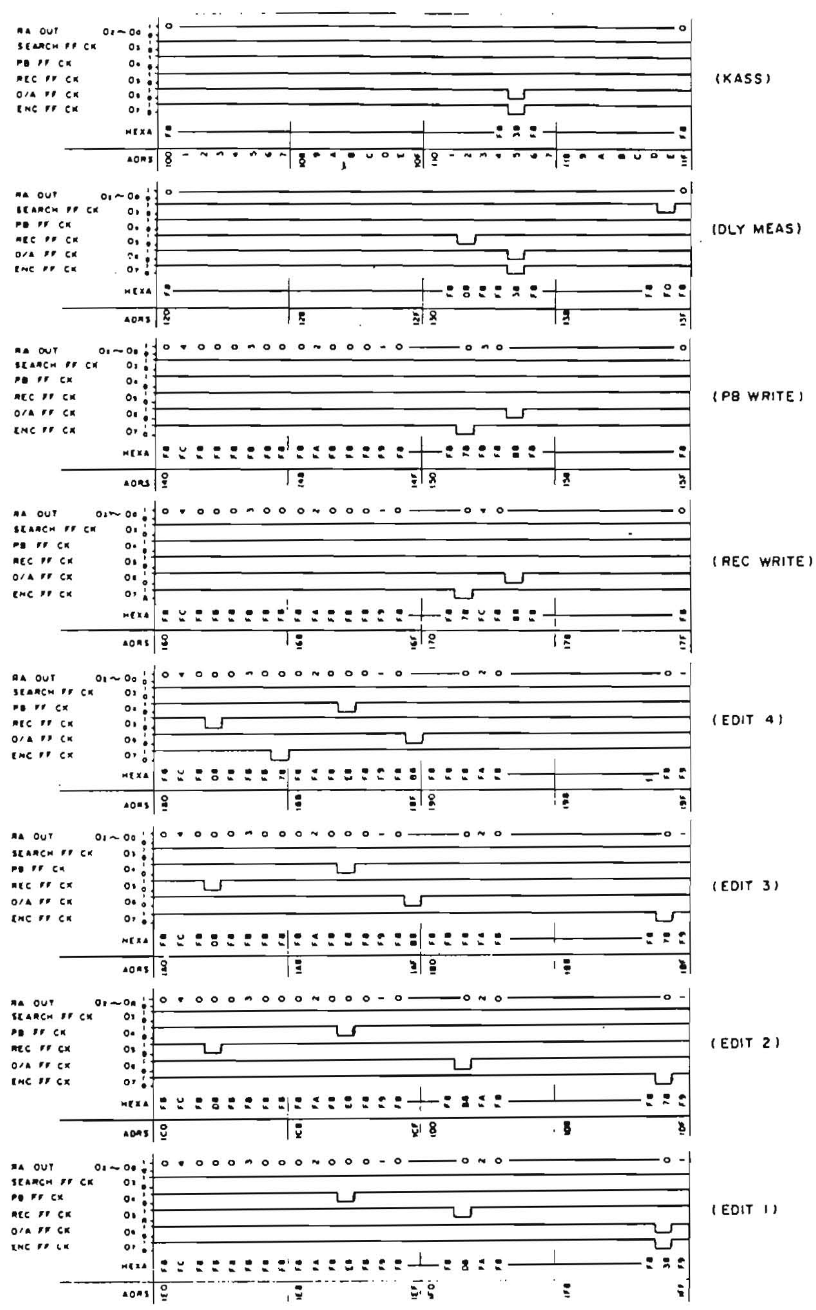
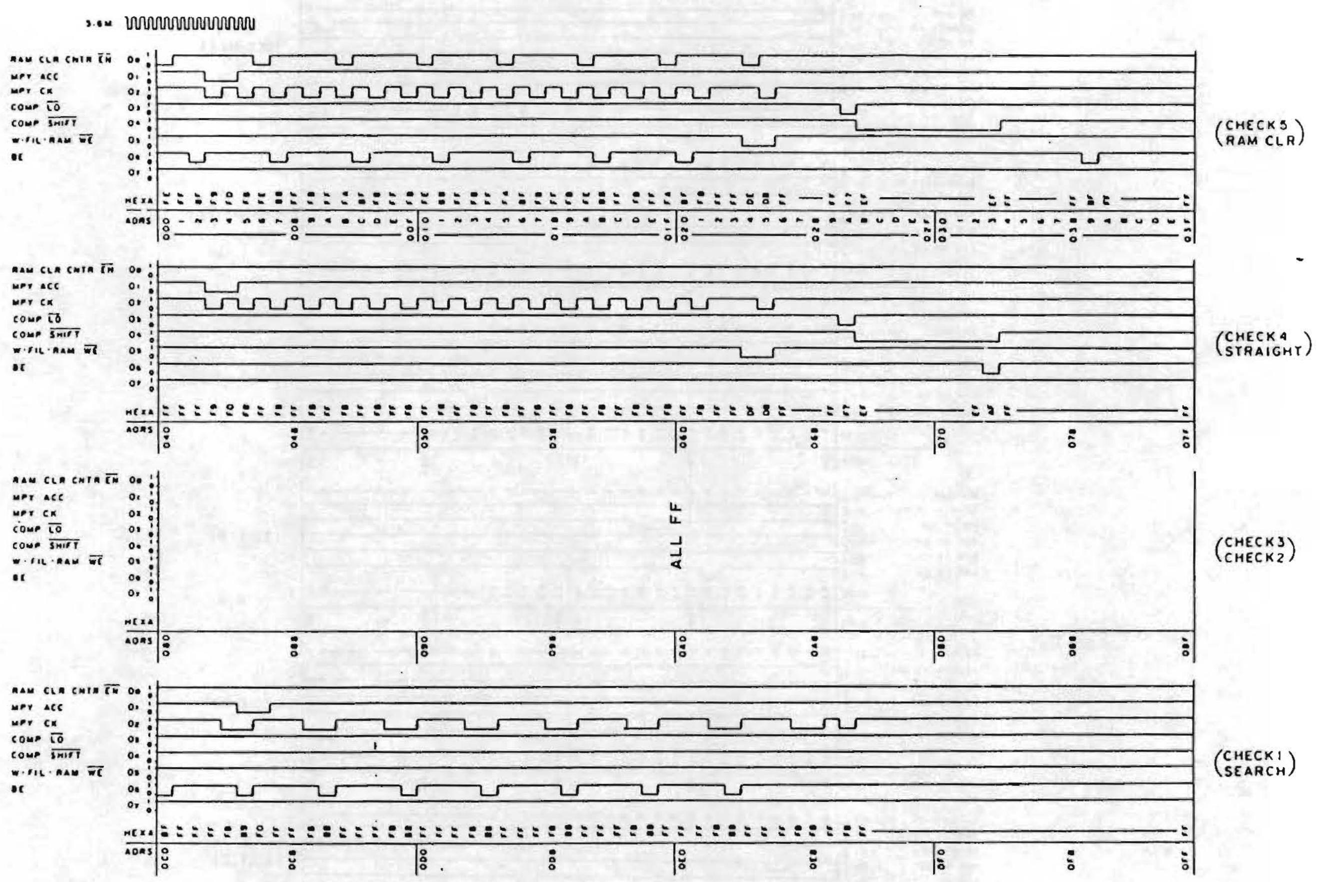


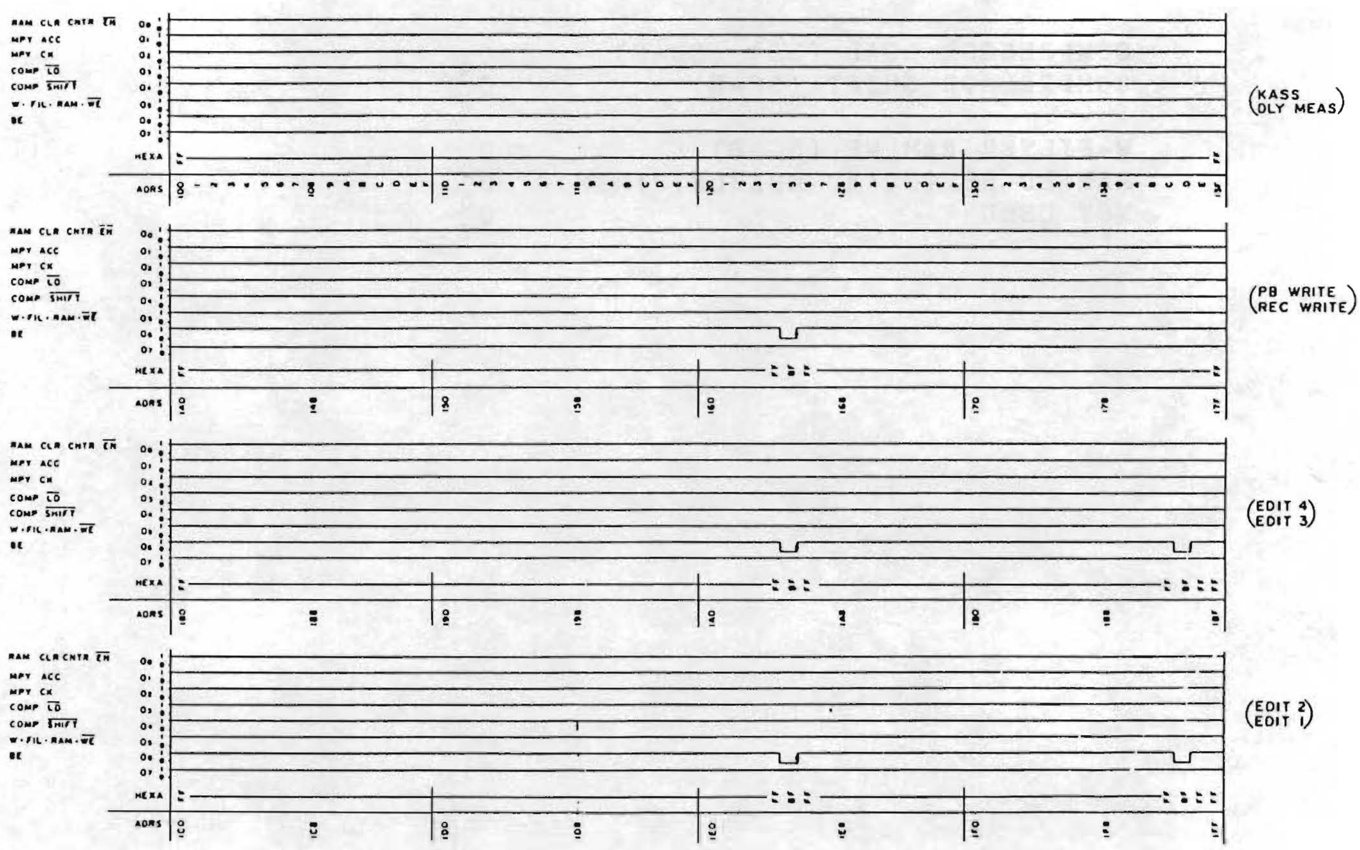
Table 7-5-2 FILTER CTL ROM (1/2) (ADDRESS 000-0FF)
IC-16 S472



7.5.3.15. FILTER CTL ROM

RAM CLEAR COUNTER ENABLE (EDT)	O_0
MPY-ACC ACC (SC-B)	O_1
MPY-ACC CK (SC-B)	O_2
Only in about the first 3/4 of the word slot	
COMPRESSOR $\overline{\text{LOAD (LD)}}$ (SC-B)	O_3
COMPRESSOR SHIFT (SC-B)	O_4
W-FILTER RAM $\overline{\text{WE}}$ (SC-B)	O_5
MEM BD BE (BOARD ENABLE) (MEM)	O_6
NOT USED	O_7

FILTER CTL ROM (2/2) (ADDRESS 100-1FF)



7.5.3.16. CROSS FADER ROM

Only in about the last 1/4 of the word slot

NOT USED

a G_N 0_0

CROSS FADER FF CK $\overline{G_N \text{ FF CK}}$ 0_1

CROSS FADER FDF CK 0_2

Control of output to X/BUX, Y-BUS 0_5 0_4 0_3

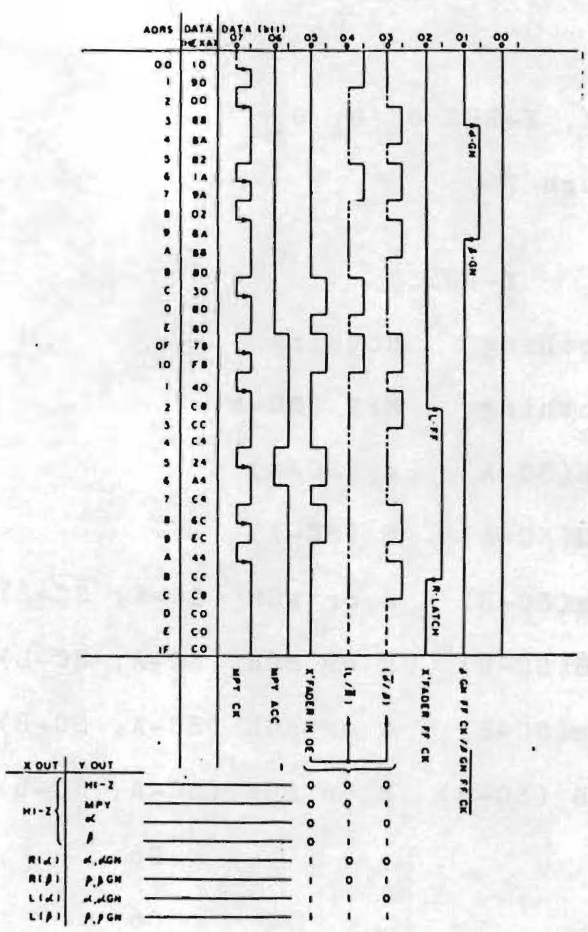
when 0_5 0_4 0_3 are 0 through 7

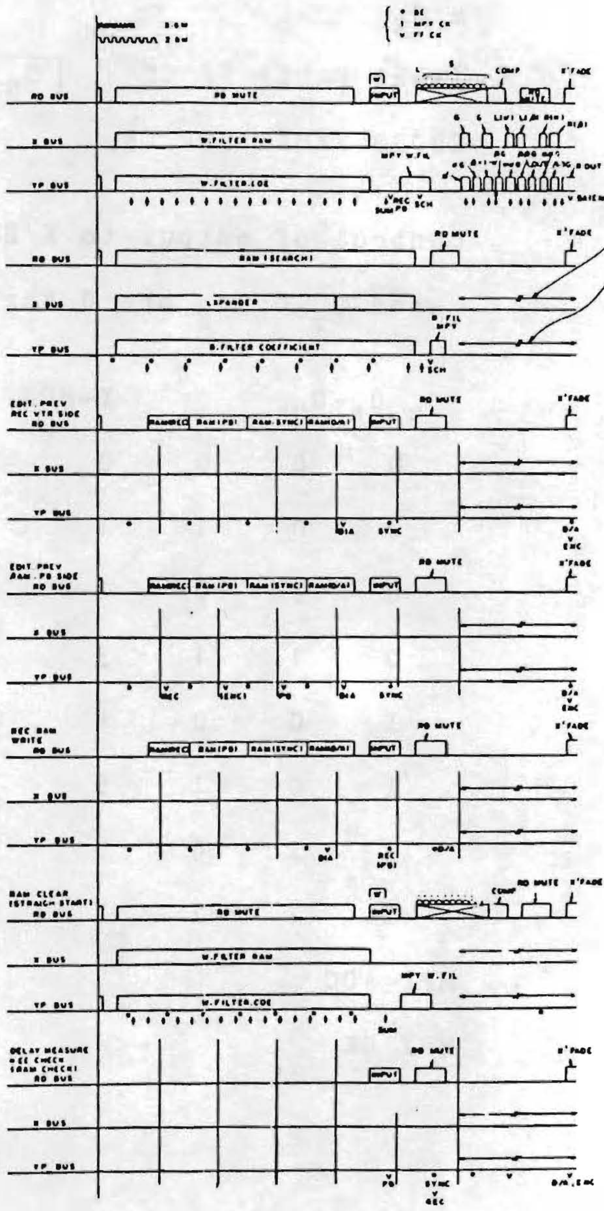
0_5	0_4	0_3		X-BUS	Y-BUS
0	0	0	0	Nothing	Nothing
0	0	1	1	Nothing	MPY (SC-B)
0	1	0	2	GN(SC-A)	a (SC-A)
0	1	1	3	GN(SC-A)	B (SC-A)
1	0	0	4	Ra(SC-B)	a or aGN (SC-A, SC-B)
1	0	1	5	RB(SC-B)	B or BGN (SC-A, SC-B)
1	1	0	6	La(SC-B)	a or aGN (SC-A, SC-B)
1	1	1	7	LB (SC-B)	B or BGN (SC-A, SC-B)

MPY ACC 06

MPY CK 06

Table 7-5-3 CROSS-FADER ROM IC-J5 S288





7.5.3.17. X'FADER CHANNEL SELECT

The operation of the X'FADE CHANNEL LEDs is as follows:

X'FADE CH LED (Light for a 1)

CH SELECT	MSB	2SB	LSB
PB CH	1	1	1
REC CH	1	1	0
PB S CH	1	0	1
REC S CH	1	0	0
MUTE	0	X	X

7.5.3.18. PB/PRE/SEARCH FLIP FLOP

Refer to circuit diagram.

7.6 I/O BOARD, CON BOARD

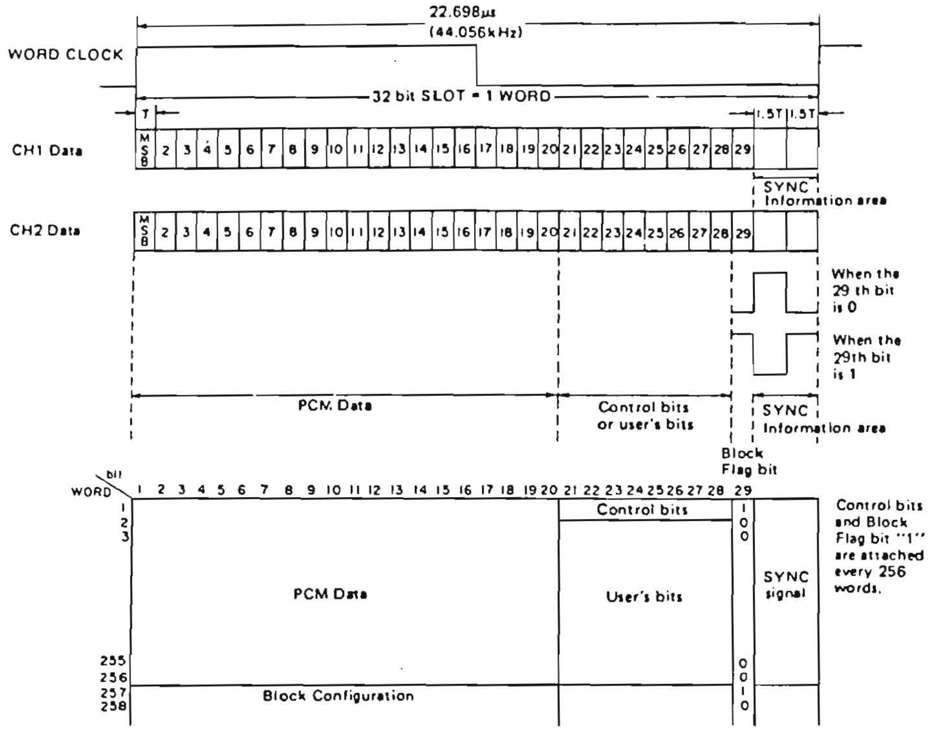
7.6.1. Outline

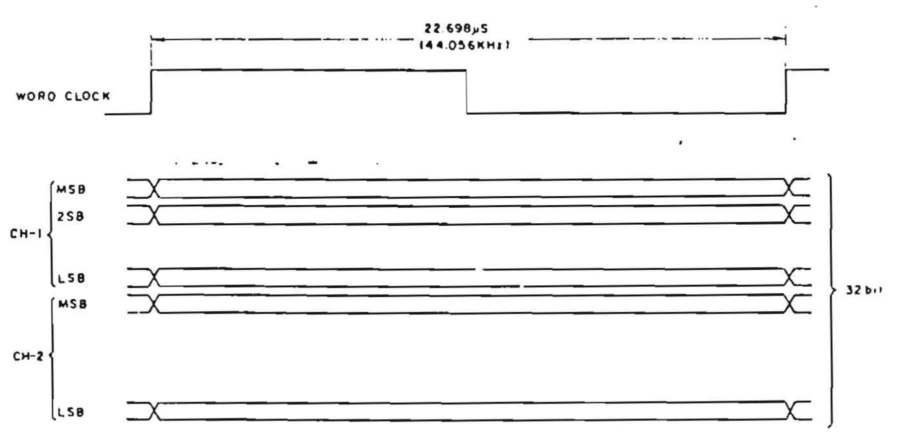
The **DAE-1100** is provided with a digital signal interface circuit that can accommodate both parallel and serial formats in order to be able to edit with either of the two PCM processors; the **PCM-1600** with parallel I/O format (Figure 7-29), and the **PCM-100**, **PCM-1610** with serial I/O format (Figure 7-30).

For processing within the **DAE-1100** for 16-bit/ch parallel format on input block, PMC data is extracted from either parallel or serial inputs, converted into internal format, and put on the data bus. On output block, PCM data from the data bus is converted into both parallel and serial I/O formats for output.

Data and Sync are selectively switched between serial and parallel modes by the selection switch on the SC-A board.

The CON board comprises static protection circuits for digital signals and VTR remote...for protecting the internal ICs from the static charges directly discharged through the external connectors.





PALALLEL I/O FORMAT

Parallel I/O Format

Figure 7-29 Serial I/O Format

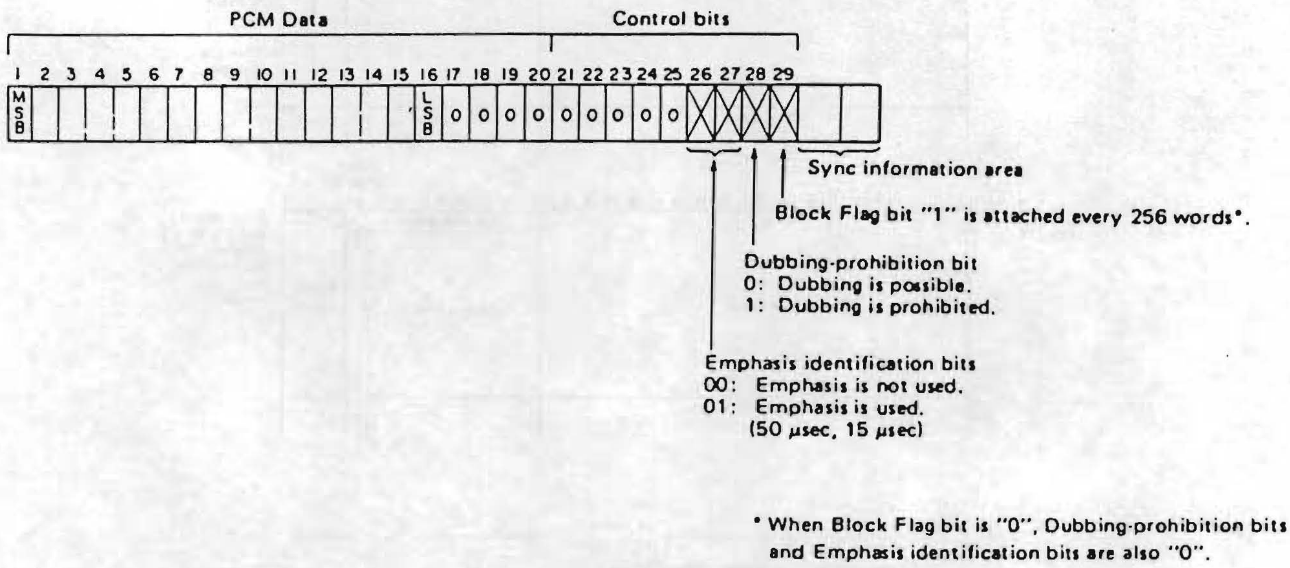


Figure 7-30 Control Signal Block Structure

7.6.2. Configuration

Digital I/O block consists of the following three main blocks:

(1) Parallel I/O block
(2) Serial I/O block, and
(3) Static protection circuit block.

Blocks 1 and 2 are mounted on the I/O board and block 32 is mouinted on the CN board.

2-1 Parallel I/O block

Figure 7-31 shows the block diagram

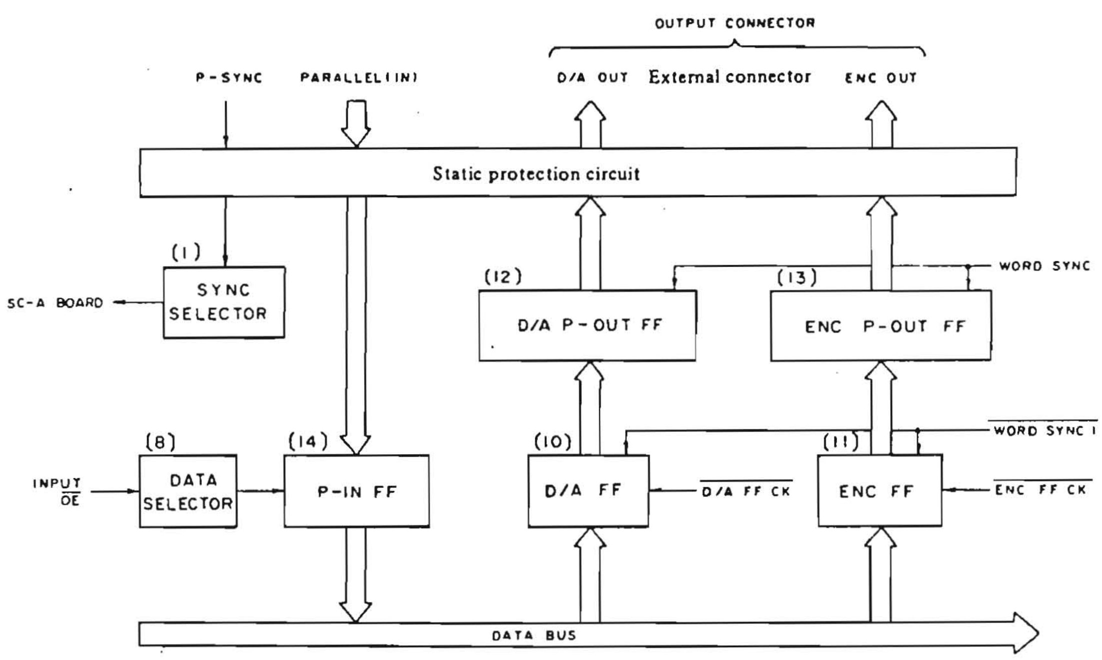


Figure 7-31 Parallel I/O Block Diagram

2-2 Serial I/O Block

Figure 7-32 shows the block diagram

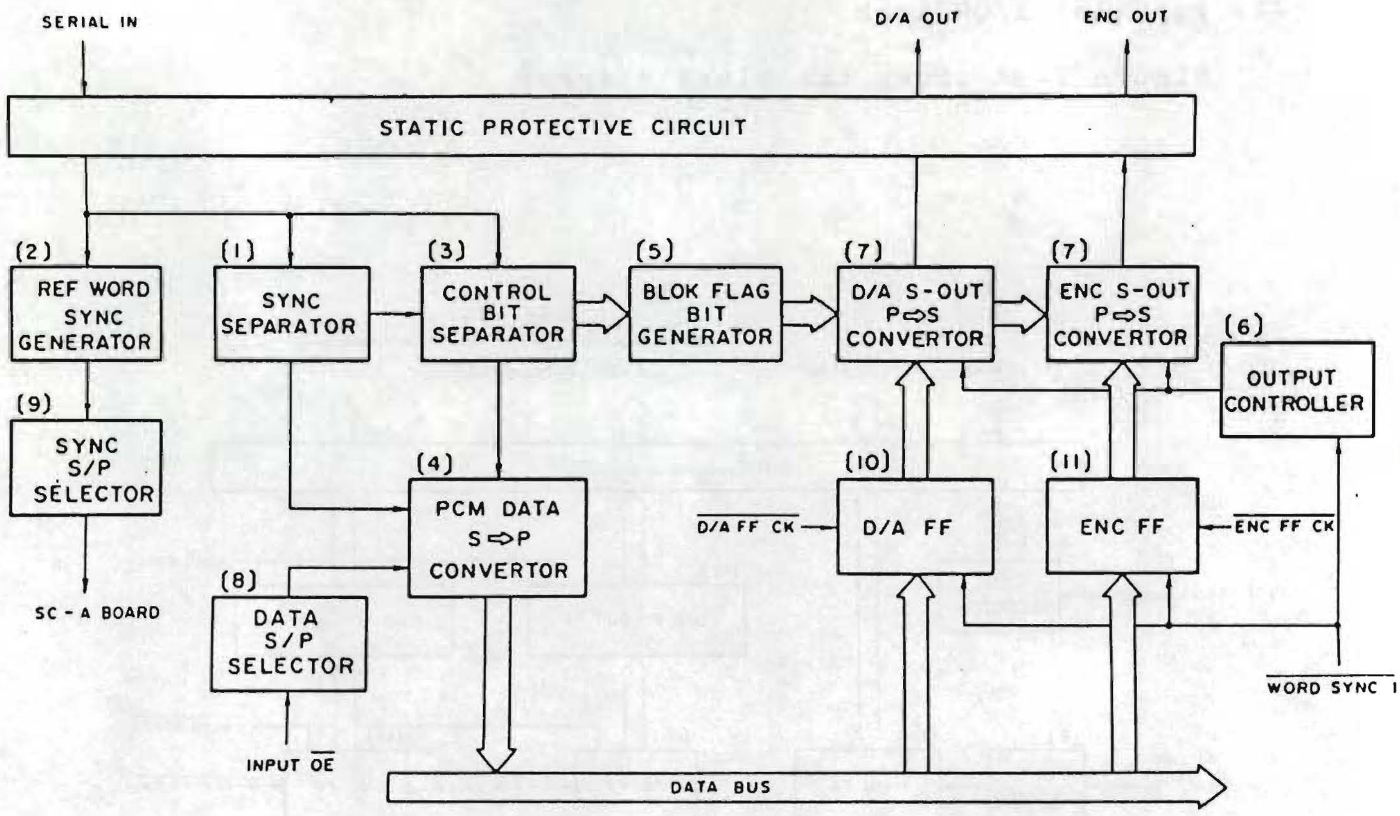


Figure 7-32 Serial I/O Block Diagram

7.6.3. Circuit Description

7.6.3.1 Parallel Input

A) Parallel data entering the P in FF via the static protection cirucit is latched by input OE signal, and is output to the data bus. When input OE is high, the output of the P-in FF is in 3 states.

B) Parallel Output

ENC data latched from the data bus at the ENC FF by ENC FF CK is output by WD SYNC1, and enters the ENC P out FF. There, ENC data is latched with the rising edge of the output control circuit counter (IC-D1Qc) and is output to the external connector via the static protection circuit. Ic-D1Qc can also be used as an S-out SYNC signal. Similarly, D/A data is output to the external connector by the D/A FF and the D/A P-out FF.

7.7 Serial I/O Block (I/O Board)

7.7.1 A) Serial Input

Serial data enters the sync separator circuit, the ref word sync generation circuit, and the control bit separator circuit via the static protection circuit.

7.7.2 Sync Separator

Serial data (ch-1) entering IC-C3 is latched twice by an 11.3MHz clock, and data with a difference in phase is output. From this data, edge pulses for data block are obtained by exclusive-O Ring (IC-C2). From these edges pulses and using the high create clock counter (IC-D4) and IC-G3, E3, D3, only the edge pulses between each 1.5T of word sync are extracted. From these extracted edge pulses, a data latching clock (IC-C420) is made with the J.F flip flop. Similarly, for serial data (ch-2), a data latching clock (IC-C41Q) is made. (Figure 7-33A).

7.7.3 Ref Word Sync Generator

Serial data (ch-1 and ch-2) enters the data selector (IC-A2). Normally, ref word sync is formed from serial data ch-1, but when ch-1 input is absent, ch-2 is selected by the data selector. The output from the data selector is latched twice by the D-FF,d and edge pulses are obtained from the data blocks. With these edge pulses and the high rate clock counters (IC-E2) and IC-F2, F1, serial input ref word sync is formed.

When ref word sync signals are sent to the SC-A board, the sync S/P selector selects either local sync or external P-in SYNC input. In this circuit, a precision quartz clock (9.83MHz) is used. (Figure 7-33B).

7.7.4 Control Bit Separator

PCM Data S -->P Converter

Serial data (ch-1) entering the shift register (IC-A5) is shifted, register by register through IC-A4, IC-A8 and IC-A7 by the bit clock (32fs) which is the Qc output of the high rate clock counter (IC-D4). In this way, when the data latch clock formed in the sync separator circuit starts to rise, the output of the shift register (IC-A7) QH, QG, QG...becomes serial data; MSB, 2SB, 3SB....and LSB is output to IC-A8 QA. At QHK, QG, QF and QE of IC-A5, serial data bits 25, 26, 27 and 28 are output and are latched in the D-FF (IC-B5) by the latch clock.

At this time, sync bit is output form QC of IC-A5 and this output enters data selector IC-B4. Data input to IC-B4 is the input sync bit and the output of the block flag bit generator. When sync patterns are present in the input signals, the input signal control bit is output as it is.

PCM data stored in the D-FF (IC-B7, B8) is output to the data bus with input OE signals.

Control bits stored in the D-FF (IC-B5, C7) enters D/A S-out P--->S converter, and the EMC S-out P-->S converter respectively. A similar process takes place with the serial data for (ch-2).

7.7.5 Serial Output Block

7.7.5.1 Block Flag Bit Generator

When no signals from the sync separator edge detection circuits IC-C2 pin 11, (ch-1), IC-C2 pin 3 (ch-2) is detected, during WD SYNC-1 is input four times, the output of data selector IC-B4 is switched over to the carry output of IC-B1 output goes high once every 256 word sync clocks. Block flag bit and sync bit made by this block enter control bit D-FF (IC-B5) in accordance with the serial I/O format.

7.7.5.2 Output Controller

S-out P-->S converter load signals, clock inhibit signals and control bit D-FF OE signals are produced by the 2.8mHz clock counter.

7.7.5.3 S-out P-->S Converter

While word SYNC 1 is low, PCM data stored in the ENC FF is output to the shift register. Since word SYNC 1 signal simultaneously, serve for S-out P-->S shift register IC-C7, C8, 16-bit PCM data is loaded, and is shifted register by register to become serial output. When data is output from MSB to LSB, data from the control bit of D-FF (IC-C5) is loaded in the lower shift register (IC-C8). At this time, the upper shift register is filled with all "0's". In this way, serial data is output in accordance with the serial I/O format. The clock inhibit signals from the output controller form 1.5T sync patterns. When an unlock signal from the SC-A board enters the shift register, the shift register is cleared and outputs all 0's. (See Figure 7-34).

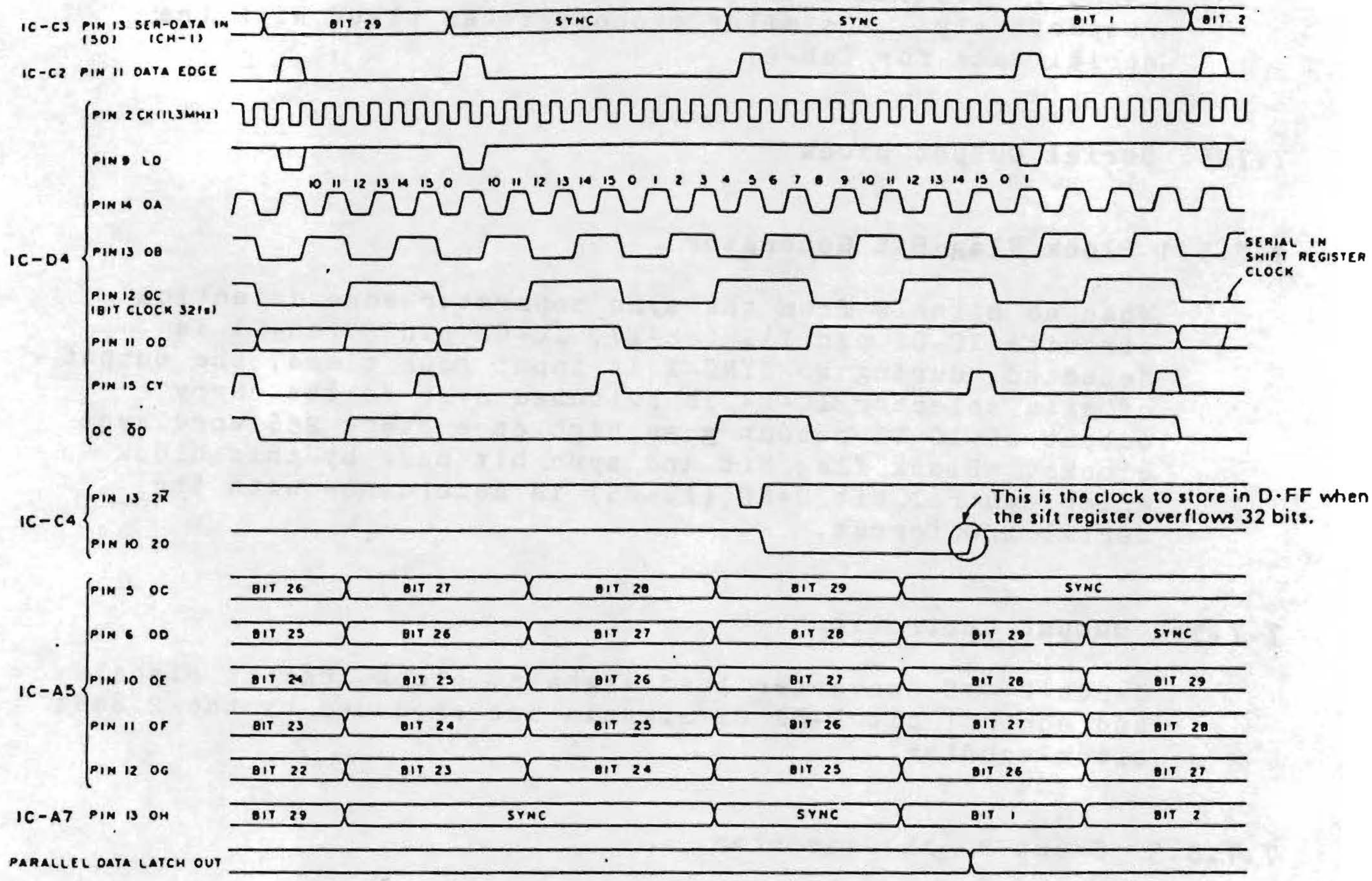


Figure 7-33A Serial in SYNC Generator

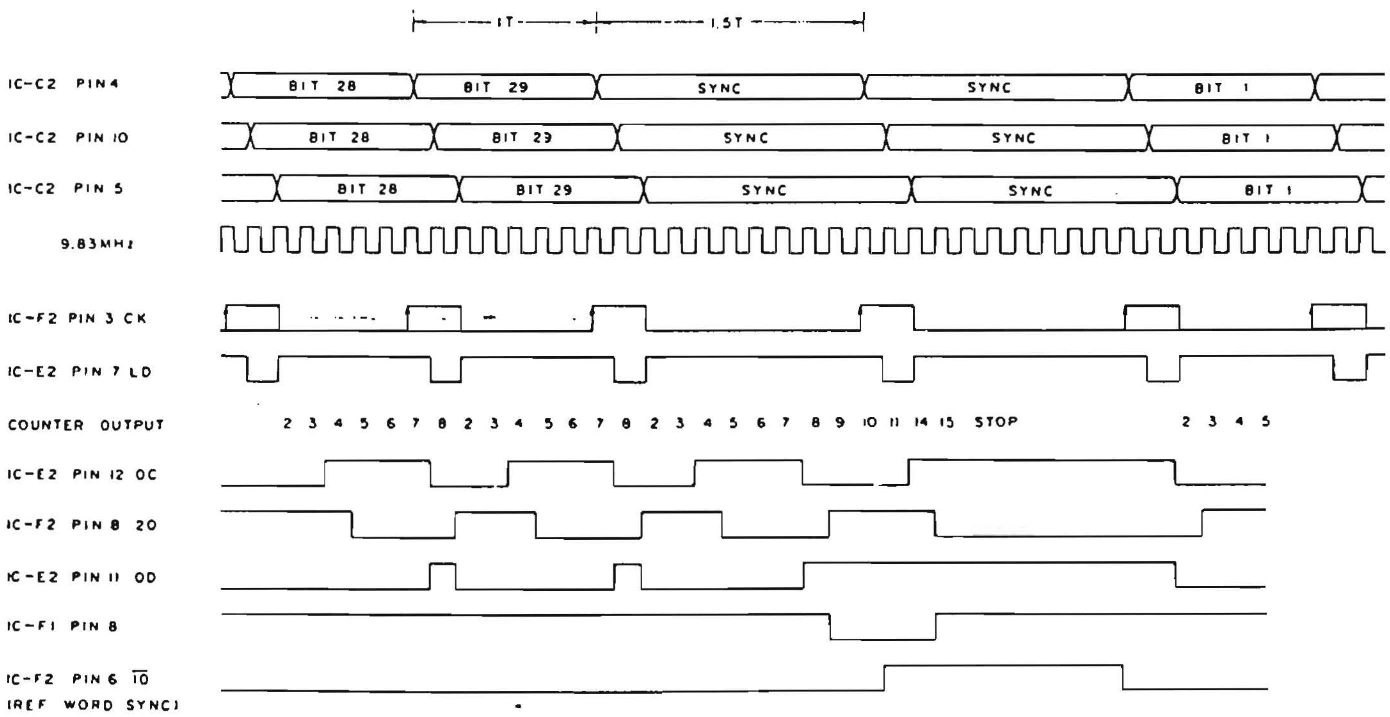
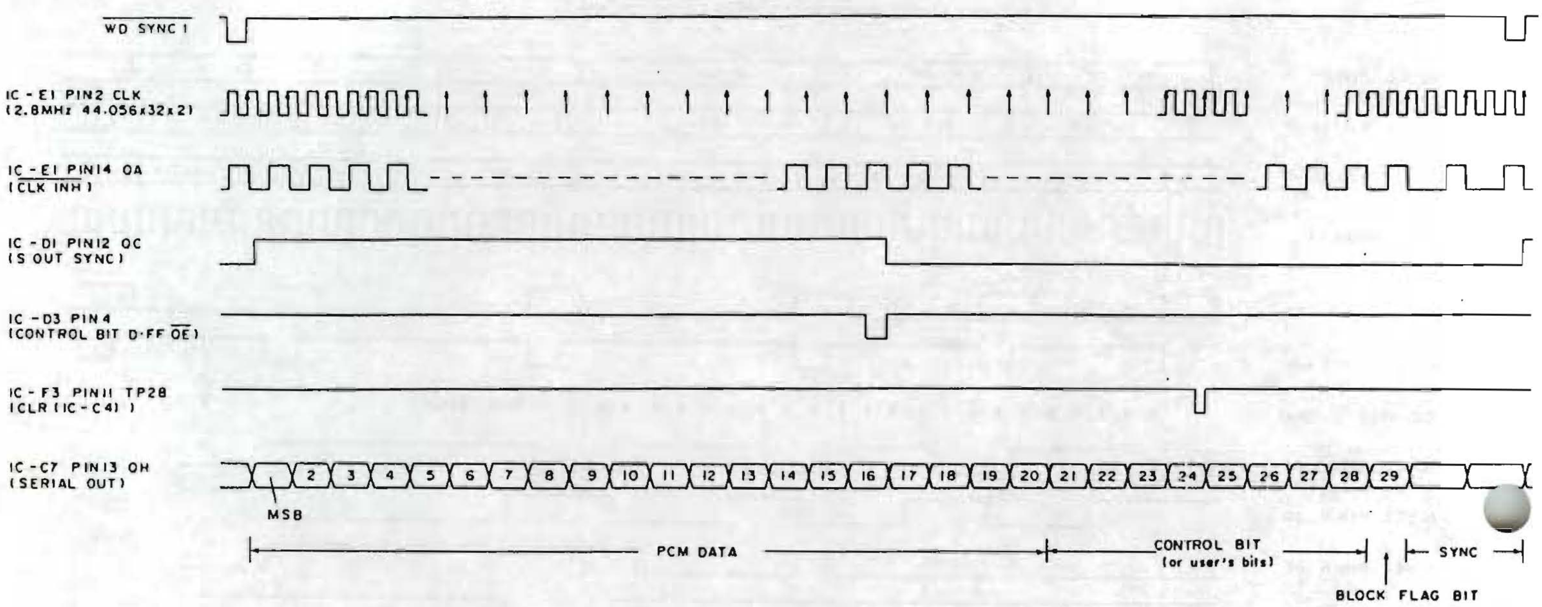


Figure 7-33B Serial in REF WD SYNC Generator



- When WD $\overline{\text{SYNC}}$ 1 is low the ENCFF PCM data is output and at the same time it is loaded into S P shift register (ICs C7, C8, E7 and E8).
- When $\overline{\text{CLK/NH}}$ is low the 2.8 MHz CLK is not counted, so from the MSB up to bit 29 is output within 1T and SYNC is output with 1.5T. (Effective only on the rising edge is the timing chart)
- The QC of IC-D1 is output as the S out sync, and becomes the parallel out FF check clock.
- When pin 4 of IC-D3 is low, the control bit data of the control bit DIFF (IC-C5) is output and at the same time the lower S —— P sift register (IC-C8) is loaded.
- When pin 11 of IC-F3 is low the sync separator T·$\overline{\text{R}}$ FF is cleared and the next sync edge is searched.
- This signal is the same format as the CH-2 output to ENC and the output to the D/A.

Figure 7-34

7.8 Static Protection Circuit (CON Board)

7.8.1 Parallel out (To ENC: to D/AO

The parallel-out circuit consists of a buffer (7407) for driving the parallel output (for PCM-1600) from the I/O board at TTL level, and a static protection circuit (Figure 7-35).

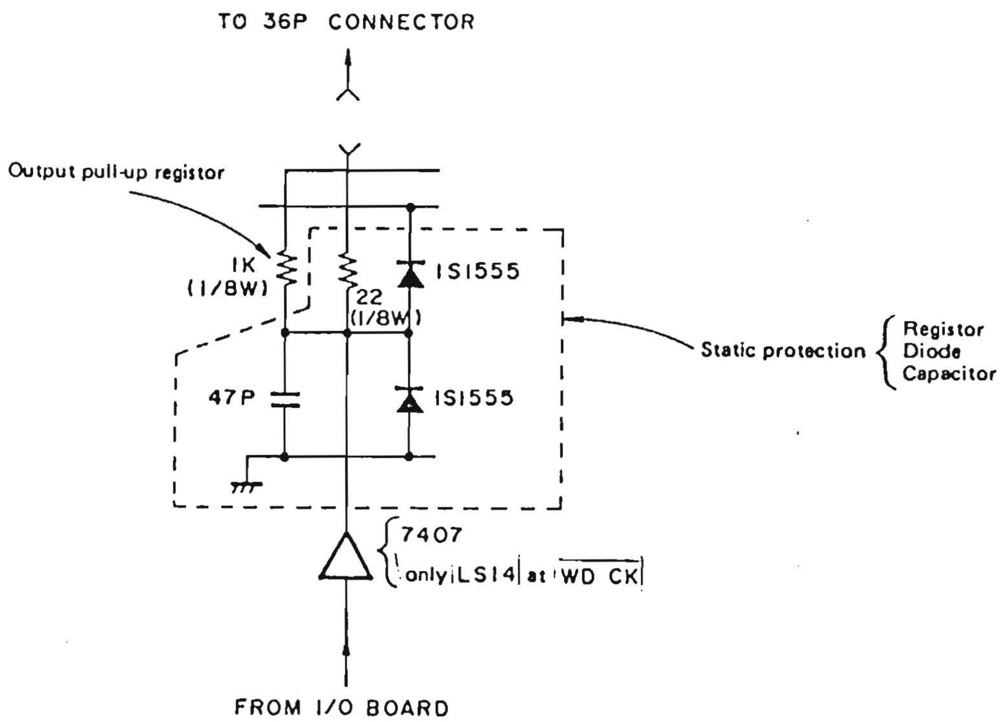


Figure 7-35 Parallel Out Buffer

Static charge which is directly discharged through the connector terminals and passes through a 22 ohm register and is bypassed to the supply side or to the GND by a diode to protect IC(7407). As diode 1S1555 cannot follow sharp rises in voltage, the transient time is extended with a ceramic capacitor (47pF) connected between the signal line and the GND. There are 32 output lines (data 32 bits) both for END and D/A, one output line for WD CK (parallel) and two ground lines.

7.8.2 Parallel In

Parallel input from PCM-1600 is sent to the I/O board. this circuit is also provided with a static protection circuit (Figure7-36).

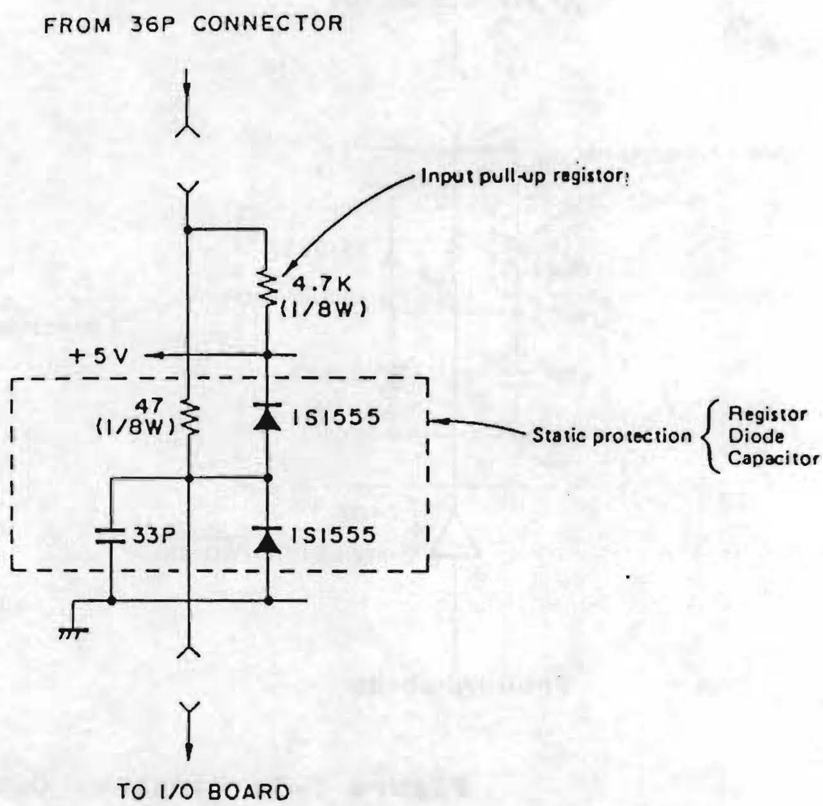


Figure 7-36 Parallel in *Buffer*

There are 32 input lines for 32-bit DATA, one line for WD CK (parallel) and two GND lines. WD CK is buffered by IC-A9 (75122) and then one line is sent to the I/O board and further buffered in two stages by IC-B9 (LS14) and output to PARALLEL OUT (both ENC and D/A).

7.8.3 Serial Out

This circuit consists of a driver for the 75 ohm coaxial cable by serial output from the I/O board, and a static protection circuit. (Figure 7-37). Output is four sets of DATA lines (ENC 2CHs, D/A 2 CHs) and one line for SERIAL OUT WD SYNC.

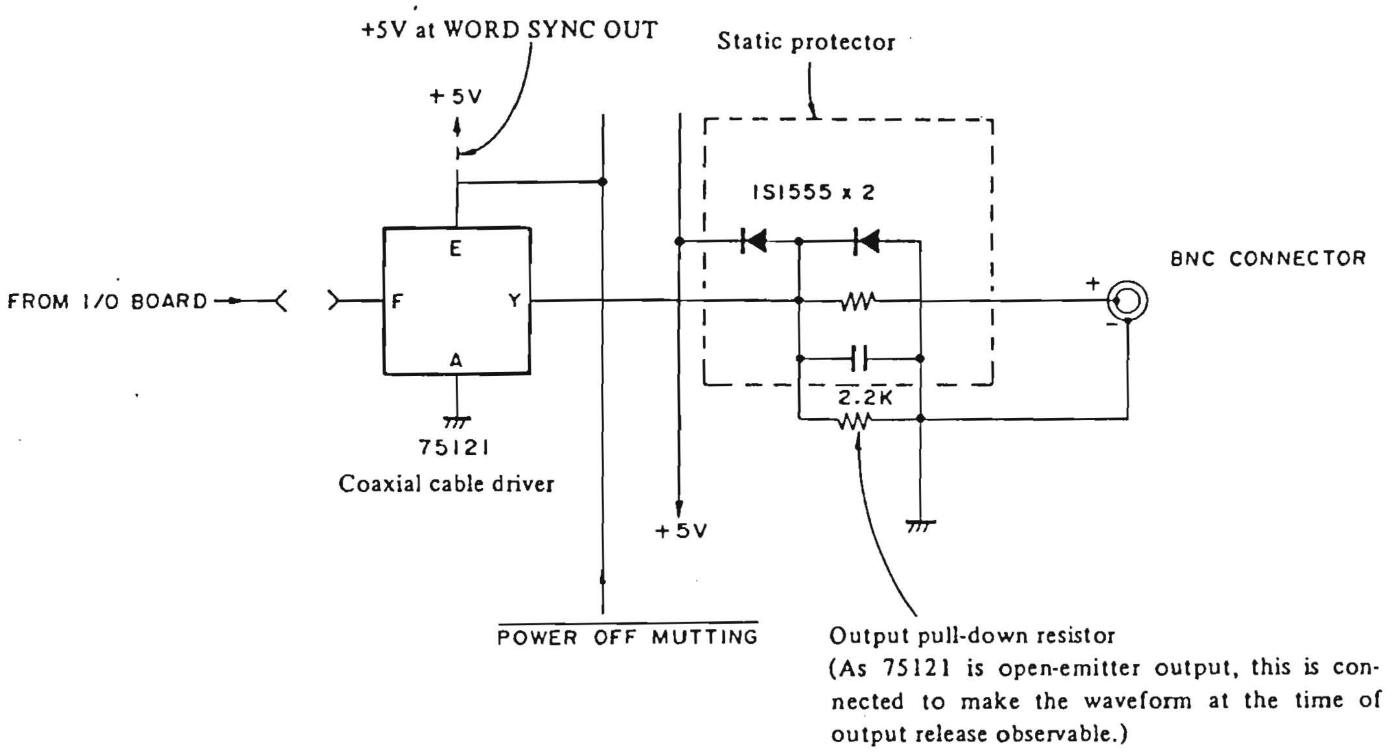


Figure 7-37 Serial Out Buffer

7.8.4 Serial In

This circuit consists of a line receiver for the 75 ohm coaxial cable and a static protection circuit and serves to send serial input to the I/O board. There are only two sets of input lines which are DATA lines.

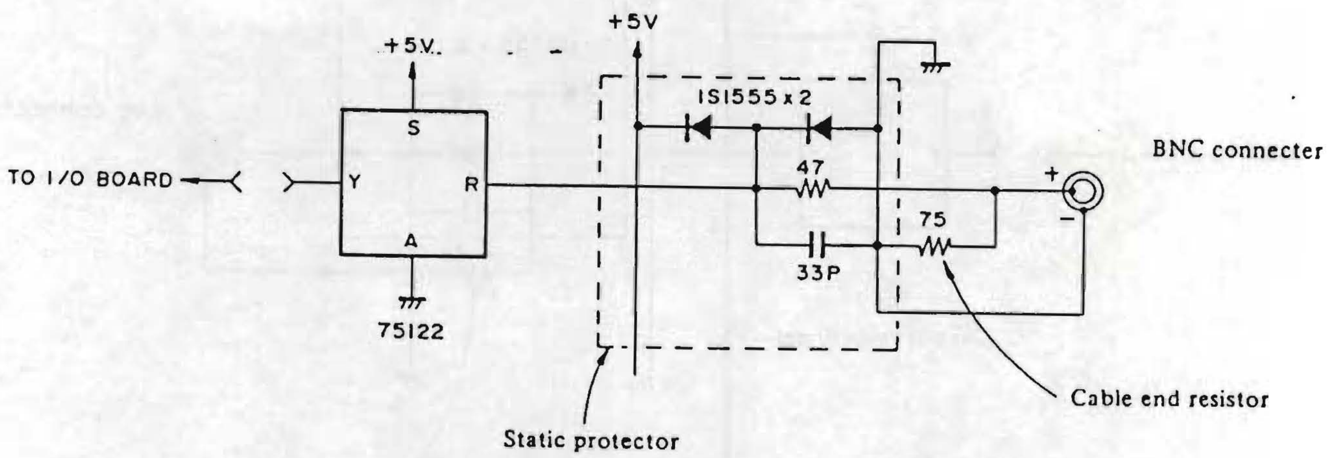


Figure 7-38 Serial In Buffer

7.8.5 Power ON/OFF Muting Circuit

This power ON/OFF muting circuit forces the parallel/serial data output to all 0's to eliminate noise when the power suply is turned on and off, or when PLL lock (SC-A board) has failed to lock.

When the power supply is turned on,the input to IC-B9 (SN74LS14) is delayed from the rise of supply voltage by R154 (33k-ohm) and C130 (33-uF), and the output of IC-B9 (6) becomes high. this causes Q1 (2SC1362) to turn on and Q4 of the differential amp to turn off. At this time, the Darlington pair made up of Q6 and Q3 is also turned off and drive, Q5 (2SA772) to bring the parallel data output to all 0's is turned on. As its emitter is connected to the static protection diode for the parallel digital out circuit, the output becomes all 0's. The serial digital output becomes all 0's as the enable signal of driver IC (SN75121) becomes low. When PLL does not lock, Q1 is turned off by UNLOCK signals in the same way as when the power is turned on to obtain a muted output.

When the power supply is turned off, the emitter of Q4 of the differential amp is kept at the same voltage by the charge stored in C131 (100uF) to turn off the output of the differential amp, and hence to turn off Q6 and Q3.

In this way, the Q5 emitter and the output of IC-B9 (12) is brought low to result in output muting.

During these mute output periods, the power supply to the driver (open-collector output) resistor of the parallel digital output is also turned off.

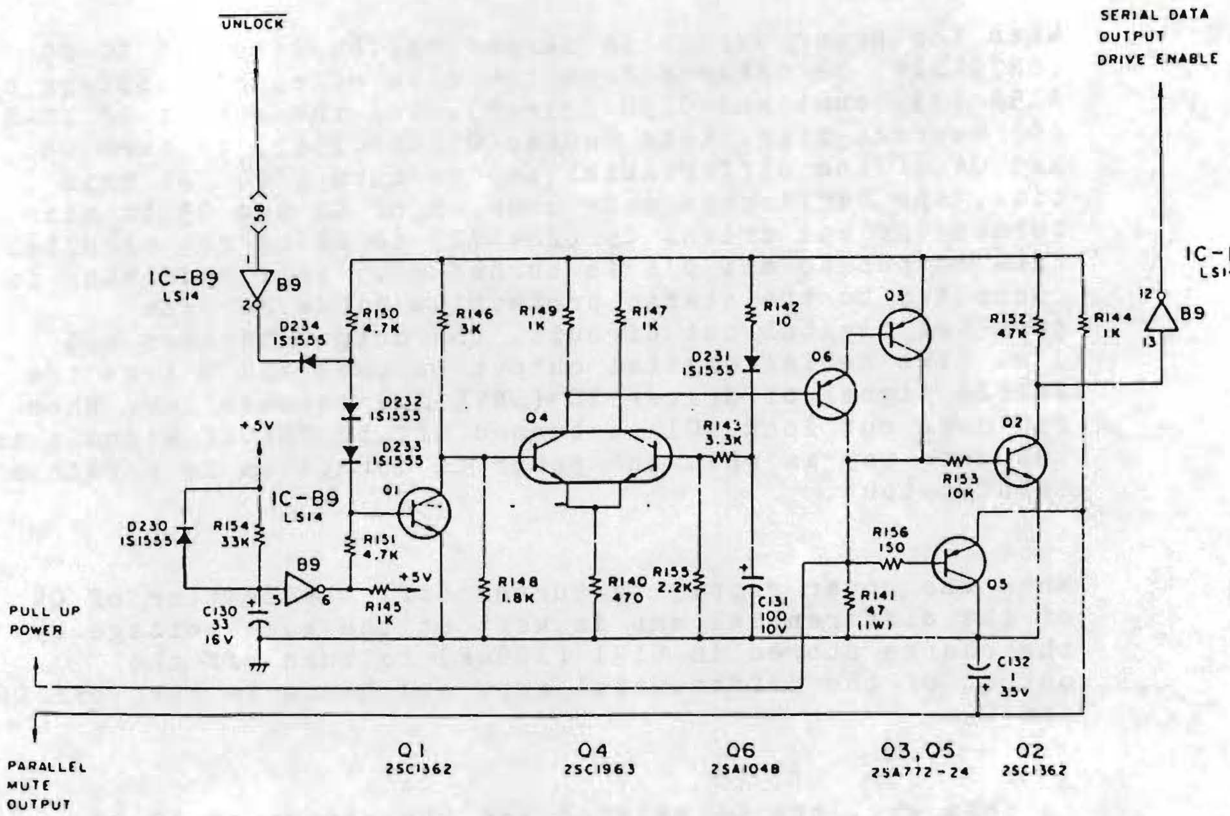


Figure 7-39 Power On/Off Muting Circuit

7.8.6 VTR Remote Static Protection Circuit

VTR remote control output from the SYS board and status input are connected to the remote connector via a static protection circuit, as with digital I/O signals. (Figure 7-40)

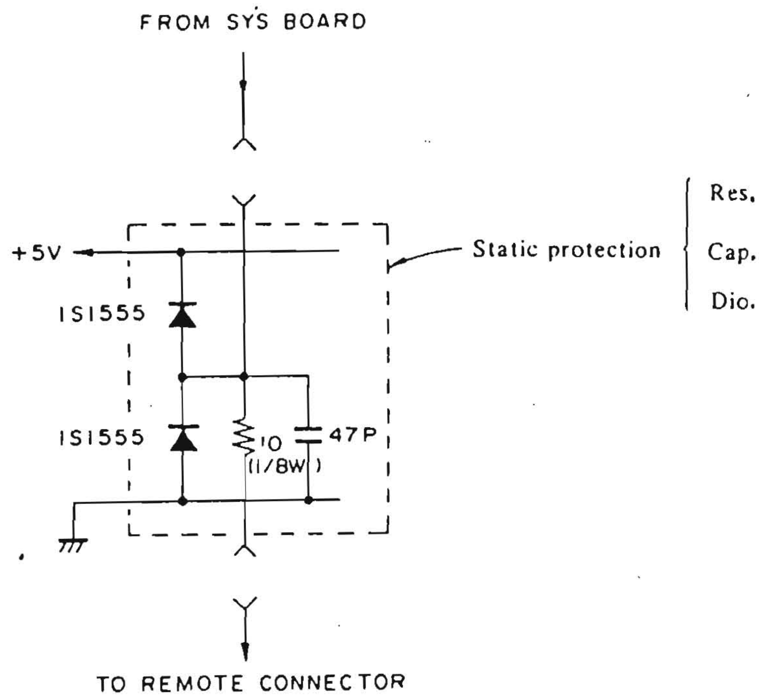


Figure 7-40 VTR Remote Static Protection Circuit

7.9 MEMORY CIRCUIT (MEM BOARD)

7.9.1 Introduction

5.95 seconds of compressed PCM data are recorded into the memory circuit of the **DAE-1100** and subsequently read out for the purpose of cueing the edit point.

In Preview or Edit mode, in order to match the Recorder data and the Player data, the memory circuit (Edit Mode Memory) is used for the Play delay data and the D/A output delay from the encoder output.

As the Search mode memory and the Edit mode memory cannot be used simultaneously, the same memory can serve both purposes. the memory cirucit comprises 64 16K-bit dynamic RAM chips (MK-4116-3, MB8116E etc.) for 1M bits (32K words X 32 bits) of memory.

Since the memory circuit uses dynamic RAM, refresh is necessary. The refresh circuity is incorporated in the memory circuit and from the outside the RAM appears as static. The MEM Board consists of more than just the memory circuit; it also includes a Check circuit.

7.9.1 Configuration

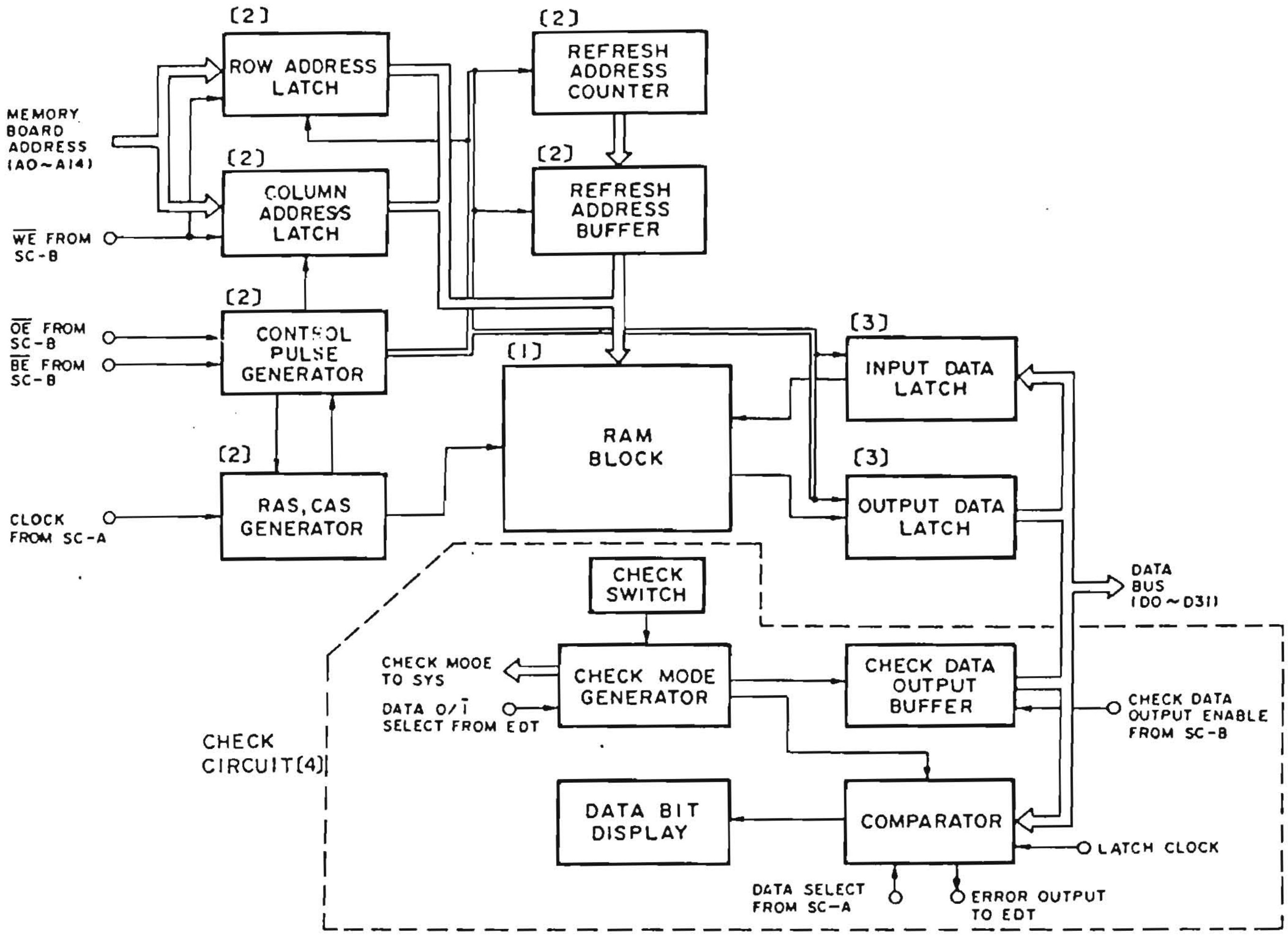
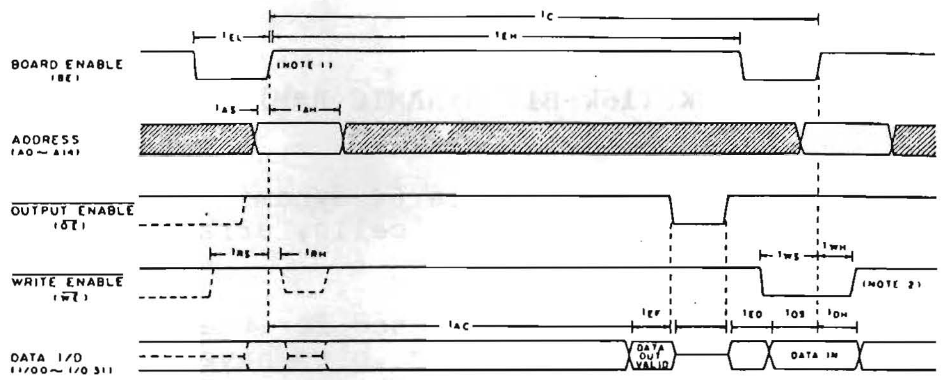


Figure7-41 Block Diagram for MEM board

The memory circuit block schematic is shown in Figure . The Check circuit has been included but is not described in detail.

The memory uses 16K-bit dynamic RAMs (MK-4116) configured as 32K words X 32 bits = 1M bits. A 15 bit address (RA_0 - RA_{14}) selects each word which is output as 32 bits of data (RD_0 -RD_3) on a bidirectional data bus. In order for the memory circuit to appear to be static RAM externally, the Row/Column addresses are separated and RAS (Row Address Strobe) and CAS (Column Address Strobe) control signals are generated in the board. All 128 Row addresses of the 16K bit dynamic RAM must be individually refreshed within 2 msec; automatic refresh control occurs in the memory cirucit.

When a 11.27832MHz clock is input to the memory board, addresses RA_0 - RA_{14} and $\overline{WE}$ (Write Enable) will be latched on the rising edge of BE (Board Enable). In the Write Mode, the Data Input RD_0 -RD_{31} are also latched at the same time. The access time from the memory board BE is 1 usec. When $\overline{WE}$ is low, the data bus is automatically tri-stated and control is in the same manner as when OE (Output Enable) is low.



Note 1: Raising edge of BE Latches $A_0 \sim A_{14}$, WE, and Data Inputs ($I/O_0 \sim I/O_{31}$).
Note 2: Data outputs hold high impedance (Z) when WE is in the low state.

Figure 7-42 Memory Block Switching Waveforms

Table 7-9-1 Switching Characteristics

Parameters	Description	Test Condition	Min.	Max.	Units
t_C	Cycle Time	Master Clock (MSTCK = fφ) = 11.27832 MHz	1.0		μs
t_{AC}	Access Time (Be to Output Valid Delay)			1.0	μs
t_{AS}	Address to Board Enable Set-Up Time	Transition Time ≤ 20 ns	50		ns
t_{AH}	Board Enable to Address Hold Time	Output Load = 1 TTL Gate +50PF	10		ns
t_{RS}	Read to Board Enable Set-Up Time		30		ns
t_{RH}	Read to Board Enable Hold Time	Input and Output Timing Reference Level are 0.8V and 2.0V.	10		ns
t_{WS}	Write to Board Enable Set-Up Time		30		ns
t_{WH}	Write to Board Enable Hold Time		10		ns
t_{EO}	OE or WE to Output ON Delay		80		ns
t_{EF}	OE or WE to Output OFF Delay		80		ns
t_{DS}	Data Input Set-Up Time		50		ns
t_{DH}	Data Input Hold Time		10		ns
t_{EL}	Board Enable LOW Time		50		ns
t_{EH}	Board Enable HIGH Time		50		ns

7.9.2 Circuit Description

7.9.2.1 RAM BLOCK (16k-BIT DYNAMIC RAM)

The memory circuit uses 64 dynamic RAM chips comprising 16K word X 1 bit memory cells, arranged as 32K words x 32 bits.

MK-4116-3 chips may be used for the 16K word X 1 bit dynamic RAM. The address bits have to have separate 7 bit Row and Column timing. The uppermost address line of the memory board input, RA_{15} is used as a chip select since a 32K words comprise two chips. The refresh cycle has to refresh each row address within 2 msec.

Figure 7-43 shows the block schematic of a 16K bit dynamic RAM (MK-4116) and Figure 7-44 shows the pin layout.

Table 7-9-1 gives the electrical characteristics of the MK-4116-3 while Figure shows the Read Cycle waveforms, Figure shows the Write Cycle waveforms and Figure shows the Refresh Cycle waveforms.

In the Read cycle, the Row Addresses are latched on the falling edge of RAS while the falling edge of CAS latches the Column Address. RA_7 - RA_{13} of the Memory Board input addresses RA_0 - RA_6 form the Column addresses. In order to insure that the access time from RAS is 200nsec, the time from the falling edge of RAS to the rising edge of CAS must be less than 65nsec. However, in the **DAE-1100** memory block, one clock division delay (89nsec) is taken and so it is decided by the access time from CAS of 135nsec. The output data becomes valid on the rising edge of CAS and is latched by the rising edge.

The Write Cycle, as with the READ Cycle, latches the Row and the Column addresses on the falling edge of RAS and CAS; the input data is strobed by the later of the falling edge of CAS or WRITE and as Early Write Cycle is used in this memory, the data is input on the falling edge of CAS as valid data.

The Refresh Cycle functions on "RAS Only" and the Refresh Counter performs the refresh function on the 128 row addresses. In this circuit, the Refresh Cycle comes before and after Read/Write cycles.

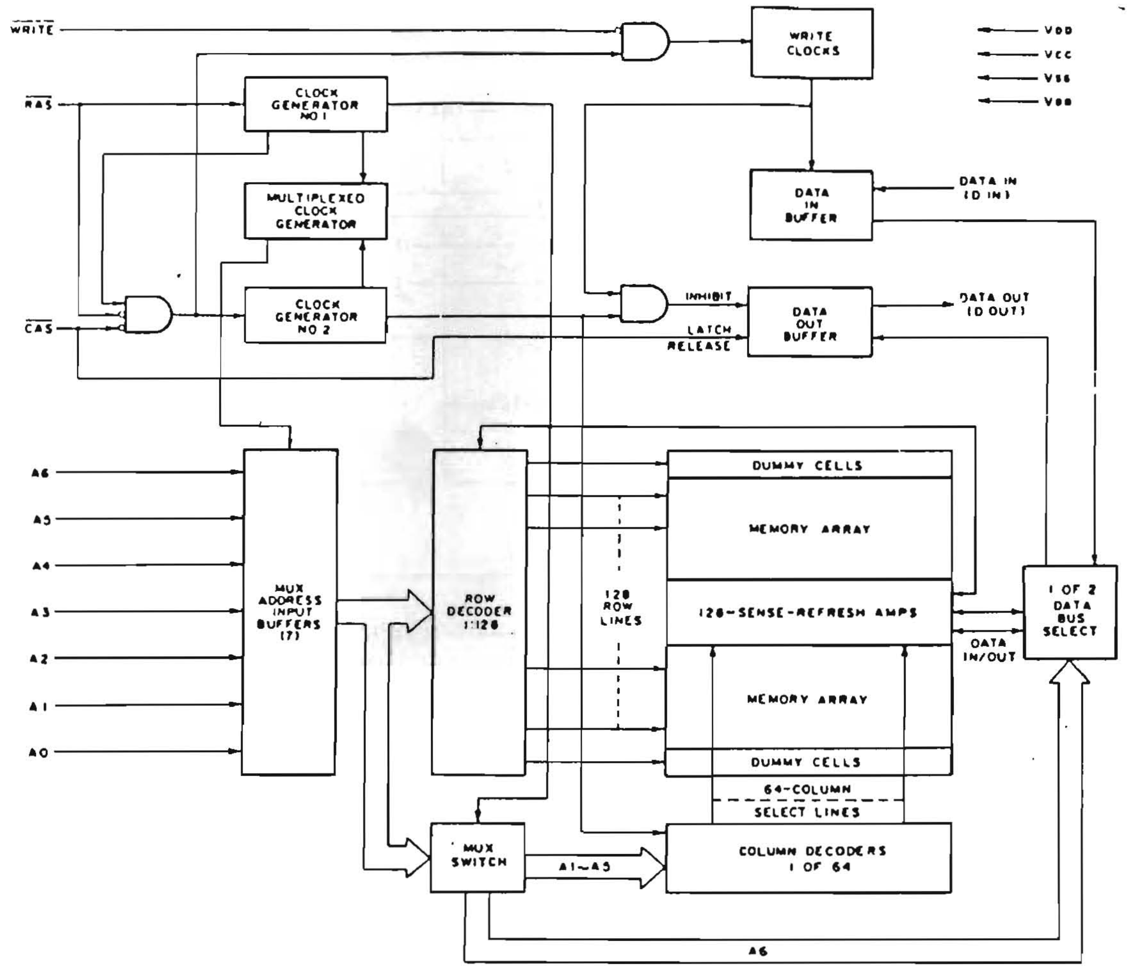
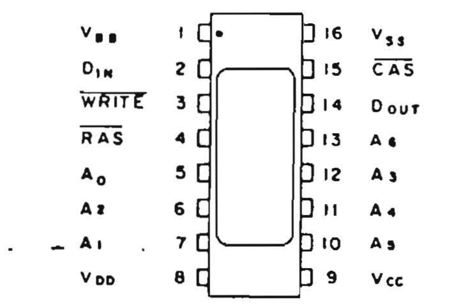


Figure 7-43 Function Diagram



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

Figure 7-44 Pin Connections

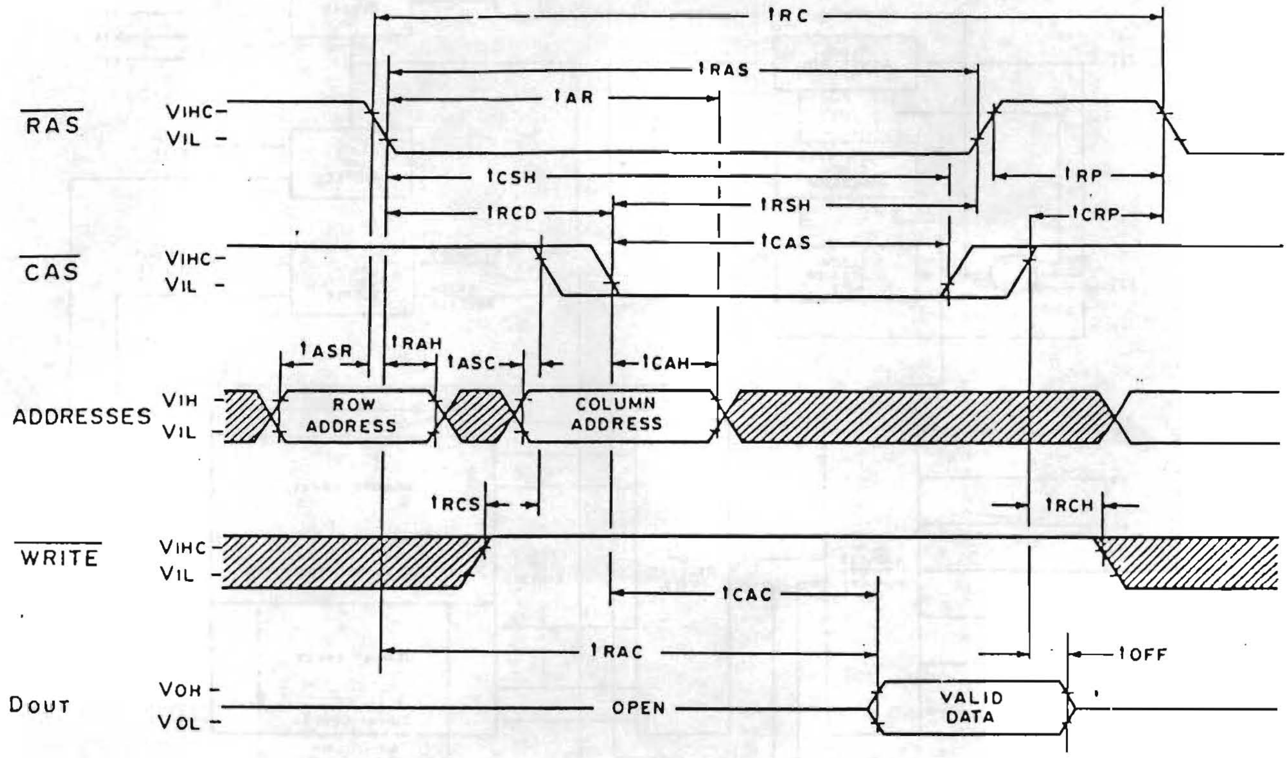


Figure 7-45 Read Cycle

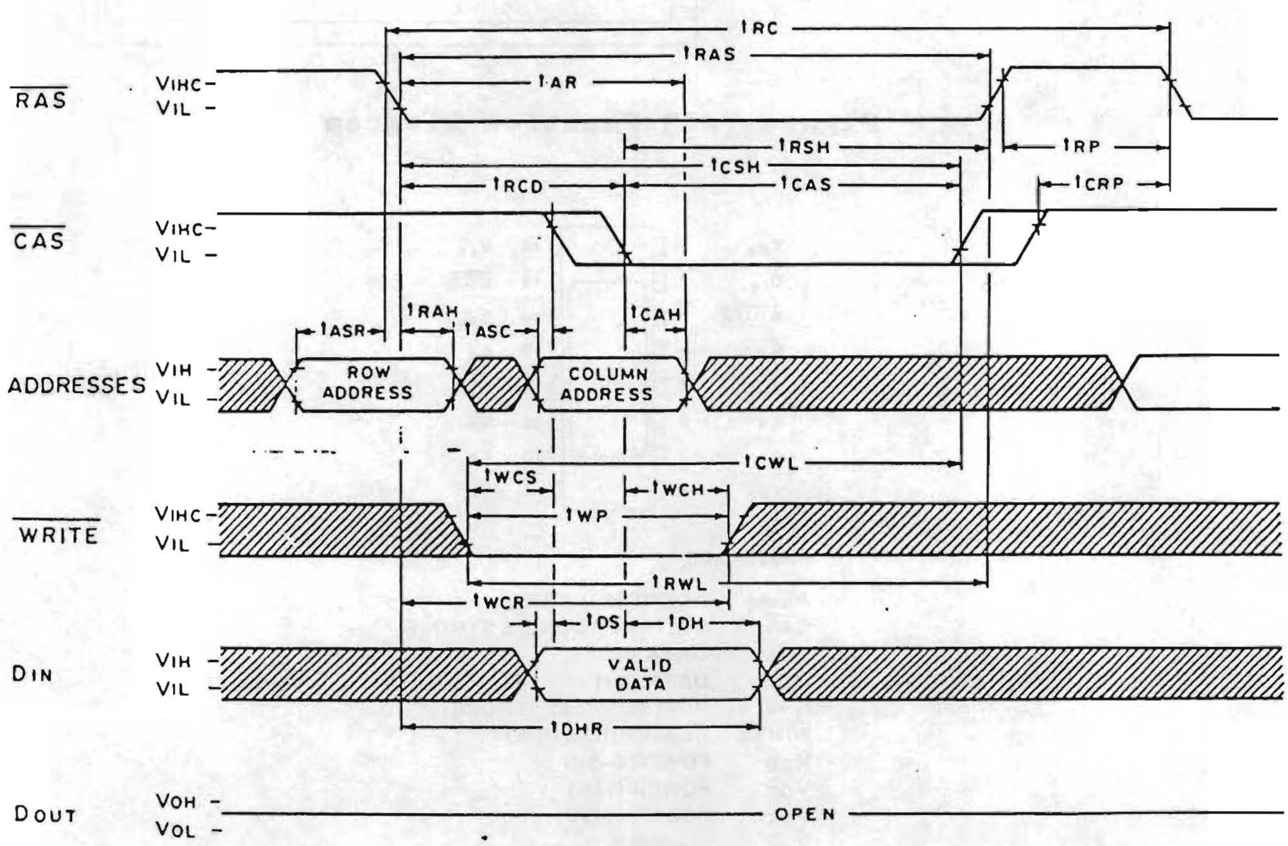
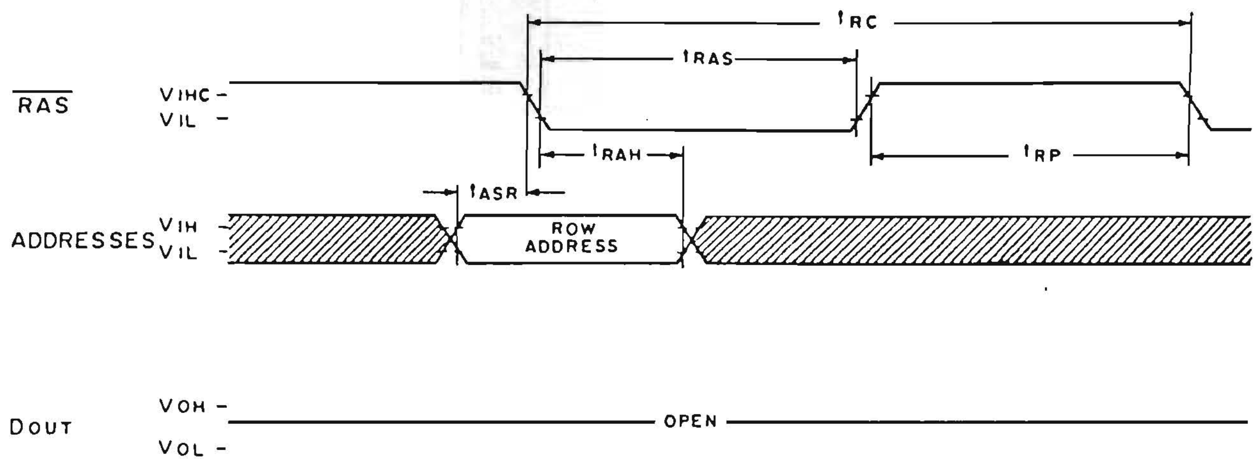


Figure 7-46 Write Cycle (early write)



Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

Figure 7-47 "RAS ONLY" Refresh Cycle

Table 7-9-2 Electrical Characteristics of MK4116-3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (1, 2, 3)
($0^\circ C \leq T_A \leq 70^\circ C$) ($V_{DD}$ = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, $-5.7V \leq V_{BB} \leq -4.5V$)

PARAMETER	SYMBOL	MK 4116-3		UNITS	NOTES
		MIN	MAX		
Random read or write cycle time	t_{RC}	375		ns	4
Read-write cycle time	t_{RWC}	375		ns	4
Read modify write cycle time	t_{RMW}	405		ns	4
Page mode cycle time	t_{PC}	225		ns	4
Access time from RAS	t_{RAC}		200	ns	5, 7
Access time from CAS	t_{CAC}		135	ns	6, 7
Output buffer turn-off delay	t_{OFF}	0	50	ns	8
Transition time (rise and fall)	t_T	3	50	ns	3
RAS precharge time	t_{RP}	120		ns	
RAS pulse width	t_{RAS}	200	10,000	ns	
RAS hold time	t_{RSH}	135		ns	
CAS hold time	t_{CSH}	200		ns	
CAS pulse width	t_{CAS}	135		ns	
RAS to CAS delay time	t_{RCD}	25	65	ns	9
CAS to RAS precharge time	t_{CRP}	−20		ns	
Row Address set-up time	t_{ASR}	0		ns	
Row Address hold time	t_{RAH}	25		ns	
Column Address set-up time	t_{ASC}	−10		ns	
Column Address hold time	t_{CAH}	55		ns	
Column Address hold time referenced to RAS	t_{AR}	120		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
Write command hold time	t_{WCH}	55		ns	
Write command hold time referenced to RAS	t_{WCR}	120		ns	
Write command pulse width	t_{WP}	55		ns	
Write command to RAS lead time	t_{RWL}	70		ns	
Write command to CAS lead time	t_{CWL}	70		ns	
Data-in set-up time	t_{DS}	0		ns	10
Data-in hold time	t_{DH}	55		ns	10
Data-in hold time referenced to RAS	t_{DHR}	120		ns	
CAS precharge time (for page-mode cycle only)	t_{CP}	80		ns	
Refresh period	t_{REF}		2	ms	
WRITE command set-up time	t_{WCS}	−20		ns	11
CAS to WRITE delay	t_{CWD}	80		ns	11
RAS to WRITE delay	t_{RWD}	145		ns	11

1. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2. AC measurements assume t_T = 5ns.
3. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
4. The specifications for t_{RC} (min) t_{RMW} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0 C < T_A < 70^\circ C$) is assured.
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
6. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
7. Measured with a load equivalent to 2 TTL loads and 100pF.
8. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
10. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify write cycles.
11. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

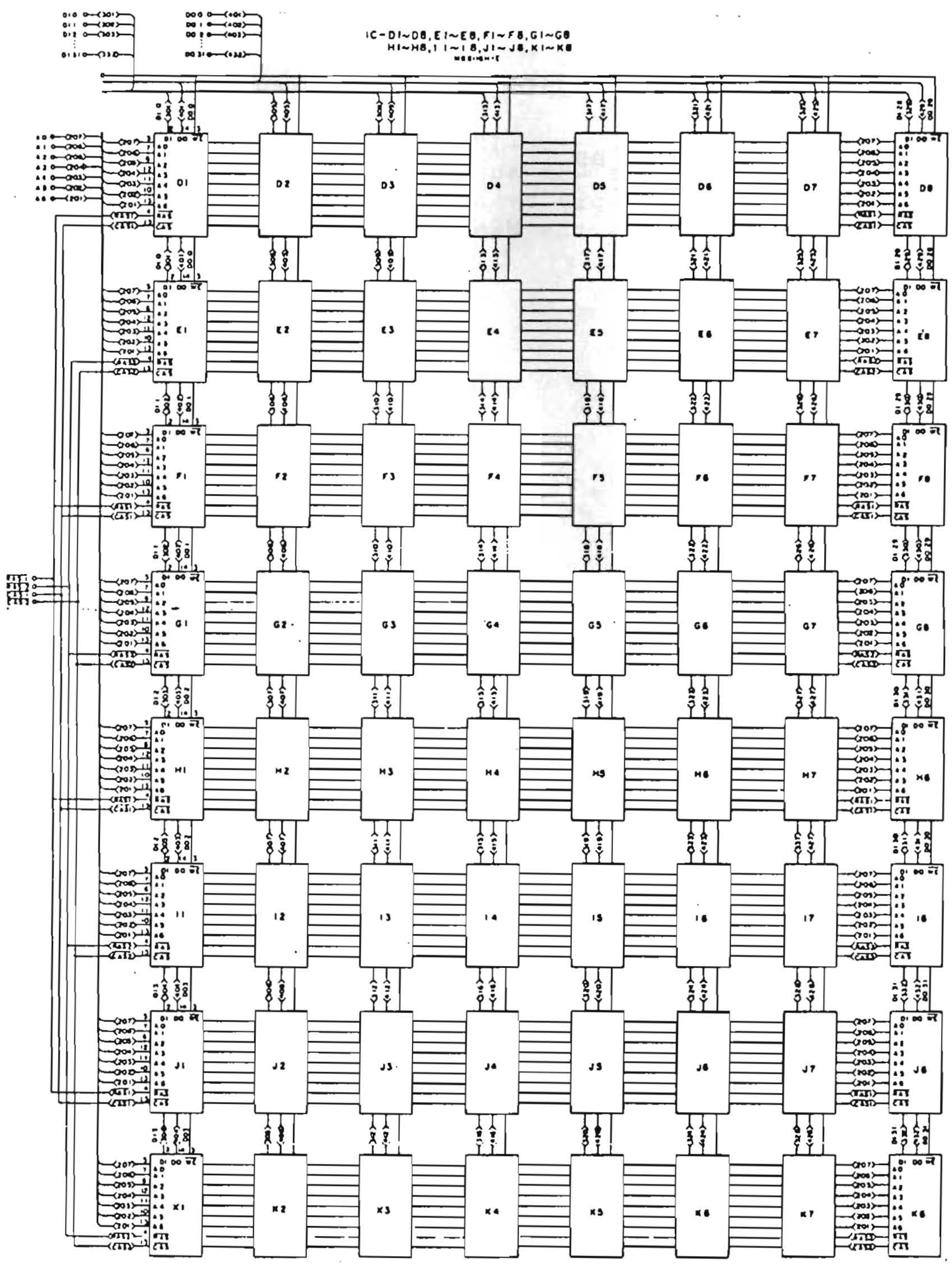


Figure 7-48 RAM Block Circuit Diagram

Three power supplies are required:

V_{CC} = +5V, V_{DD} = +12V and V_{BB} = -5V (V_{SS} = 0V = GND). The -5V supply, V_{BB} is derived from the -12V supply by a 3-terminal regulator (FS7905M) on the MEM Board.

7.9.3 ADDRESS AND CONTROL SIGNAL GENERATOR CIRCUIT

This block generates control signals so that externally the memory appears to be "static" although dynamic RAM is actually used on the board.

RAS and CAS and the Row/Column and Refresh addresses have to generated: the Read and Write control is based on the rising edge of the BE (Board Enabel) signal. An 11.3mHz clock needs to be supplied in order to generate the control signals.

Figure 7-49 shows the control signal generator circuit. The Clock (11.3M) BE and RAM OE are buffered in by IC-B2 (SN74LS125).

Figure 7-50 shows the internal timing and the name of each of these signals is indicated in the circuit diagram in Figure 7-49.

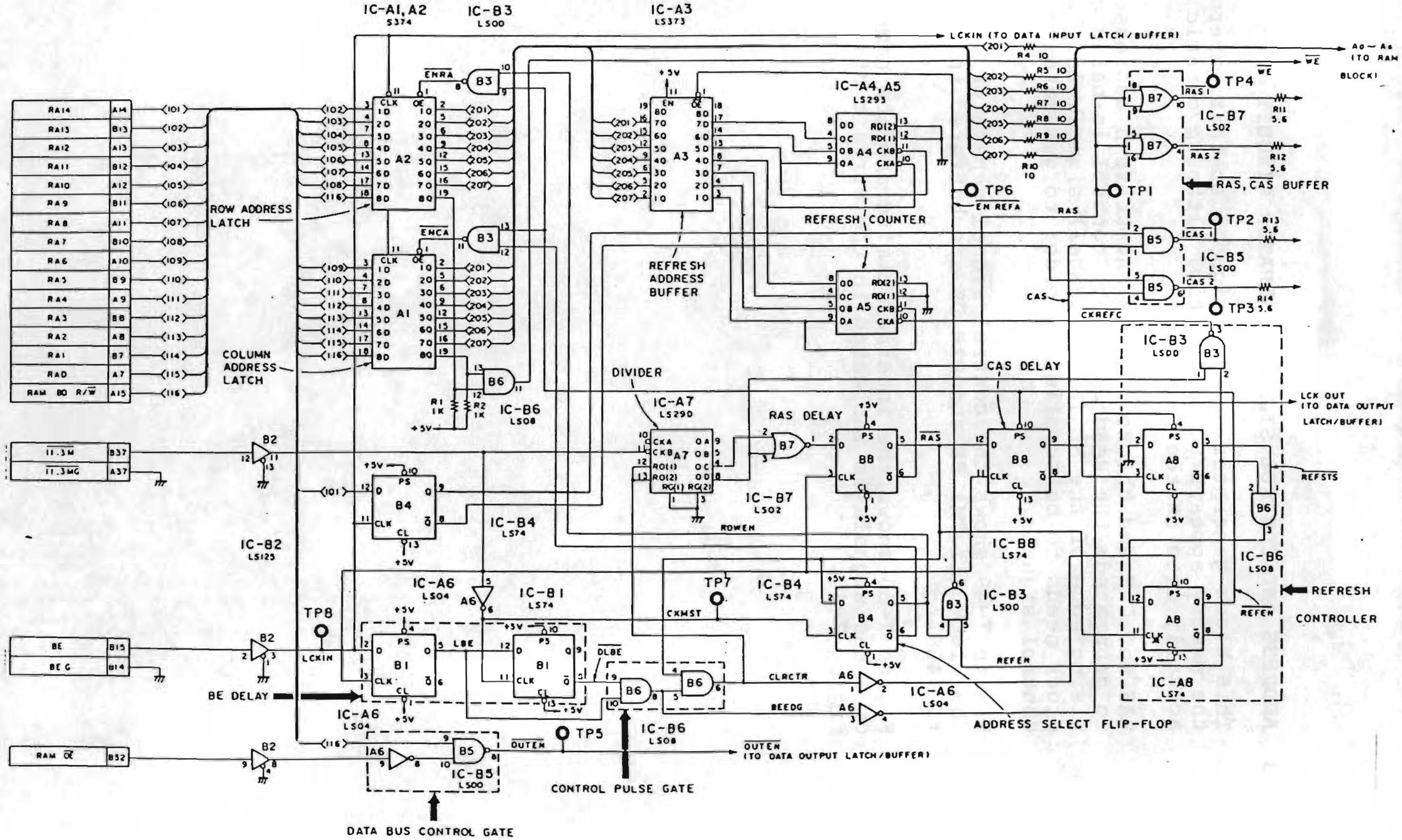


Figure 7-49 Address and Control Signal Generator Circuit

7.9.2.3 $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Generator

$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Generator comprises a divider (IC-A7:SN74LS290), a NOR gate (IC-B7:SN74LS02), a RAS delay (IC-B8: SN74LS74) a CAS delay (IC-B8) and the RAS and $\overline{\text{CAS}}$ buffer (IC-B7: SN74LS02; IC-B5: SN74LS00).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals for operation of RAM block Read, Write and Refresh use the Qc and Qd outputs of IC-A7 (SN74LS290) where the 11.3MHz clock has been divided by 5. The $\overline{\text{RAS}}$ signal low level pulse width needs to be more than 200 nsec and so it uses a pulse width of three periods of the 11.3MHz clock (266 nsec). The $\overline{\text{RAS}}$ signal high level pulse width needs to be at least 120 nsec and so it uses two 11.3MHz clock periods (177 nsec).

When the Qc and Qd outputs of the IC-A7 divider are NORed, the low and high level ratio will be 3:2 and so can be used as the RAS signal. The Qc and Qd NOR output signal (byIC-B7: SN74LS02) is delayed by 11.3MHz clock period in the IC-B8 (SN74LS74) RAS Delay and used as the RAS signal. The IC-B8 output is buffered by IC-B7 and is supplied to the RAM Block.

The $\overline{\text{RAS}}$ signal is supplied to the RAM block even when there is a Refresh Cycle, but $\overline{\text{CAS}}$ signal is supplied only during a Read or Write Cycle. During a Refresh Cycle, when a Read or Write BE is being input, $\overline{\text{CAS}}$ is controlled so that Read or Write Cycle is input after the refresh cycle has been completed. $\overline{\text{CAS}}$ has to be output after delay of 25 nsec or more after $\overline{\text{RAS}}$, but the RAM block addresses A_0 -A_6 have to change over from row addressed to column addresses up to 10 nsec after the falling edge of $\overline{\text{CAS}}$ (the column address setup time = - 10 nsec). Considering the Row/Column address switching, the CAS signal is generated from the $\overline{\text{RAS}}$ signal delayed by one 11.3MHz clock period in the IC-B8 CAS delay (falling edge only, 1 period: 89 nsec). During a Refresh Cycle IC-B8 is preset so that $\overline{\text{CAS}}$ will not be output. When the Refresh Cycle is completed and $\overline{\text{RAS}}$ goes high, the IC-A7 divider (SN74LS290) is cleared so that the Read or Write Cycle starts and RAS and CAS are generated.

Since the RAM Block comprises 32K words X 32 bits, chip select is by RA_{14} selecting CAS_1 or CAS_2. The dynamic RAM data output becomes valid on the rising edge of the $\overline{\text{CAS}}$ signal and $\overline{\text{CAS}}$ signal is used as the Data Output latch clock.

Refer to Figure 7-50 timing chart ($DIVQ_B$ -$\overline{\text{CAS}}$) for the timing of these blocks.

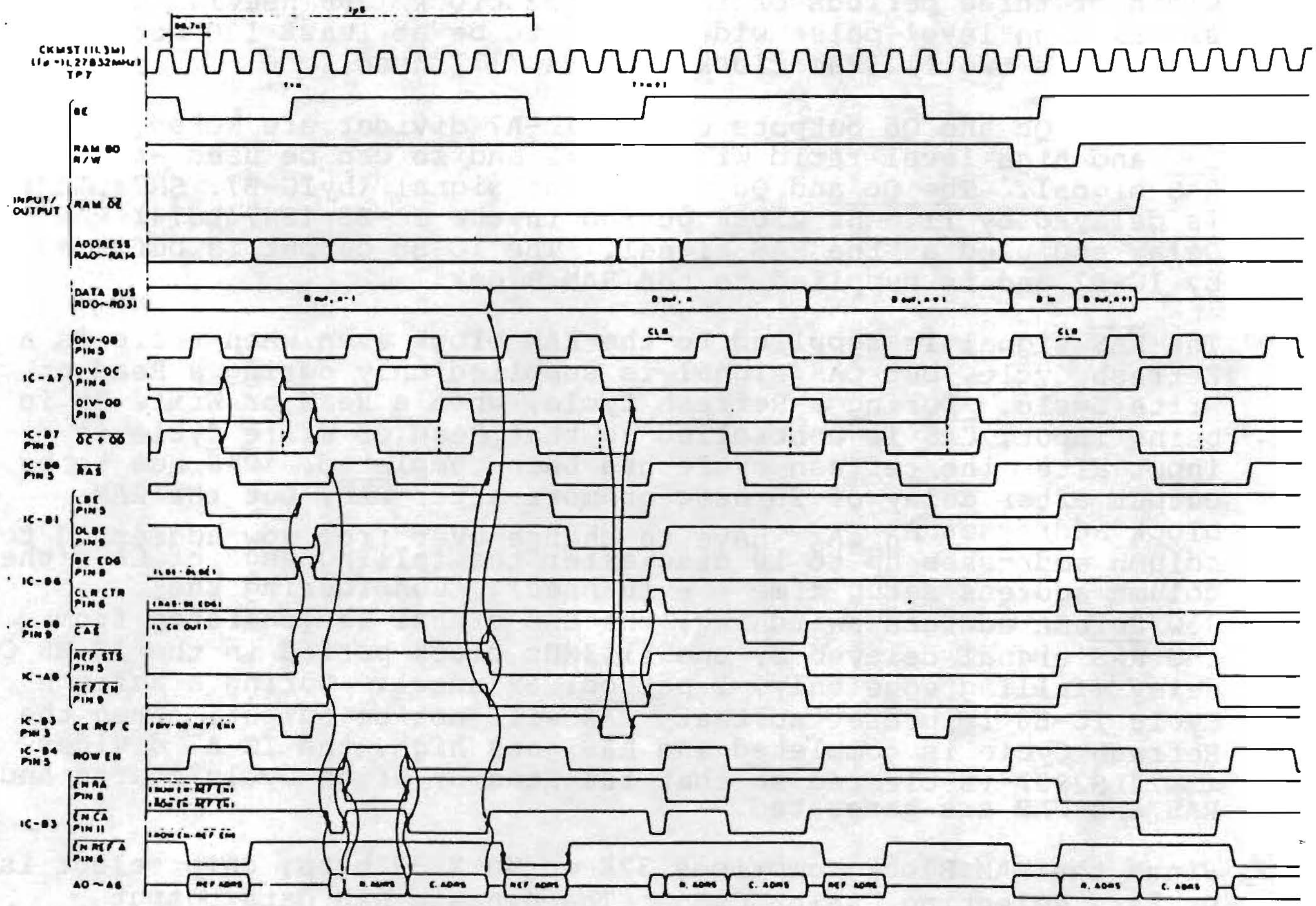


Figure 7-50 RAS/CAS Timing Diagram

7.9.3.4 Control Pulse Generator

This block is configured as follows (refer to Figure 2-4-9).

(a) Be Delay (IC-B1:SN74LS74) -> delays the BE signal and is used to detect the rising edge. CKMST (11.3MHz) or 11.3MHz is used for the Delay Clock.

(b) Control Pulse Gate (IC-B6: SN74LS00) -> generates the CLRCTR (Clear Counter) pulse to clear the divider and BE rising edge pulse (on the delayed BE signal formed in the BE Delay Block)

(c) Chip Select Flip-flop (IC-B4: SN74LS74) -> selects the 2 16K-bit RAM chips from which the 32 bit word is comprised using address RA_{14}.

(d) Address Select Flip-flop (IC-B4: SN74LS74) -> selects the RAM Row/Column address and forms ROWEN (Row Enable) on the delayed $\overline{RAS}$ by CKMST (11.3MHz).

(e) Refresh Controller (IC-A8: SN74LS74; IC-B6: SN74LS08; IC-B3: SN741S00) -> forms the Refresh Counter clock ($\overline{CKREFC}$) and Refresh Enable (REFEN) in order to repeat Refresh Cycle except in Read or Write Cycle.

(f) Data Bus Control Gate (IC-B5: SN74LS00) -> forms the control signal to control the Output Enable of the Output Data Buffer so that the Data bus (RD_0-RD_{31}) is in the output mode when either RAM $\overline{OE}$ is high or when RAM BD R/W is low.

Row, Column or Refresh address control and the Refresh Cycle or Read/Write Cycle occur through the processes (a) - (f) above, and the Latch Clock of Data Output Latch/Buffer and Output Enable are formed.

7.9.3.5 Row/Column Address Latch

RA_0 - RA_{14} address are input to the memory board but at the RAM Block the 7 address bits A_0 - A_6 have to be separated into Row/Column addresses. So the rising edge of BE latches RA_0 - RA_6 as Column addresses and RA_7 - RA_{13} as Row addresses by means of IC-A1 and IC-A2. Address Output is controlled by the ENRA_and ENCA signals. At the IC-A1 and IC-A2 8D inputs, RAM BD R/$\overline{W}$ is input and latched as the RAM Block WRITE signal.

7.9.3.6 Refresh Counter/Refresh Address Buffer

IC-A4 and IC-A5 (SN74LS293) generate the Refresh Address for Row address refreshing. The Refresh Counter clock is generated at the Control Pulse Generator.

The address generated at the Refresh Counter, by means of the Refresh Address Buffer (IC-A3: SN74LS373) controls the output of the RAM Block Address A_0 - A_6.

(3) DATA INPUT/OUTPUT LATCH/BUFFER

On a memory board Write Cycle, data is latched on the rising edge of BE and supplied to the RAM Block. On a Read Cycle, the RAM Block data output is latched by the Output Latch/Buffer. The Data Input/Output Latch/Buffer (shown in Figure 7-51) comprises IC-C1 - IC-C8 and uses SN74LS374s. The RAM Block's Data output is latched in the Output Latch/Buffer by LCKOUT (Output Latch). The rising edge of LCKOUT is same timing as that of CAS. Output enable of the Output Latch/Buffer is controlled by means of RAM OE and RAM BD $R/\overline{W}$ so that the Data bus RD_0 - RD_{31} can be used bidirectionally.

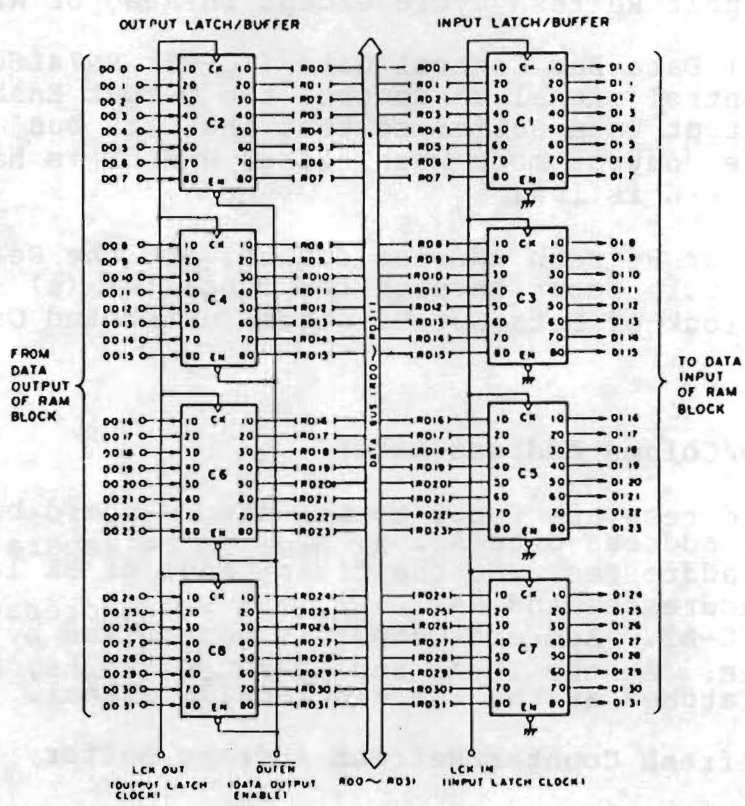


Figure 7-51 Data input/output latch/buffer

7.9.4 CHECK CIRCUIT

The Check circuit is for checking the Data bus and has no connection with actual edit operation. Only brief details of the circuit are given here.

The circuit shown in Figure 2-4-12 comprises: a Data Generator which outputs 32 bits of all 0s or 1s to the Data bus; a Comparator that compares every four bits of input data (IC-A10, A11, B10, B11, C10, C11, D10, D11); an Indicator circuit to indicate if it is exactly the same or not (IC-K11); an Error Latch circuit (IC-F10, F9); a Check Switch Latch circuit (IC-K9) and a Check Mode Encoder (IC-J10).

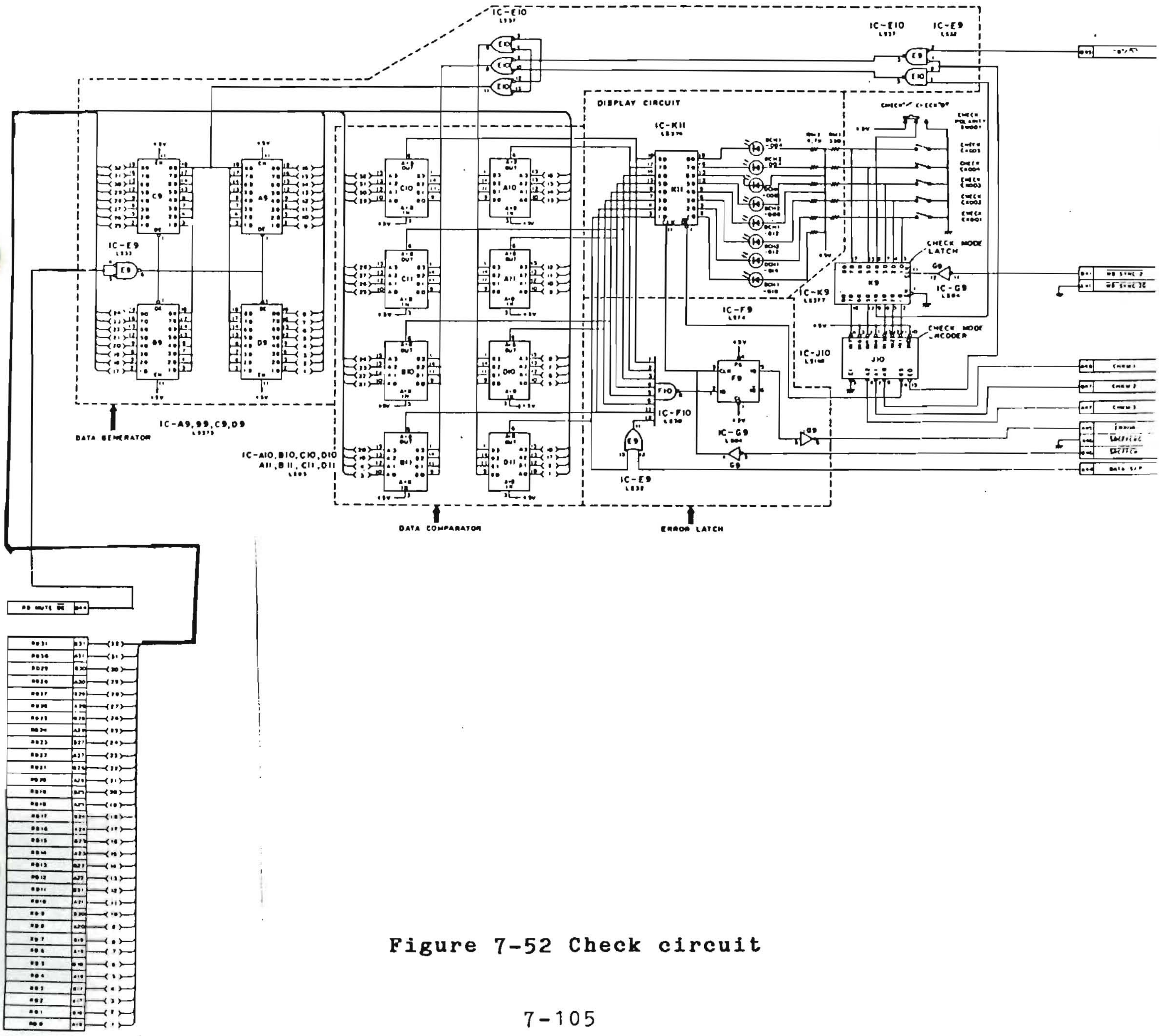


Figure 7-52 Check circuit

7.10. EDITING CONTROL CIRCUIT (EDT BOARD)

7.10.1 General

The **DAE-1100** can perform the CROSS-FADE at the editing point at the time of the PREVIEW an the AUTO-EDIT, and take off the unnaturalness of the editing point. Moreover, it has the features that the editing point can be freely selected even for using a VTR available to the editing only per the FRAME, and that the data recording on the tape actually can listen with the monitor sound.

To carry out these poerations, the EDT board is used with 4 dividing the MEMORY of the MEM board, and the control of those ADDRESSES is made.

The functions of the RAM divided to 4 portions:

7.10.1.1 REC RAM

This is used for listening to the FADE-OUT DATA of the cross FADE and to the monitor continuously.

7.10.1.2 SYNC RAM

This is used for synchronizing the editing point.

7.10.1.3 D/A RAM

This is used for delaying the MONITOR DATA taken out to the D/A OUT.

7.10.1.4 PB RAM

This is used for preventing the generation of MUTING when the VIDIO signal is switched.

The VIDEO SELECTOR is on the EDT board and the VIDEO signal selected due to the KEY BOARD is given as the output to the PCM processor.

The time code signal supplied to the TLC board is sent to the EDT board from the VTR, and to the TLC board after the conversion into the TTL level. On the contrary, the output of the TIME CODE GENERATOR is sent from the TLC board, and is supplied to the VTR as the output after the adjustment to the specified level.

7.10.2 Fundamental Operation of EDITOR

The **DAE-1100** uses one PCM processor and two VTRs (one is for a PLAYER and the other is for a RECODER), and decides FADE IN POINT by the PLAYER and FADE OUT POINT by the RECODER, in addition, as it performs the CROSS FADE due to IN POINT and OUT POINT, the editing is carried out by recording the signals of the RECODER and the PLAYER on the RECORDER TAPE.

The above-mentioned operation is shown in Figure 7-53.

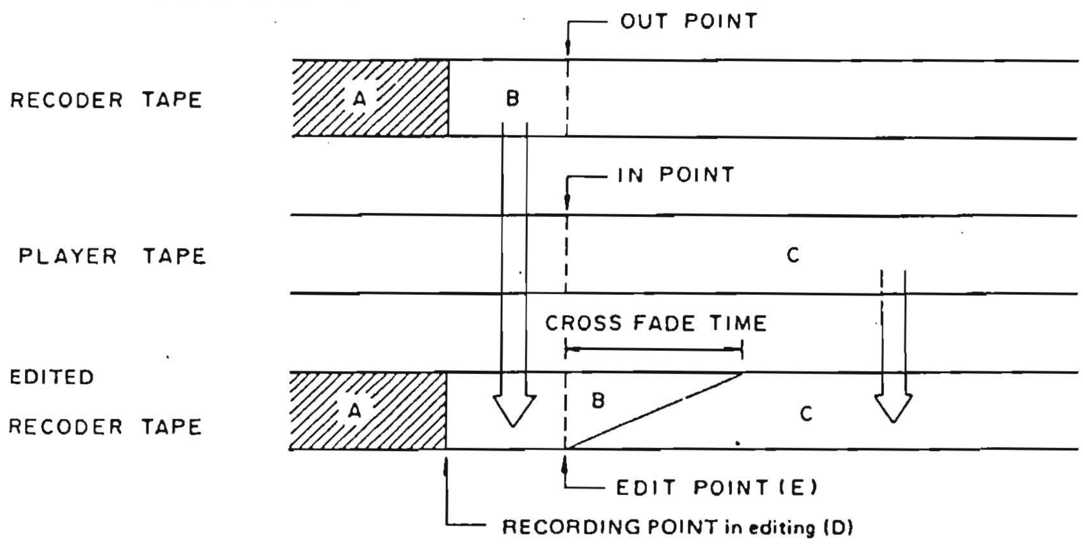


Figure 7-53 EDIT IN/OUT and Crossfade Time

A is the DATA recorded already to the RECODER TAPE.

B is the same DATA as A, but it is the DATA to be rerecorded again in case of the editing.

C is the DATA recorded to the PLAYER TAPE, but it is the DATA to be rerecorded to the RECODER TAPE in case of the editing.

D point is the point necessary for using the VTR available to the editing only per the FRAME, and is selected at the beginning of the FRAME in which the EDIT POINT is included.

E point is the EDIT POINT, and the CROSS FADE begins from this point.

Note: The DATA recorded actually to the TAPE is, of course, encoded by the PCM processor, therefore it cannot be distinguished clearly on the TAPE like this.

First of all, the following is the DATA DELAY of the PCM processor.

The PCM processor provides the correction code of the ERROR to prevent the DATA ERROR due to the DROP-OUT of TAPE and so on, and the DELAY of the DATA occurs due to the ENCODER and DECODER to correct the ERROR. This DELAY time shows a different value as per the coding method.

When the VIDEO OUTPUT and VIDEO INPUT of the PCM processor are connected, the DATA DELAY occurs to the ENCODER INPUT and the DECODER OUTPUT.

In case this state regards the DECODER OUT signal as the reference, it is shown in Figure 7-54.

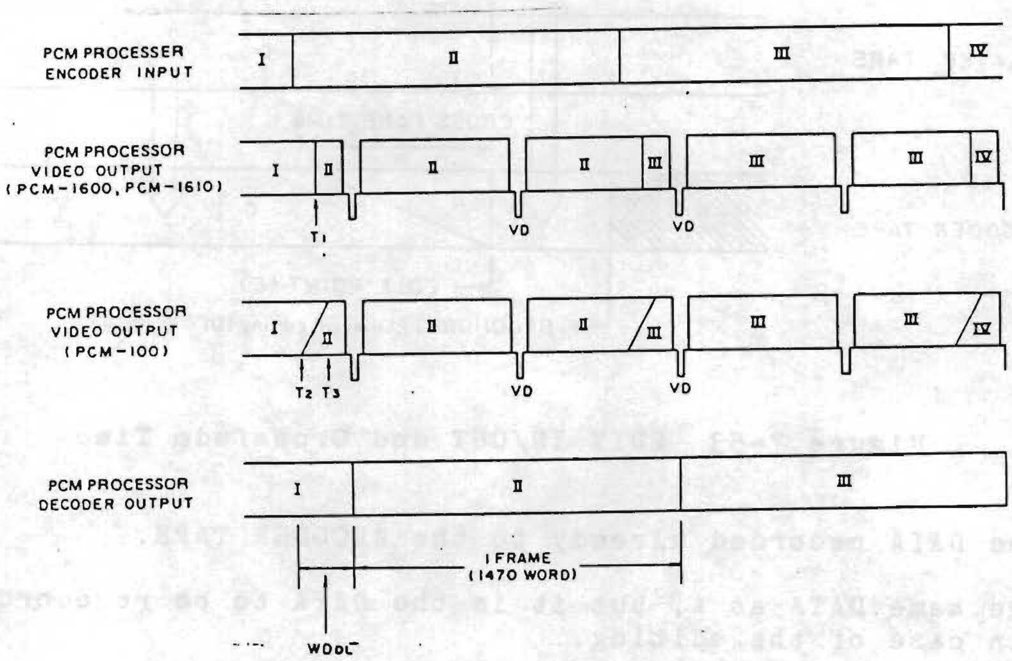


Figure 7-54 Data delay

In this figure, since the codes of the **PCM-1600**, **PCM-1610**, and **PCM-100** are different, the DELAY time, WD_{DL} is also different, and if the **PCM-1600** and **PCM-1610** select a certain appropriate time T_1, it is possible to distinguish the DATA on the VIDEO signal as follows: the front from the T_1 indicates the DATA of I and the rear from the T_1 shows the DATA of II. However, even though the **PCM-100** selects an appropriate time, you should give attention to that there is the section during which the DATA of I and II are mixed as the interval from T_2 to T_3.

The EDIT POINT (the OUT POINT of RECODER or the IN POINT of PLAYER) is decided due to listening to the reproduced sound which converted the digital output given from the DECODER into the analog signal. (This EDIT POINT can, of course, decide further accurate POINT due to the SEARCH MODE, but it is its reference that is the EDIT POINT decided here.)

The EDIT POINT is given by the FRAME of TIME CODE recorded on the TAPE, and by the WORD COUNTOR counting the WORD in the FRAME.

In the meantime, return to the Figure 7-53 and refer to the DATA B, the B memorizes previously the DECODER OUT signal rather than the FRAME including the OUT POINT to the RAM and, by reading from the RAM earlier by WD_{DL} than the TIMING written to the RAM in editing, inputing to the ENCODER INPUT and recording a sound from the OUT POINT FRAME, it can record again the same thing as the DATA recorded on the TAPE. This RAM is called the REC RAM.

With respect to the DATA C of the PLAYER, when seen at the ENCODER INPUT, the IN POINT has to correspond to the OUTPOINT.

You have only to adjust the phase of the VTR in order to make the FRAME fit, and moreover, to delay the DATA C by using the RAM for the purpose of fitting the WORD.

Thus, since there are some dispersions to the VTR, it is difficult to adjust the phase of the VTR till the FRAME in a short time, therefore the adjusting phase is allowable up to ± 1 FRAME and the other is delayed by using the RAM. This RAM is called SYNC RAM.

This editing system uses only one PCM processor, for this reason, it has to switch over the input to the VIDEO INPUT of the PCM processor from the VIDEO OUT of the RECODER VTR to the VIDEO OUT of the PLAYER VTR in the editing.

Furthermore, at that time, there are the following differences about the **PCM-1600**, **PCM-1610**, **PCM-1630** and **PCM-100**.

As the **PCM-1600** and **PCM-1610** and **PCM-1610** use a code completed at the BLOCK (35H), if the phases of two VTRs are fitted, the code error does not occur in case of the changeover by the FRAME.

Figure 7-55 shows the codes of the **PCM-1600**, **PCM-1610** and **PCM-1630**.

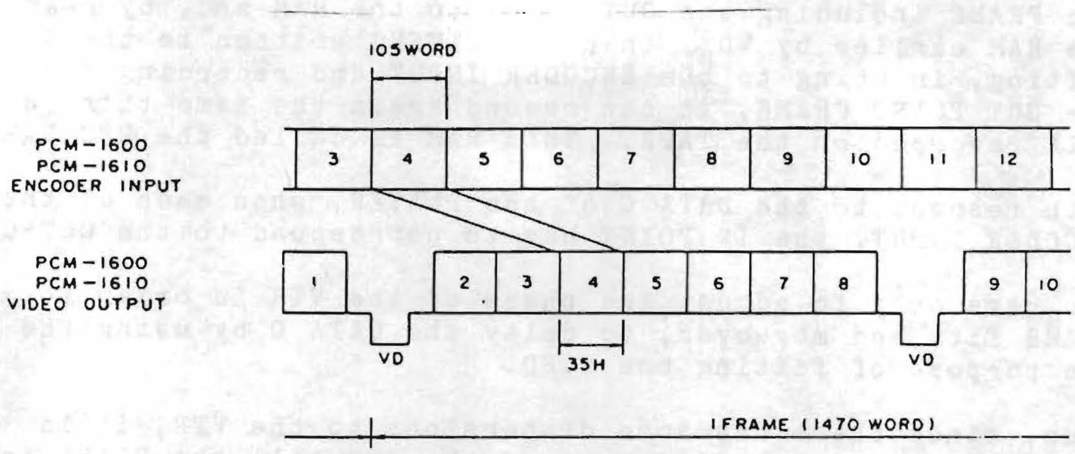


Figure 7-55 Encode input/video output (PCM-1600, PCM-1610)

On one hand, as the **PCM-100** conforms to the format of EIAJ (Electronic Industries Association of Japan), the data are not completed by the FRAME, therefore, when the VIDEO signal is switched over by the FRAME, the code error occurs.

The code of the **PCM-100** is shown in Figure 7-56.

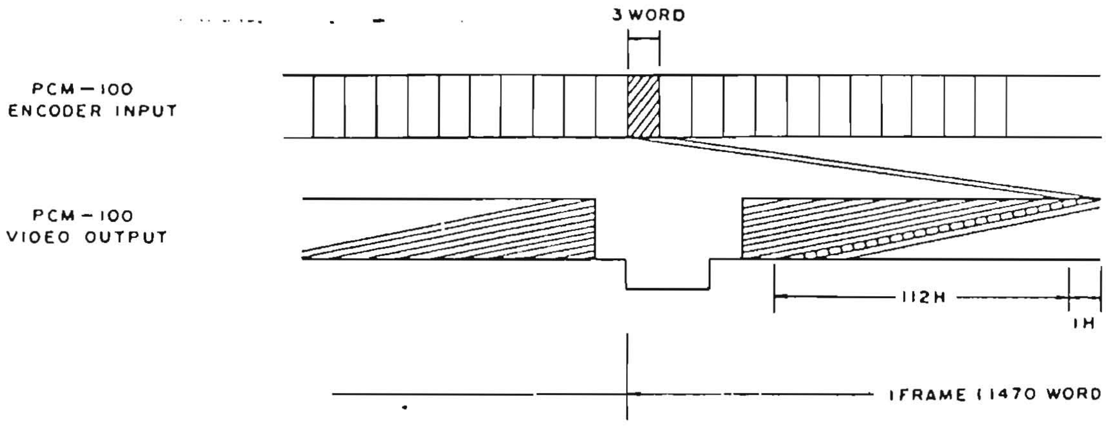


Figure 7-56 Encode input/video output (PCM-100)

In the **PCM-100**, for this code error, as there is a possibility to produce a different sound after having made an erring correction during the interval of 112H (336 WORD), the MUTING is performed.

Figure 7-57 shows the difference of the DECODER OUTPUT for the **PCM-100**, **PCM-1600**, **PCM-1610** and **PCM-1630** when the signal of the input VIDEO is switched over by the FRAME.

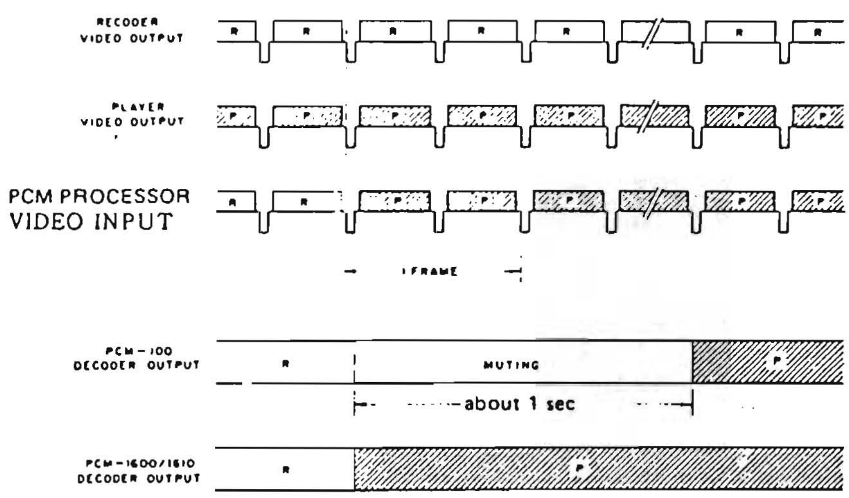


Figure 7-57 Differences of the DECODER OUTPUT for each model

When this MUTING occurs, the output of the DECODER OUTPUT is sent out "0" for about one second, accordingly, in order to listen to a continuous monitor sound, it is necessary to write into the MEMORY previously during its section. For this purpose, the MEMORY capacity needs about 1.4×10^6 bits, and is not practical, therefore a certain circuit is required to prevent the generation of the MUTING.

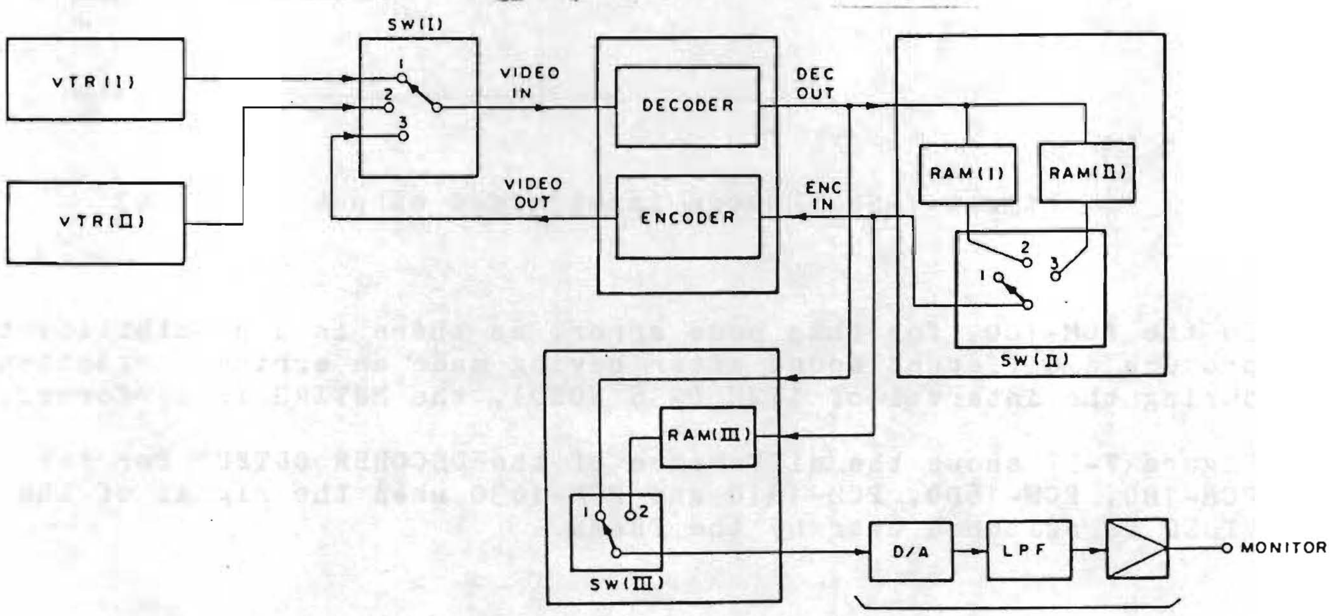


Figure 7-58 Basic circuit of EDITOR

Thus, the circuit like Figure 7-58 is considered. SW(I) is the SWITCHER of the VIDEO signal, and is inputed to the PCM processor by switching over the VIDEO OUT of the VTRs(I), (II) and the PCM processor.

SW(II) is the SWITCHER of the DIGITAL signal, and is inputed to the ENCODER INPUT of the PCM processor by switching over the OUTPUT of RAMs(I) and (II).

The RAM(I) is the RAM to make the MEMORY of the DATA for the VTR(I), and the RAM(II), for the VTR(II), in addition, the RAM(III) is the RAM to delay the portion of the DATA DELAY by (WD_{DL}) for the PCM processor.

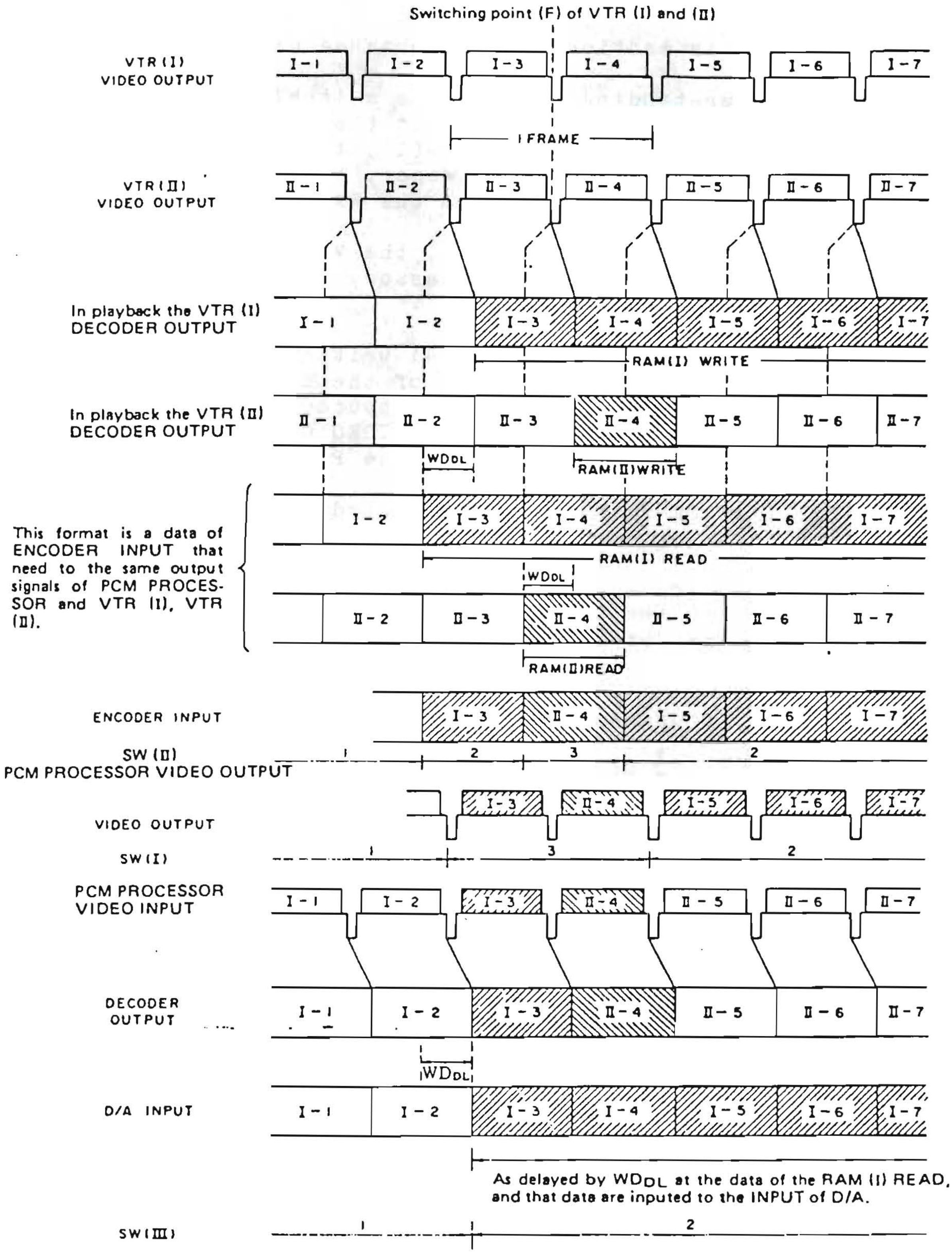


Figure 7-59 Timing chart of Figure 7-58

The explanation is mentioned in accordance with Figure 7-59.

To help the understanding easily, the switching point of the INPUT assumes (F) that is situated at the middle of the FRAME. At first, (1) is selected in the SW(I), the VIDEO OUT of the VTR(I) is inputed to the PCM processor, and then the DECODER OUT (later than I-3) is written to the RAM(I).

Next, (2) is selected in the SW(I), the VIDEO OUT of the VTR(II) is inputed to the PCM processor, and then, the DECODER OUT(II-4) is written to the RAM(II).

The DATA (later than I-3) and (II-4) written previously are read early for by WD_{DL}, Delay time of the processor from the TIMING written respectively, and is inputed to the ENCODER INPUT, thus, the same output as the VIDEO OUT of the VTR is made the output to the VIDEO OUT of the PCM processor.

When (I-3) is being read, (2) is selected in the SW(II), and when (II-4) is being read, (3) is selected in the SW(II).

In addition, (3) and (2) thereafter are selected to SW(I) for 1 FRAME during which the DATA of, at first (1), next (I-3), and (I-4) are made the output to the VIDEO OUT of the PCM processor.

Thus, by such a process, the VIDEO OUT signal of the VTR(I) against before (I-2), the VIDEO OUT signal of the PCM processor similar to the VIDEO OUT of the VTR(II) against (I-3), the VIDEO OUT signal of the PCM processor similar to the VIDEO OUT of the VTR(II) against (II-4) and the VIDEO OUT of the VTR(II) against later than (II-5) are inputed to the VIDEO INPUT of the PCM processor.

Therefore, as shown in this example, in the case the time when (2) and (3) are selected against the SW(II) is more than 336 WORD (or 112H), as the code error does not occur between (I-2) and (I-3), (I-3) and (II-4), and (II-4) and (II-5), the input of the PCM processor can switch over from the VIDEO OUT of the VTR(I) to the VIDEO OUT of the VTR(II) without the generation of the MUTING.

And after the DECODER OUT signal of the VTR(II) without generating the MUTING obtained from the aforementioned process has been adjusted the phase by the SYNC RAM, the CROSS FADE is done as the DATA of the FADE IN.

The monitor sound converted into analog from digital, even if the input of the PCM processor is switched over, has to be listened as the sound of VTR(II) until the monitor sound is made the CROSS FADE, accordingly, the SW(III) switches over from (1) and (2) before the input is switched over, and the monitor sound is obtained by switching over the READ OUT DATA of the RAM(I) from the DECODER OUT DATA to the DATA delayed for WD_{DL} only due to the RAM(III).

The RAM(I) used here is called REC RAM, the RAM(II), PB RAM, and the RAM(III), D/A RAM.

This REC RAM also is the RAM that memorizes the DATA B of Figure 7-10-1.

As mentioned above, this editing system requires 4 RAMs as follows:

1) REC RAM
2) D/A RAM
3) PB RAM
4) SYNC RAM

The following shows how these RAMs are used concretely.

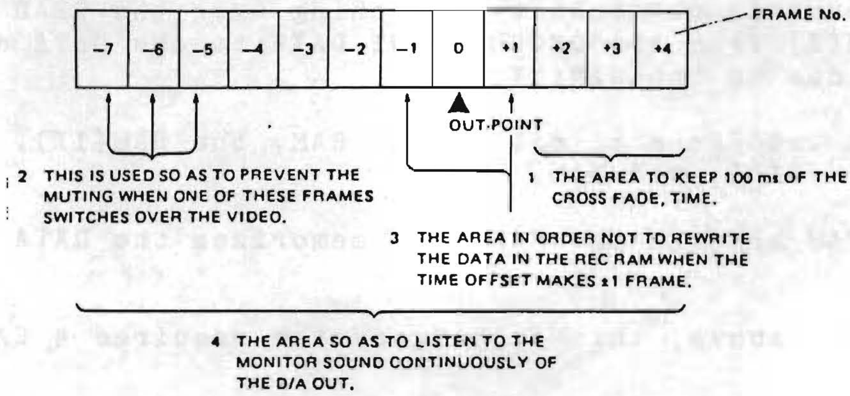
As the MEMORY of the **DAE-1100** uses the MEM board of 32 bits x 32K, this is utilized as 4 RAMs with four dividing as listed in Table 7-10-1.

Table 7-10-1 RAM Addressing

ADDRESS / AREA	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	FRAME No. (TOTAL 22.3 FRAME)
REC RAM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	12.02
	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	(17665 WD)
D/A RAM	1	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0.52
	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	(767 WD)
PB RAM	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1.74
	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	(2560 WD)
SYNC RAM	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	8.01
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	(11776 WD)

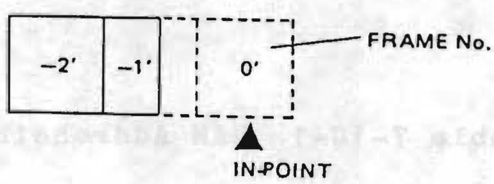
The REC RAM is the RAM providing the capacity of 12 FRAMES.

These 12 FRAMES are as below.



The D/A RAM is the RAM providing the capacity of 767 WORDS, and is employed so as to listen as the monitor sound of the D/A OUT due to delaying the outputs of the REC RAM and SYNC RAM for by the DELAY of the PCM processor.

The PB RAM is the RAM providing the capacity of 1.74 FRAME, and is employed in order not to generate the MUTING when the input VIDEO signal of the PCM processor in case of the PREVIEW or the AUTO-EDIT has switched over from the RECODER to the PLAYER.



The SYNC RAM is the RAM providing the capacity of 8 FRAMES.

First of all, the VTR adjusts the phase of the PLAYER so as to fit the FRAME(0') of the IN-POINT to (-4) before 4 FRAMES OF OUT-POINT and when the (0') has been fitted to the FRAMES of (-3), (-4) and (-5), the adjustment of the phase by the PLAYER is over. Consequently, since then, the phase is adjusted by the SYNC RAM.

The reason why (0') fits (-4) here is to obtain so margin as to delay at the SYNC RAM when the dispersion caused by adjusting the phase of the VTR is maximum, namely, even in case of (0') and (-3).

actually pressed POINT are employed.

Now, where the OUT-POINT is 0' FRAME WD_{OP} WORD, and where the IN-POINT is 0' FRAME WD_{IP} WORD, when the adjusting phases of the VTR are (0') and (-4).

The SYNC WD which is the delayed portion of the SYNC RAM is as follows.

$$\text{SYNC WD} = 4\ \text{FRAME} + WD_{OP} - WD_{IP} - WD_{DL}$$

$$= 5880 + WD_{OP} - WD_{IP} - WD_{DL}\ \text{(WORD)}$$

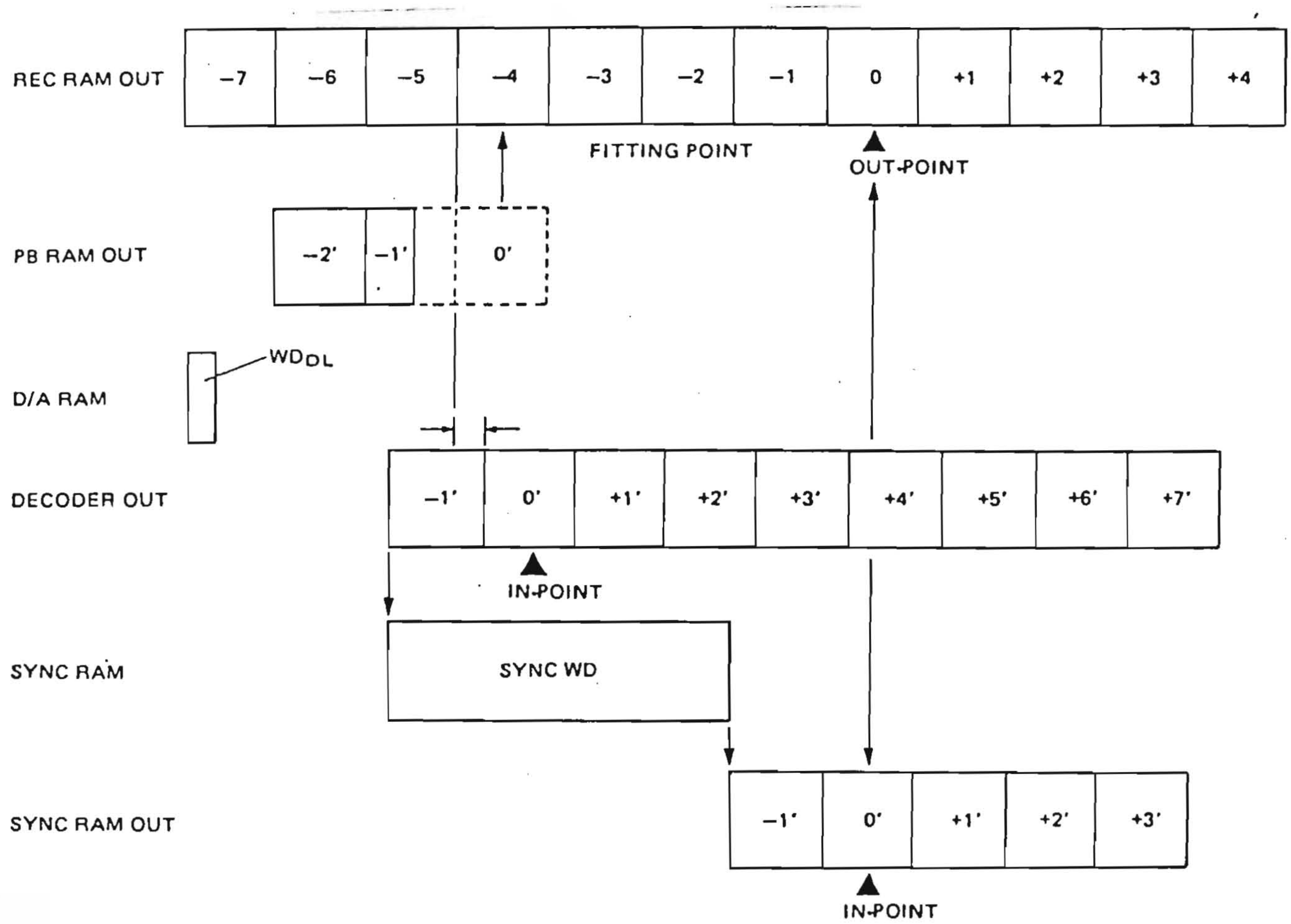
The SYNC WD becomes maximum when the phase of the VTR is adjusted to (0') and (-5), when the OUT-POINT is made +1 FRAME TIME OFFSET, and when the IN-POINT is made -1 FRAME TIME OFFSET, and $WD_{OP} = 1469$, $WD_{IP} = 0$.

In case of these phases,

$$\text{SYNC WD (MAX)} = 7 \times 1470 + 1469 - 0 - WD_{DL}$$

$$= 8\ \text{FRAME} - 1 - WD_{DL} < 8\ \text{FRAME}$$

Therefore, 8 frames are quite enough for the AREA of the SYNC RAM.



Figures 7-60 and 7-61 show the flowchart of the data in editing on the VTR, the PCM processor and the **DAE-1100**.

PCM PROCESSOR

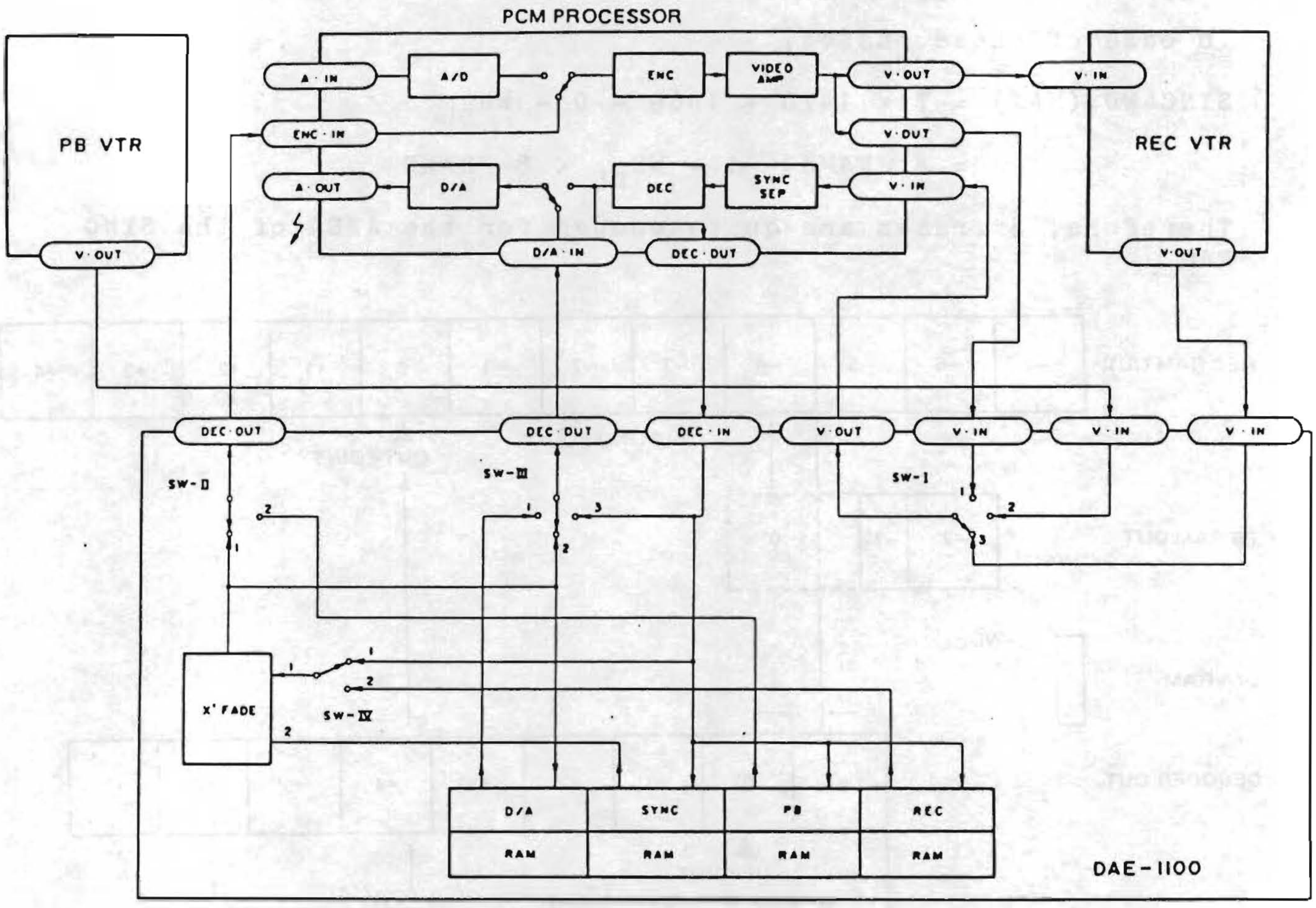


Figure 7-60 The flowchart of the data in editing

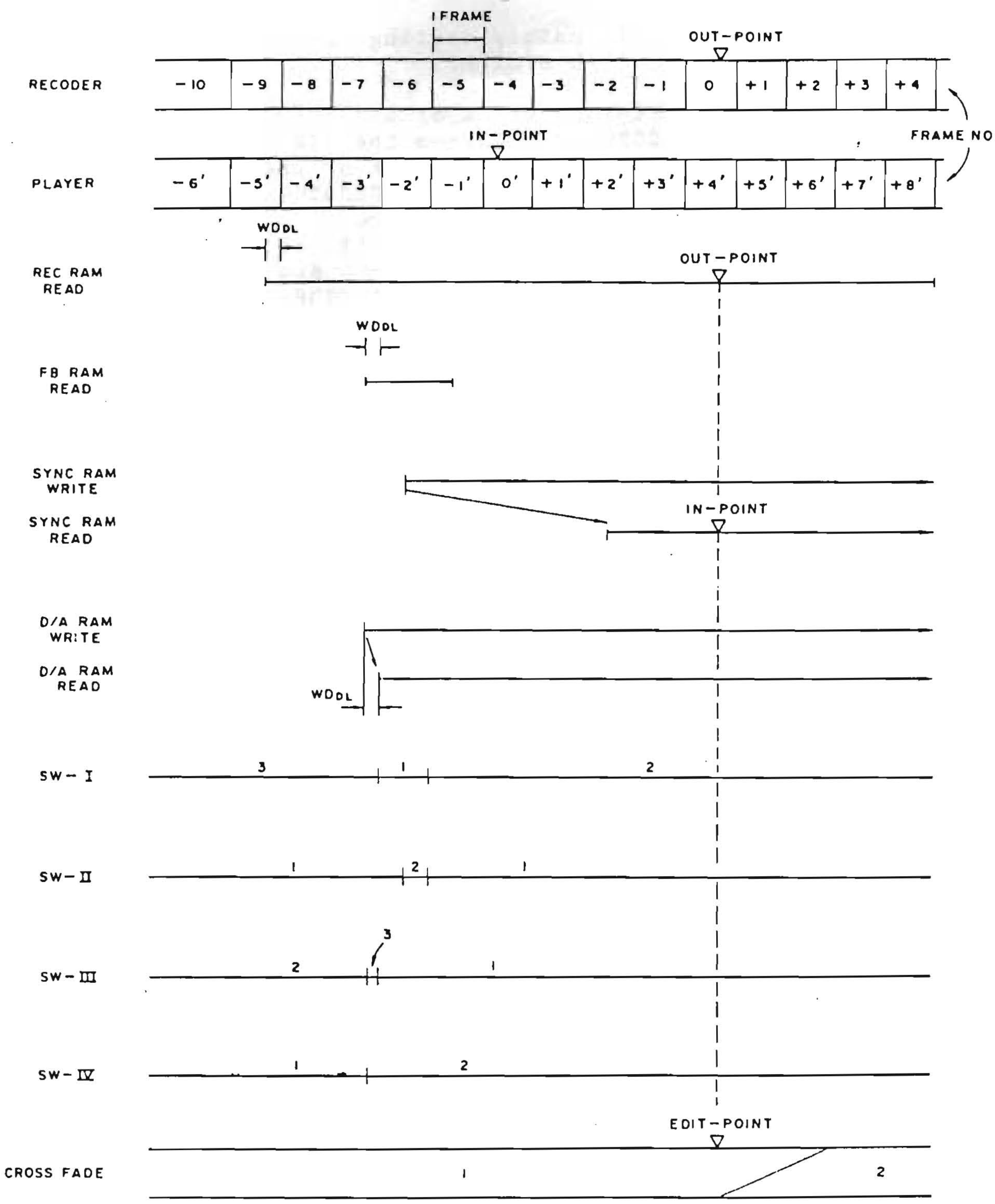


Figure 7-61 The timing chart of the data editing

7.10.3. Composition

The EDT board is mainly distinguished to 2 systems of the ANALOG and DIGITAL SYSTEMS.

The ANALOG system consists of the COMPARATOR (1) sending out the TIME CODE signal from the VTR 3 set to the TLC board processed to the TIME CODE of the TTL LEVEL, the OUTPUT BUFFER (2) giving the GENERATOR DATA of the TTL LEVEL received from the TLC board to the output of the RECODER VTR, the VIDEO SELECTOR (3) so as to select the VIDEO OUT signal of the VTR 3 sets and PCM processor, VIDEO AMP (4) giving the output as the VIDEO OUTPUT due to fitting the levels of the outputs of the VIDEO SELECTOR and PCM processor, and the FRAME SEPARATOR (5) deriving the FRAME signal from the VIDEO OUT of the PCM processor.

In the meantime, The Digital system consists of the REC RAM ADDRESS COUNTER (8) controlling the ADDRESS OF 4 RAMs, the D/A RAM ADDRESS COUNTER (9), PB RAM ADDRESS COUNTER (10), SYNC RAM ADDRESS COUNTER (11), 1470-DELAY WORD COUNTER (7) necessary for reading early the REC RAM and PB RAM by WD_{DL}, the EDIT POINT WORD COUNTER (12) serving also as the CROSS FADE START WORD COUNTER, the EDIT TIMING CONTROLLER (6) controlling these COUNTERS, and the EDIT MODE CONTROLLER (13) arranging the EDIT MODE of the FRAME unit sent from the SYS board, to the MODE of the WORD unit.

The BLOCK DIAGRAM is shown in the Figure 7-62.

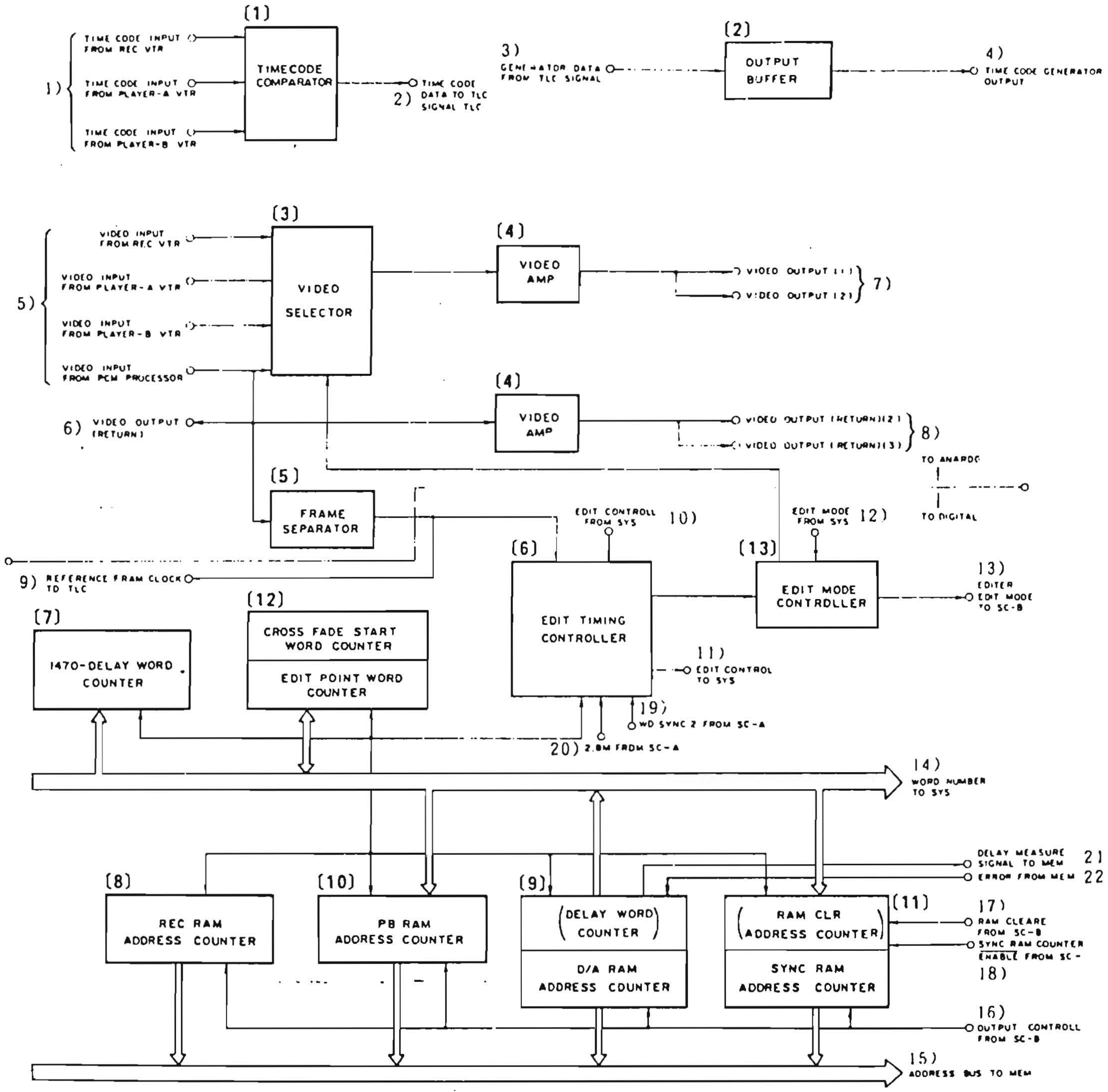


Figure 7-62 EDT Board Block Diagram

7.10.4. Explanation of Circuit

7.10.4 INPUT AND OUTPUT SIGNAL

1. TIME CODE INPUT from VTR

The input signal of the TIME CODE sent from the VTR:

TC1: BALANCE TIME CODE INPUT; HOT
TC2: BALANCE TIME CODE INPUT: COLD
TC3: UNBALANCE TIME CODE INPUT
REC TC: TIME CODE from RECODER VTR
PLA TC: TIME CODE from PLAYER-A VTR
PLB TC: TIME CODE from PLAYER-B VTR

2. TIME CODE SIGNAL (TCDT1, TCDST2, TCDT3) to TLC board

3. GENERATOR SIGNAL (TCGN) from TLC board

The TIME CODE signal of TTL LEVEL:
TCDT1: The TIME CODE signal of RECODER VTR
TCDT2: The TIME CODE signal of PLAYER-A VTR
TCDT3: The TIME CODE signal of PLAYER-B VTR
TCGN: The TIME CODE GENERATOR signal

4. TIME CODE GENERATOR OUTPUT (TC1, TC2, TC3)

The output of the TIME CODE GENERATOR of the ANALOG LEVEL:

TC1: BALANCE TIME CODE GENERATOR OUTPUT; HOT
TC2: BALANCE TIME CODE GENERATOR OUTPUT; COLD
TC3: UNBALANCE TIME CODE GENERATOR OUTPUT

The output LEVEL is about 2-2Vp-p.

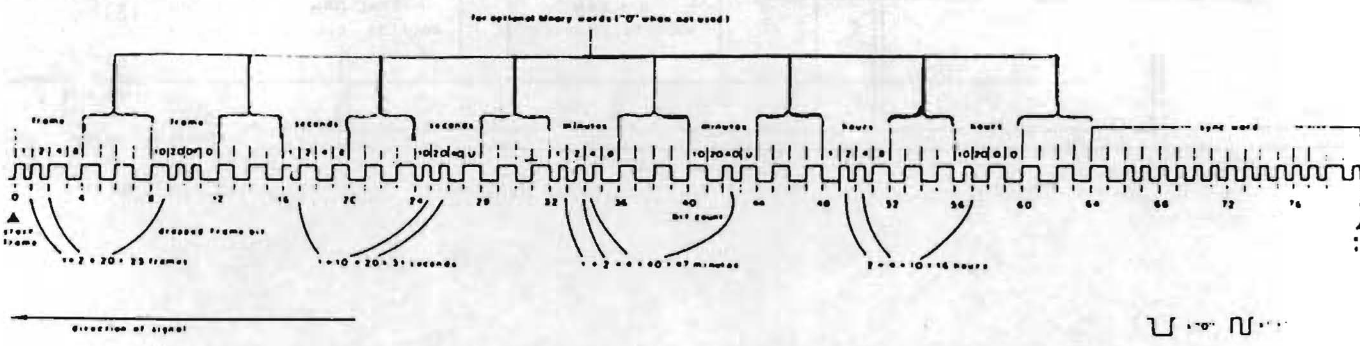


Figure 7-63 Standard SMPTE time code (1 frame)

5. **VIDEO INPUT from VTR and PCM processor (VIDEO IN (1), VIDEO IN (2), VIDEO IN (3), and VIDEO IN (4))**

VIDEO IN (1): The VIDEO signal from PCM processor.
VIDEO IN (2): The VIDEO signal from REDODER VTR
VIDEO IN (3): The VIDEO signal from PLAYER-A VTR
VIDEO IN (4): The VIDEO signal from PLAYER-B VTR

6. **VIDEO OUTPUT (RETURN) (VIDEO IN (1))**

The signal of theis VIDEO OUT (RETURN) is the VIDEO OUT signal connected to the VIDEO IN (1) directly and the VIDEO signal can be obtained in parallel when 75 resistor of the rear panel is turned OFF.

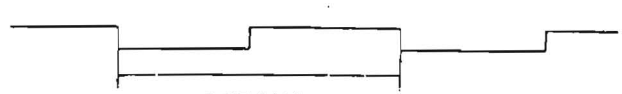
7. **VIDEO OUT (1), VIDEO OUT (2)**

This is the VIDEO OUT signal given to the output through the VIDEO AMP after one in the VIDEO OUT signals of the PCM processor and 3 set VTRs is selected.

8. **VIDEO OUTPUT (RETURN) (2), VIDEO OUTPUT (RETURN) (3)**

The VIDEO OUT signal of the PCM processor is the VIDEO OUT signal supplied to the output through the internal VIDEO AMP.

9. **REFERENCE FRAME CLOCK (RFCK) to TLC board**



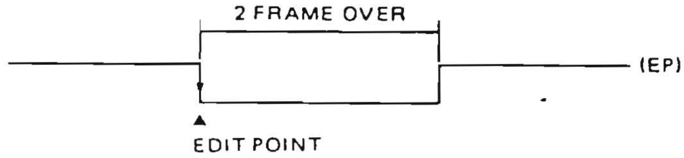
1 FRAME

10. **EDIT CONTROL from SYS board**

This is necessary signal so that the EDIT board may make the editing operation (PREVIEW, AUTO-EDIT).

EDIT POINT SIGNAL (EP)

This is the signal sent from the SYS board when the EDIT POINT (OUT POINT, IN POINT) IS PRESSED.
This signal becomes "L" when the EDIT POINT is pressed, and the "L" during 2 FRAMES at least is arranged so as to continue.



. **RAM READ START (RARST)**

This signal is the CLOCK which latchs the $\overline{1470 - WD}_{DL}$ to the FLIP FLOP of the (1470 - DELAY WORD) COUNTER circuit.

. **CROSS FADE FRAME ($\overline{\text{X'FDFM}}$)**

This is the signal supplied to the FRAME before one position doing the CROSS FADE and this signal latch the X FD ST WD, in relation to what word position of the next FRAME the CROSS FADE starts from, to the FLIP FLOP of the CROSS FADE START WORD COUNTER circuit.

. **DELAY MEASURE FRAME ($\overline{\text{DLMFM}}$)**

The EDT board gives the signal to measure the DELAY of the PCM processor to the MEM board by this signal.

. **PB RAM START TIMING (PB RAM)**

This is the signal to start the READ or the WRITE of the PB RAM. The signal is the READ when the DWFLAG is "H". On one hand, it is the WRITE when it is "L". The WRITE is sent before 3 FRAMES of the IN-POINT and the READ, before 4 FRAMES.

. **REC RAM START TIMING ($\overline{\text{REC RAM}}$)**

This is the signal to start the READ or the WRITE of the REC RAM. The signal is the READ when the DWFLAG is DWFLAG is "H" and it is the WRITE when it is "L". The WRITE is sent before 8 FRAMES of the out-POINT and the READ, before 9 FRAMES.

. **TRI-STATE REQUEST (TRST)**

This is the signal which is made "L" when the WD of the EDIT POINT and the DATA of the DELAY WD are sent from the EDT board to the SYS board.

The DATA of the DELAY WD when the DWFLAG is "H" or the WD DATA of the EDIT POINT when it is "L", are sent through the WORD NUMBER BUS.

- **DEMANDED WORD FLAG (DW FLAG)**

This signal is the FLAG which has the meaning due to combining REC RAM, PB RAM and TRST.

	DW FLAG "L"	DW FLAG "H"
$\overline{\text{REC RAM}}$	REC RAM WRITE	REC RAM READ
$\overline{\text{PB RAM}}$	PB RAM WRITE	PB RAM READ
$\overline{\text{TRST}}$	EDIT POINT -- SYS board	DELAY WORD -- SYS board

11. EDIT CONTROL to SYS board

This is the CONTROL signal on the EDIT

- **CROSS FADE START ($\overline{\text{X'FDST}}$)**

This signal is the TIMING signal to start the CROSS FADE.

12. EDIT MODE from SYS board

This is th signal to show the state of the **DAE-1100.**

- **VIDEO SELECT SIGNAL (VS-A, VS-B)**

This si the signal to control the VIDEO OUT signal of the DAE-1100. One signal out of either the output signal of the VTR 3 sets or the VIDEO OUT signal of the PCM processor is selected bys this signal and the selected signal is supplied to the input signal of the PCM processor.

VS-B	VS-A	SELECTED VIDEO OUT SIGNAL
0	0	PCM PROCESSER
0	1	RECORDER VTR
1	0	PLAYER-A VTR
1	1	PLAYER-B VTR

- **EDITOR MODE SIGNAL (EDT MD O 3)**

This is the input signal to show the state of the **DAE-1100** as listed below.

MODE	EDTMD			
	3	2	1	0
RAM CLEAR	0	0	0	1
STRAIGHT	0	0	1	1
SEARCH	0	1	1	1
CHECK 1	0	1	1	0
CHECK 2	0	1	0	1
CHECK 3	0	1	0	0
CHECK 4	0	0	1	0
CHECK 5	0	0	0	0
MUTE OUTPUT	1	0	0	0
REC RAM WRITE	1	0	1	1
PB RAM WRITE	1	0	1	0
DELAY MEASURE	1	0	0	1
EDIT	1	1	1	1

. **RAM CLEAR MODE**

This is the MODE to write "0" to the RAM of the MEM board and this MODE is performed without fail when shifting from each MODE to the STRAIGHT MODE.

. **STRAIGHT MODE**

This is the MODE which makes each VTR go into operation, monitor the sound and decides the EDIT-POINT.

. **SEARCH MODE**

This MODE reproduces the DATA for 6 seconds stored into the MEMORY together with condensation in the MEM board by the MANUAL or the normal SPEED (X1) or the SPEED multiplied by one half (X 1/2), and it monitor the sound.

. **CHECK MODE (CHECK 1 5)**

This is the MODE to check the SYSTEM and operates by the SWITCH on the MEM board.

. **MUTE OUTPUT MODE**

This is the MODE not to give the sound to the monitor output.

. **REC RAM WRITE MODE**

This is the MODE which writes the DATA to the REC RAM of the MEM board.

. **PB RAM WRITE MODE**

This is the MODE which writes the DATA to the PB RAM of the MEM board.

. **DELAY MEASURE MODE**

This is the MODE which measures the DATA DELAY of the PCM processor.

. **EDIT MODE**

This MODE shows the state of EDIT. This MODE is DIVIDED to 4 MODES by the EDT board and these divided MODES are the signals of the FRAME unit.

13. EDITOR MODE (MS 0 - 3) to SC-B board

The EDT MD 0 - 3 as it is supplied to the output. (The signals of the FRAME unit)

The EDIT is supplied to the output with reforming 4 MODES. (The signals of the WORD unit)

MODE	MS				COMMENT
	3	2	1	0	
RAM CLEAR	0	0	0	1	
STRAIGHT	0	0	1	1	
SEARCH	0	1	1	1	
CHECK 1	0	1	1	0	
CHECK 2	0	1	0	1	
CHECK 3	0	1	0	0	The EDTMD 0 ~ 3 as it is supplied to the output. (The signals of the FRAME unit)
CHECK 4	0	0	1	0	
CHECK 5	0	0	0	0	
MUT OUTPUT	1	0	0	0	
REC RAM WRITE	1	0	1	1	
PB RAM WRITE	1	0	1	0	
DELAY MEASURE	1	0	0	1	
EDIT 1	1	1	1	1	
EDIT 2	1	1	1	0	The EDIT is supplied to the output with reforming 4 MODES. (The signals of the WORD unit)
EDIT 3	1	1	0	1	
EDIT 4	1	1	0	0	

The EDIT from 1 to 4 is the MODES controlling the state of the SW-I ~ IV

Table 7-10-2 Editor mode (MD0 - 3)

14. **WORD NUMBER BUS (EA 0 13) to SYS board**
These signals exchange the DATA between the EDT board and the SYS board.

TRST	$\overline{\text{REC RAM}}$	$\overline{\text{RARST}}$	$\overline{\text{CF FM}}$	$\overline{\text{DWFLAG}}$	$EA_0 \sim EA_{13}$	COMMENT
1	1	0	1	X	$\overline{\text{1470–WD}_{DL}}$	SYS board ↓ EDT board
1	0	1	1	1	$\overline{\text{SYNC WD}}$	
1	1	1	0	X	$\overline{\text{XFDSTWD}}$	
0	1	1	1	0	$\overline{\text{1470–WD}_{EP}}$	EDT board ↓ SYS board
0	1	1	1	1	$\overline{\text{WD}_{DL}}$	

15. **ADDRESS BUS (RA 0 14) to MEM board**

These are the ADDRESSES of REC RAM, D/A RAM, PB RAM and SYNC RAM of the MEM board.
Refer to the Table 7-10-1 on the allocation for the ADDRESS.

16. **ADDRESS OUTPUT CONTROL (REC RA $\overline{\text{OE}}$, D/A RA OE, PB RA $\overline{\text{OE}}$, SYNC RA OE from SC-B Board.**

These are the $\overline{\text{OUTPUT ENABLE}}$ signals of each MEMORY ADDRESS.

17. **RAM CLEAR ($\overline{\text{RAM CLR}}$) from SC-B board.**

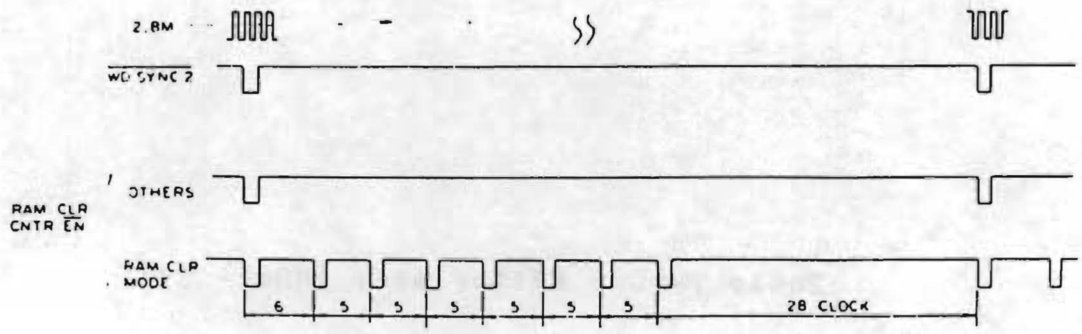
This is the signal which becomes "L" in the RAM CLEAR MODE.

18. **SYNC RAM COUNTER $\overline{\text{ENABLE}}$ (SYNC RAM CNTR $\overline{\text{EN}}$) from SC-B Board**

This signal is usually one piece per WORD similar to the WD-SYNC 2, but it is made 8 pieces per WORD in case of the RAM CLEAR MODE and is arranged to promote the RAM CLEAR ADDRESS COUNTER at 8 times the speed.

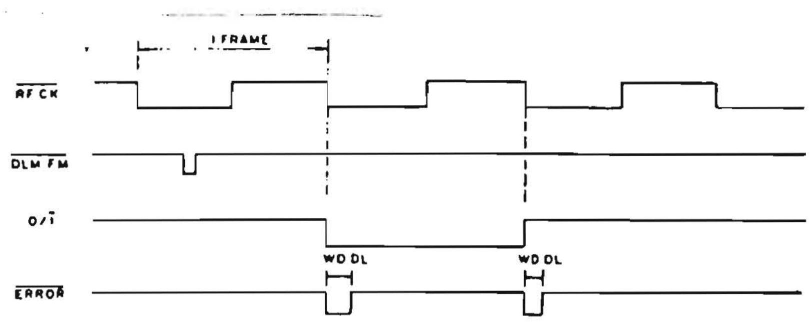
19. **$\overline{\text{WORD SYNC 2}}$ ($\overline{\text{WD SYNC 2}}$) from SC-A board.**
This is the WORD CLOCK.

20. **2.8M from SC-A board.**
This is the CLOCK of 2.8 MHz.



21. **DELAY MEASURE SIGNAL (0/1) to MEM board.**
This is the signal which gives the output to the MEM board to measure the DATA DELAY of the PCM processor and the output signal of "L" or "H" is supplied from the MEM board to the DATA BUSS on receiving this signal.

22. **ERROR SIGNAL ($\overline{\text{ERROR}}$) from MEM board.**
When the aforementioned 0/1 signal is supplied to the output, if the output given to the MEM board and the returned input are the same DATA, the signal becomes "H", on the contrary, if not, it becomes "L".



7.10.5 EACH BLOCK FUNCTION

1. **TIME CODE COMPARATOR**
The TIME CODE signal supplied from each VTR is amplified by a IC6, and its level is limited and is compared by a IC7. Furthermore, it becomes a TTL level and is supplied as the output to the TLC board. Refer to Figure 7-63.

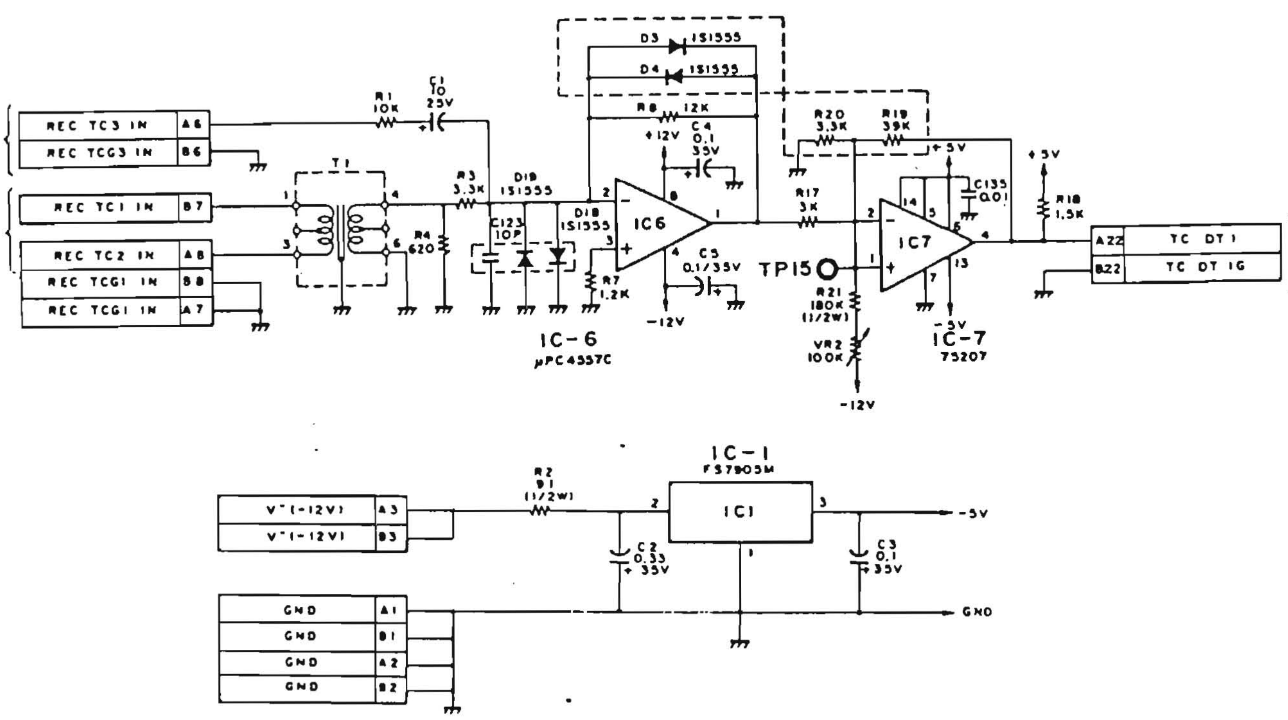


Figure 7-63 Time code comparator and power supply

2. GENERATOR OUTPUT BUFFER

The TIME CODE GENERATOR DATA of the TTL LEVEL supplied from the TLC board are adjusted to 2.2 Vp-p of the specified level, being supplied to the output.

Refer to Figure 7-64.

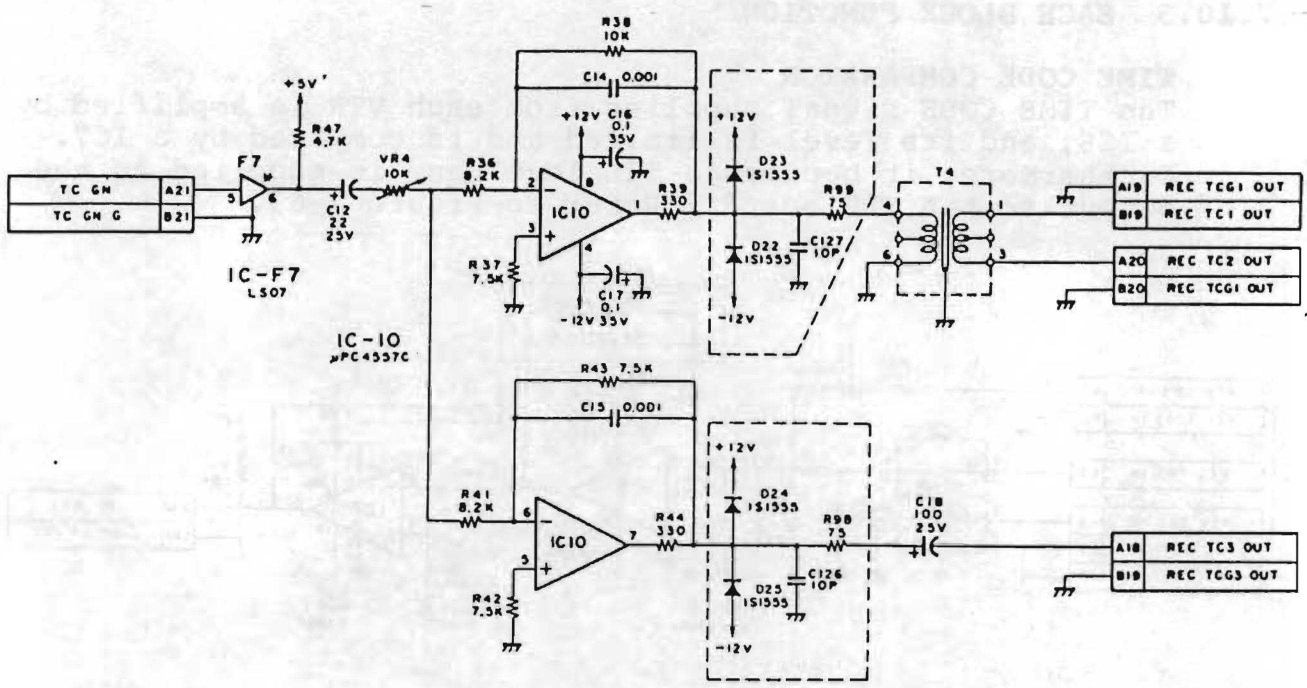


Figure 7-64 Generator output buffer

3. VIDEO SELECTOR

The VIDEO outputs of the PCM processor and 3 set VTR's are selected by the SWITCHER. Refer to Figure 7-65.

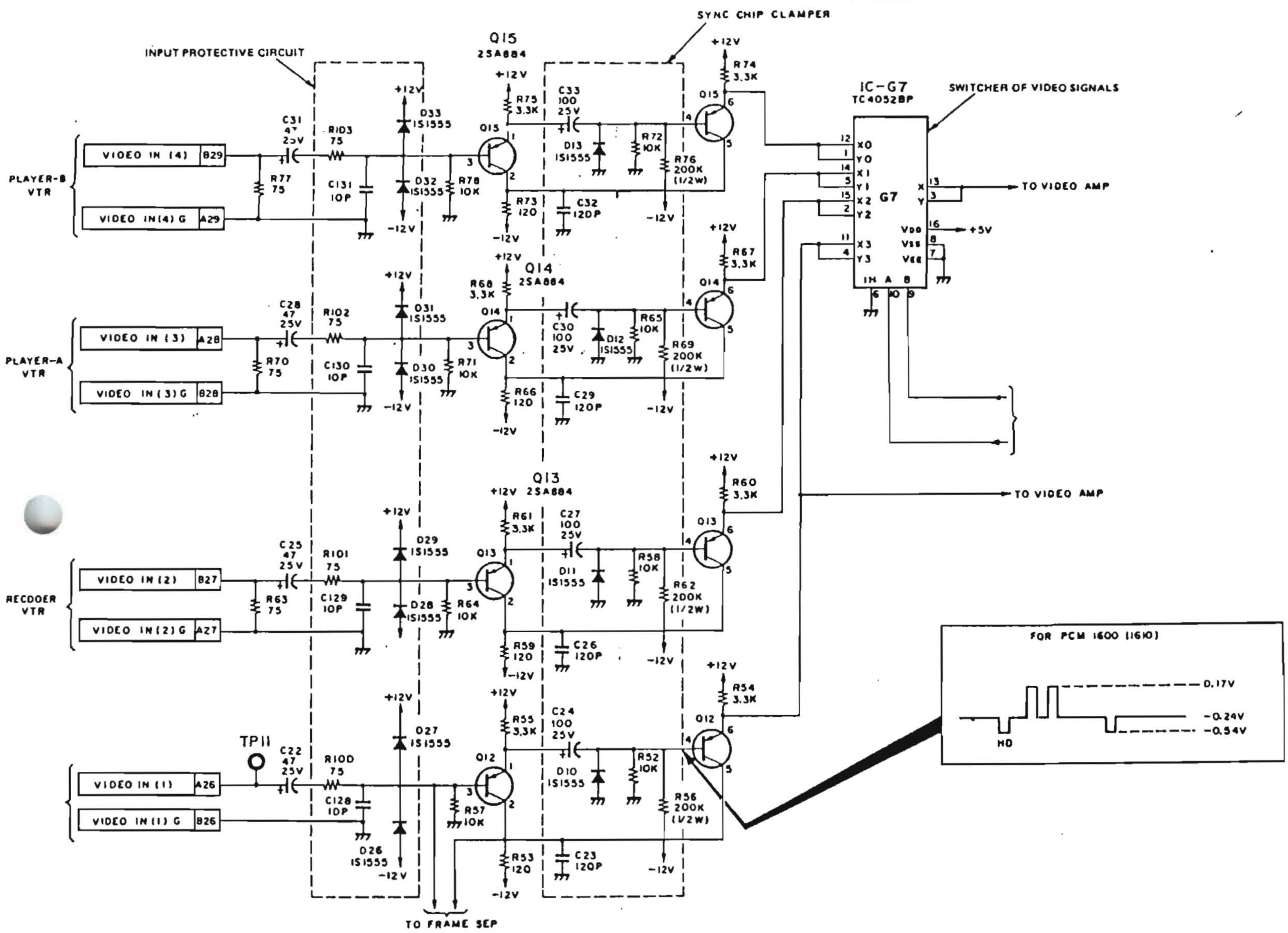


Figure 7-65 Video Selector Schematic Diagram

4. VIDEO AMP

After the output of the PCM processor and the output selected by the SWITCHER are adjusted to the specified LEVEL, the output is given by the output impeadance of 75 . Refer to Figure 7-66.

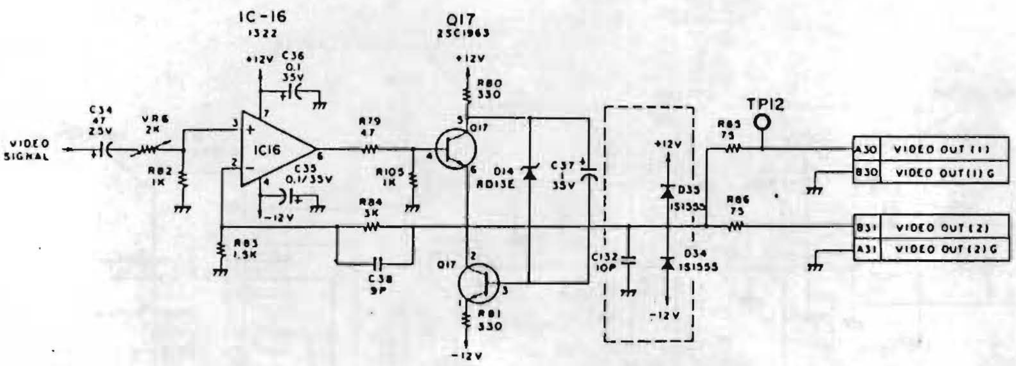


Figure 7-66 Video Amplifier

5. FRAME SEPARATOR

This derives the FRAME signal to conform with the reference from the VIDEO OUT signal of the PCM processor. Refer to Figure 7-67.

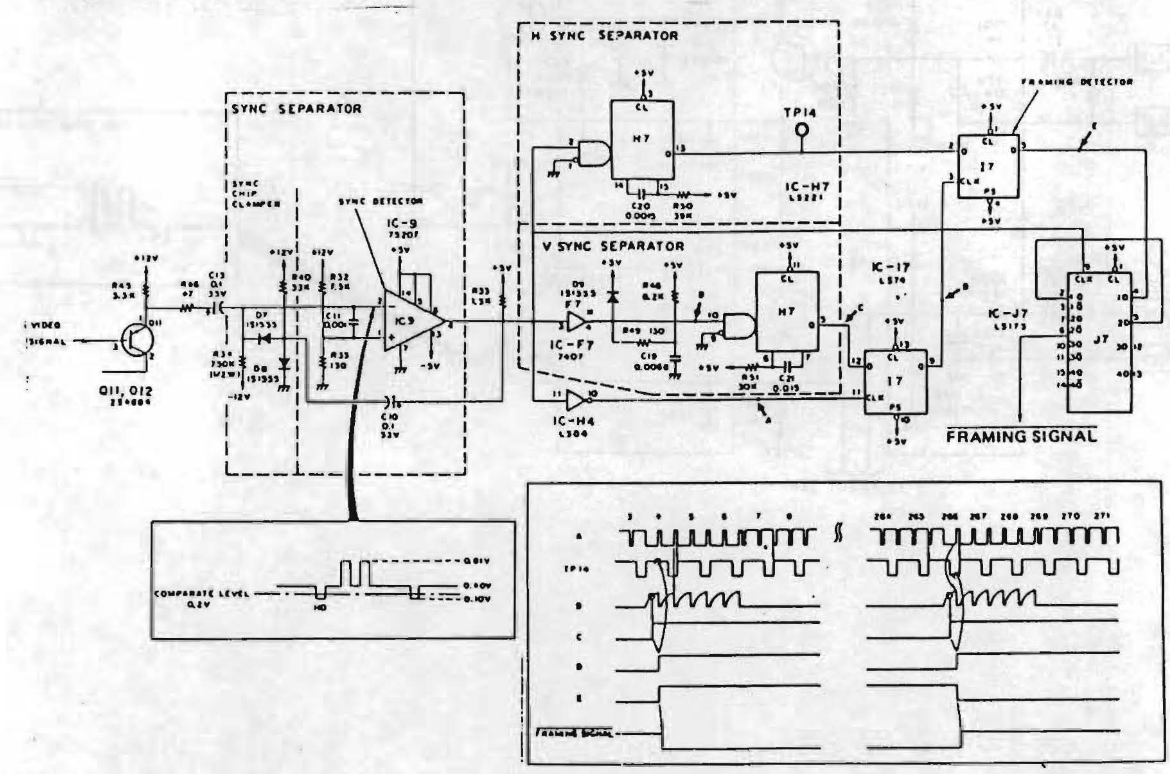


Figure 7-67 Frame Separator

6. EDIT TIMING CONTROLLER

This circuit inputs the TIMING of the FRAME unit necessary for the EDIT from the SYS board, reforming it to the TIMING of the WORD unit, and then it controls the ADDRESS COUNTER of the EDT board. Refer to Figures 7-68, 7-69, and 7-70.

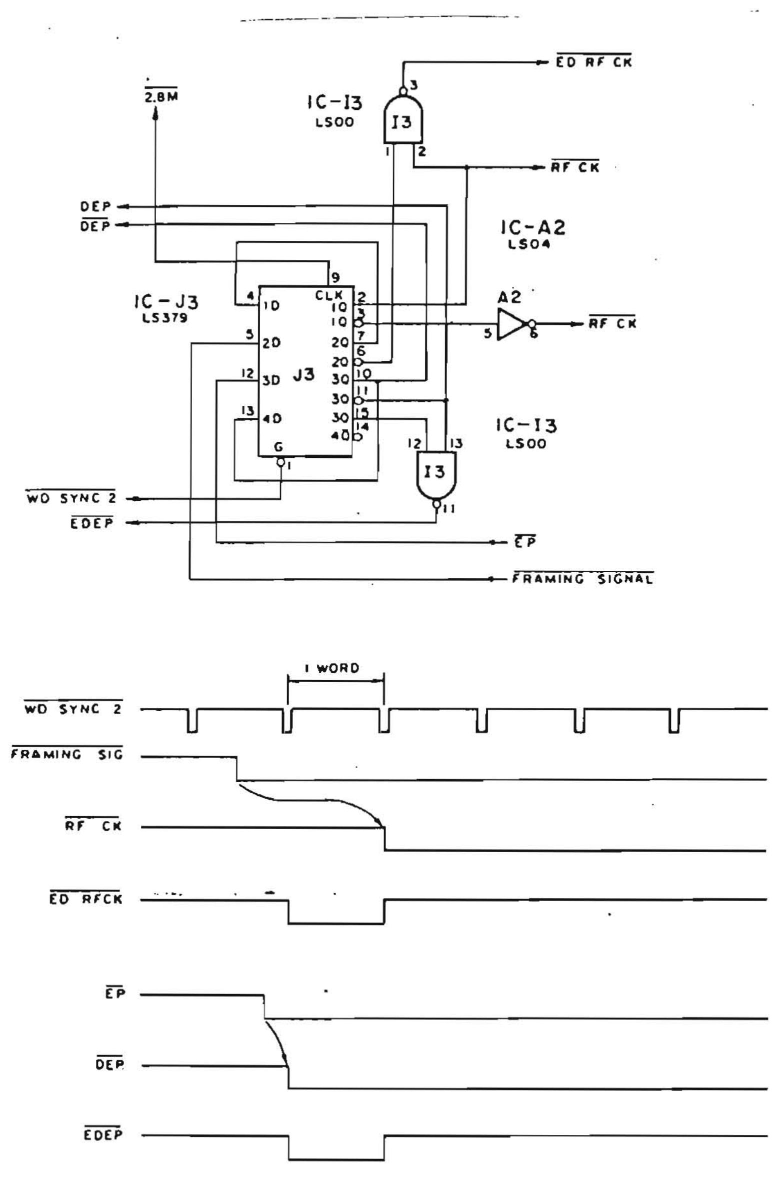


Figure 7-68 EDIT Timing Controller (1)

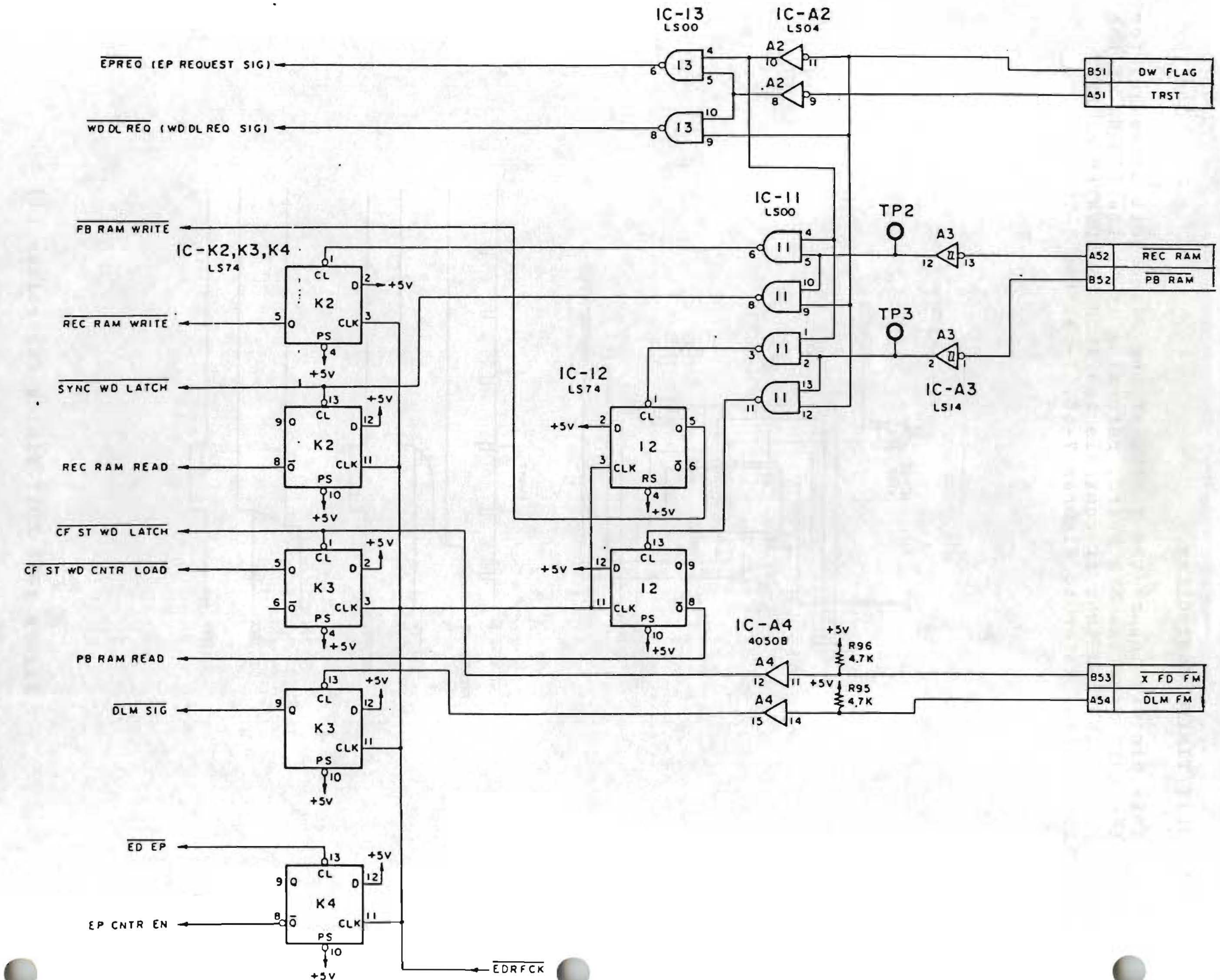


Figure 7-69 EDIT Timing Controller (2)

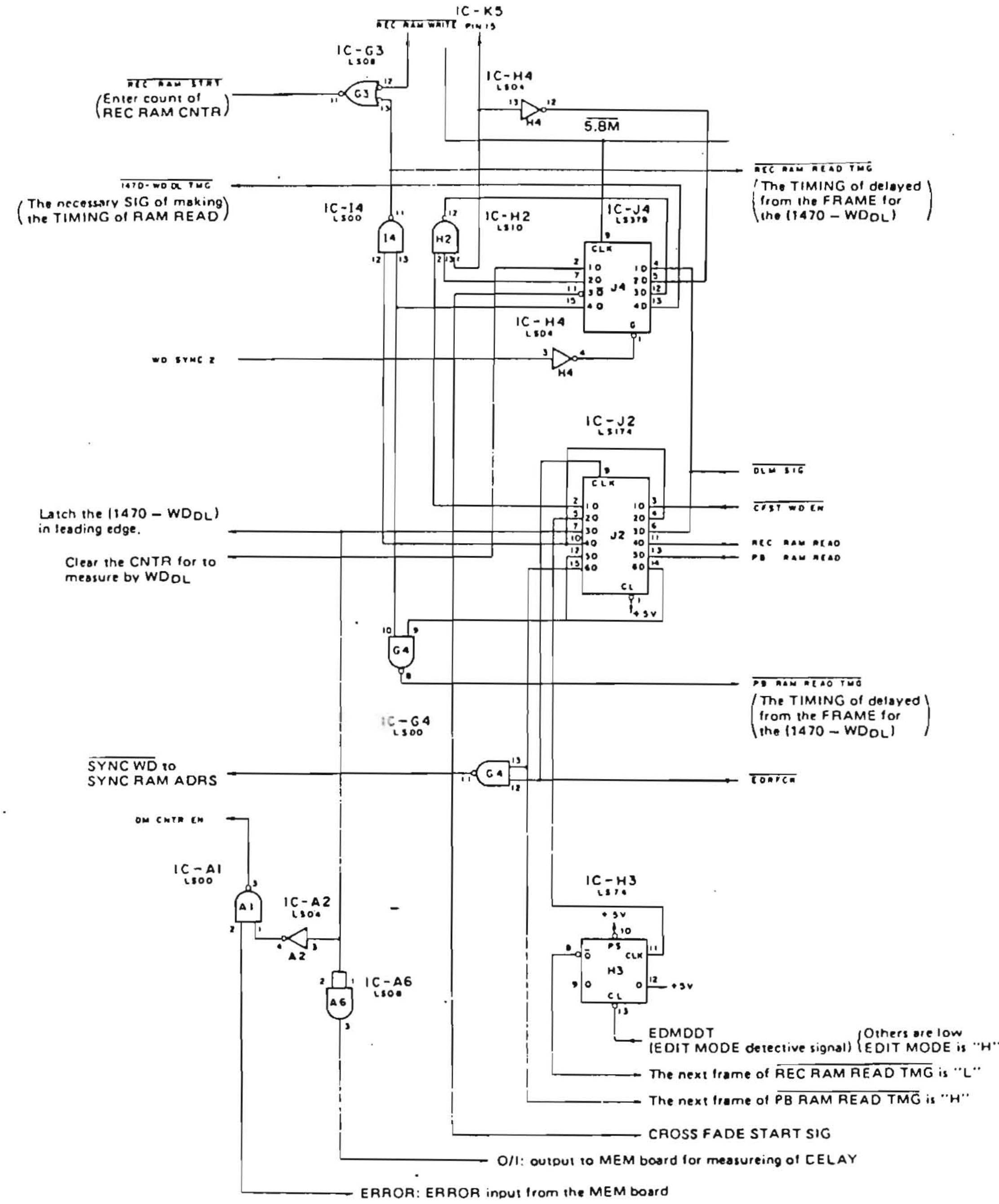


Figure 7-70 EDIT Timing Controller (3)

7. 1470-DELAY WORD COUNTER

This COUNTER is making the TIMING necessary for reading out the DATA written in the REC RAM or PB RAM from each RAM, early by the DELAY WORD (WDDL). Refer to Figure 7-71.

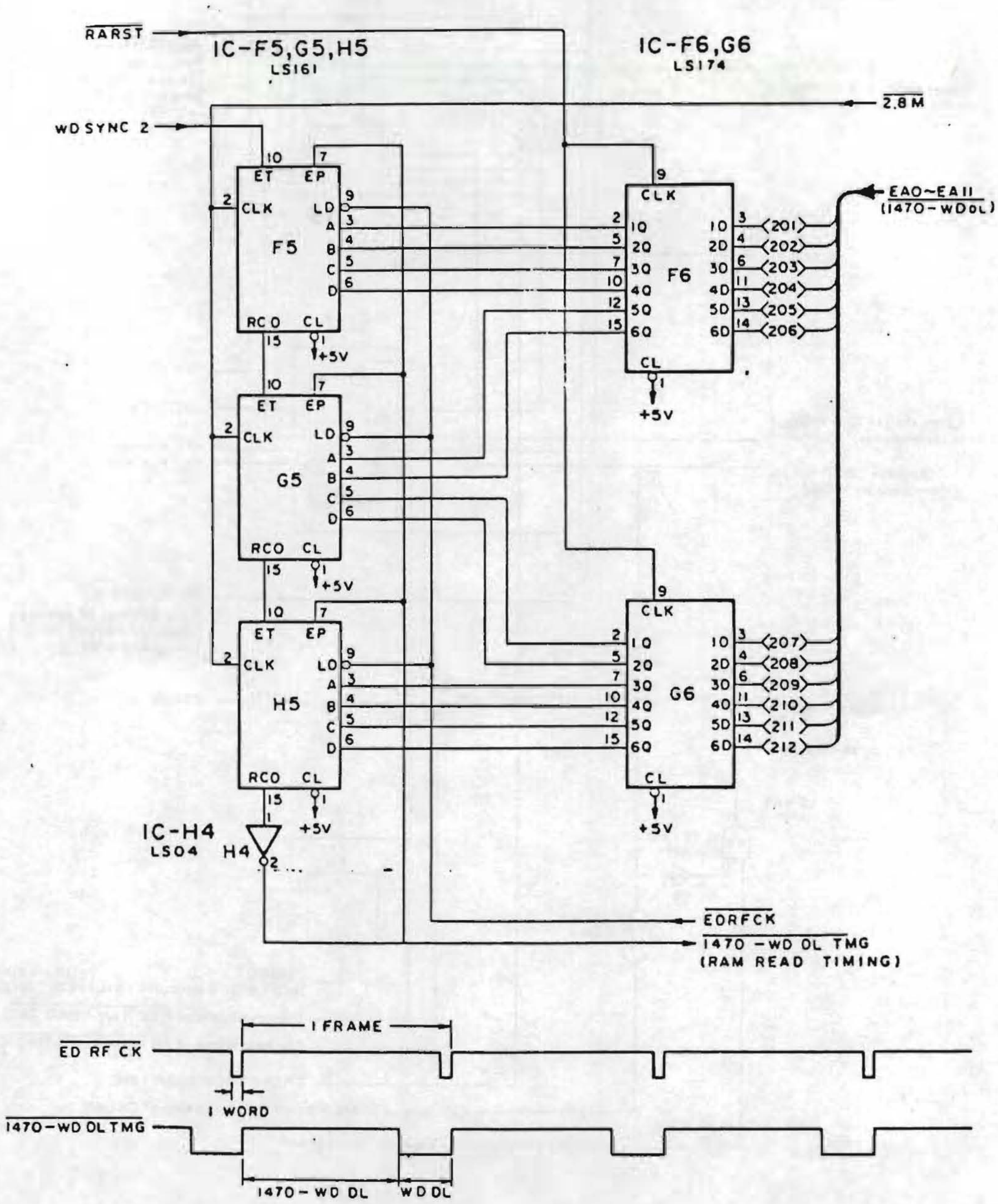


Figure 7-71 1470-delay word counter

8. REC RAM ADDRESS COUNTER

This circuit is composed of the ADDRESS COUNTER and OUTPUT BUFFER of the REC RAM. Refer to Figure 7-72.

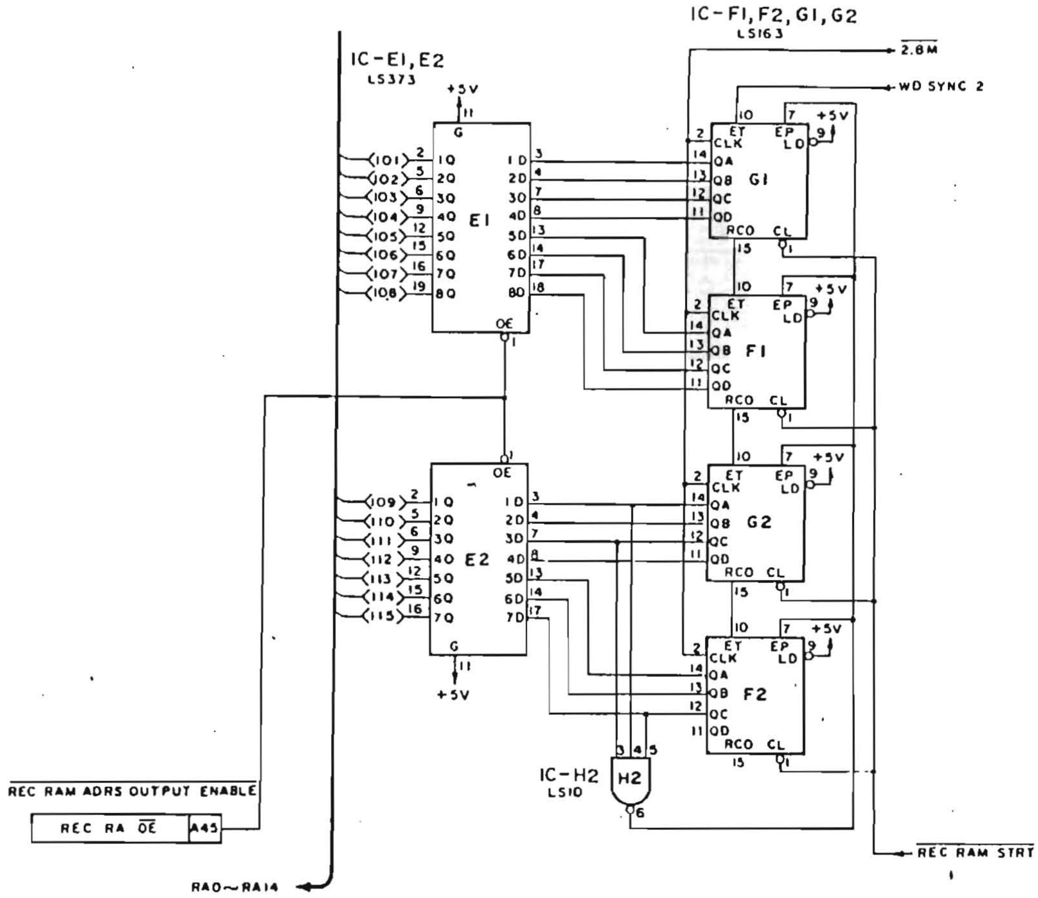
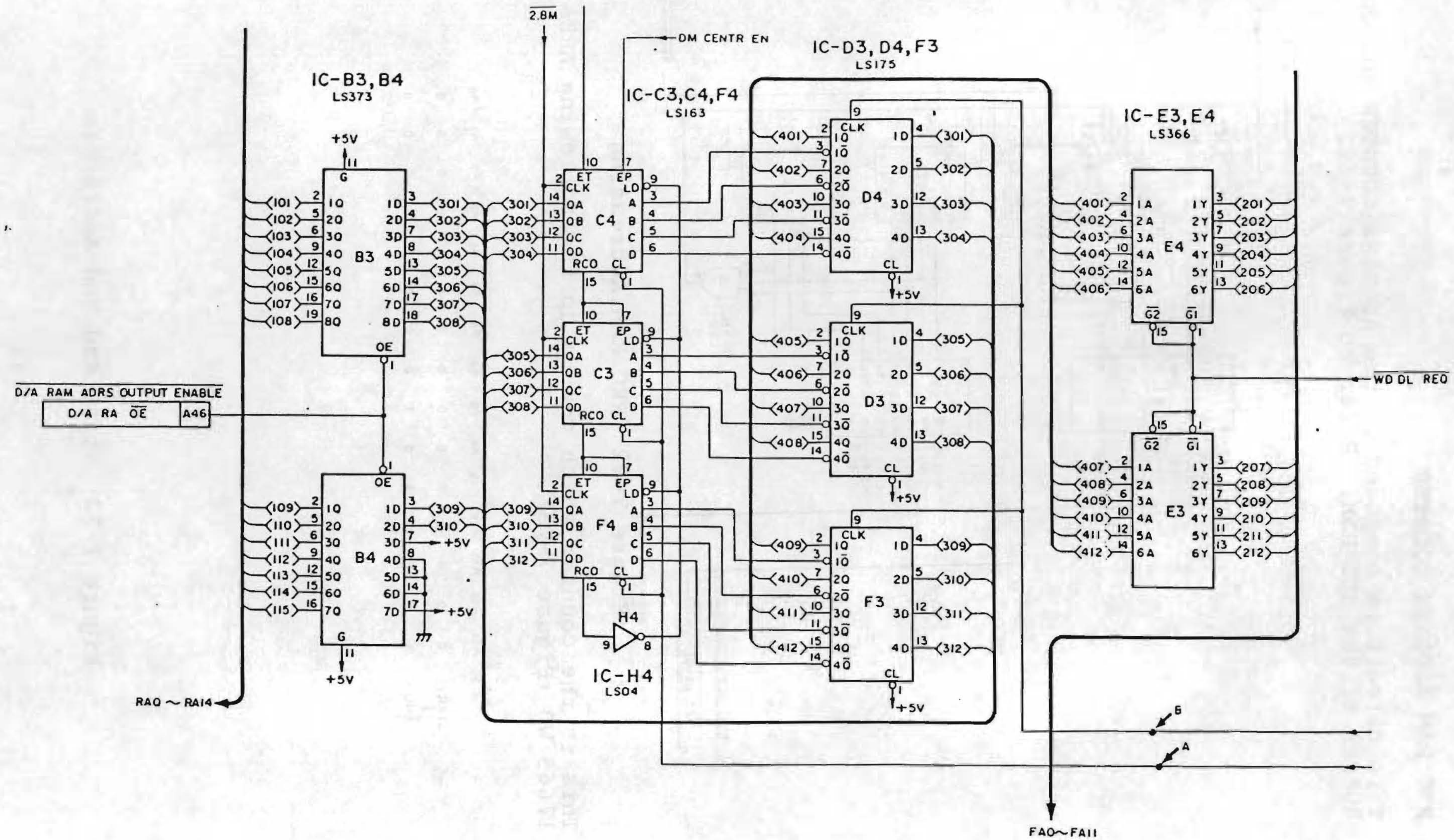


Figure 7-72 REC RAM Addressing

This is the counter which counts up the following AREA of 17665 WD (Figure 7-73).

	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
START	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
↓ END	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Figure 7-73 Start and End Addresses



IC-B3, B4
LS373
IC-C3, C4, F4
LS163
IC-D3, D4, F3
LS175
IC-E3, E4
LS366
IC-H4
LS04
2.8M
DM CENTR EN
D/A RAM ADRS OUTPUT ENABLE
D/A RA OE
A46
WD DL REQ
RA0 ~ RA14
FA0 ~ FA11
B3
B4
C4
C3
F4
D4
D3
F3
E4
E3
H4
+5V

9. D/A RAM ADDRESS COUNTER

This circuit is composed of the D/A ADDRESS COUNTER, its OUTPUT BUFFER and DELAY WORD COUNTER, and its DATA LATCH and OUTPUT BUFFER. Here, the D/A RAM ADDRESS COUNTER and the DELAY WORD COUNTER are used as the same COUNTER (C4,C3,F4). Refer to Figure 7-74.

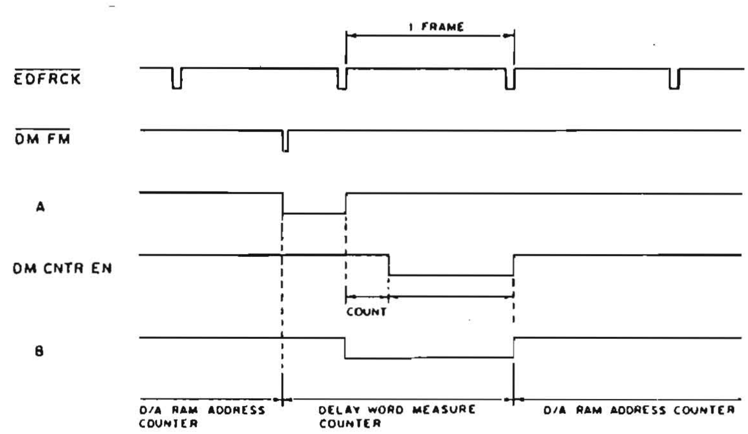
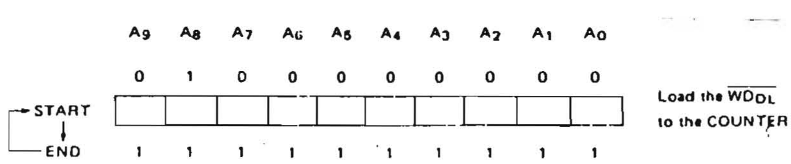


Figure 7-74 D/A RAM address counter

The D/A RAM ADDRESS COUNTER is the RING COUNTER which makes COUNT UP from on the way to the following AREA (767WD). Load the WDDL to the COUNTER.



Counter Load Address

10. PB RAM ADDRESS COUNTER

This circuit is composed of the PB RAM ADDRESS COUNTER and its OUTPUT BUFFER. Refer to Figure 7-76.

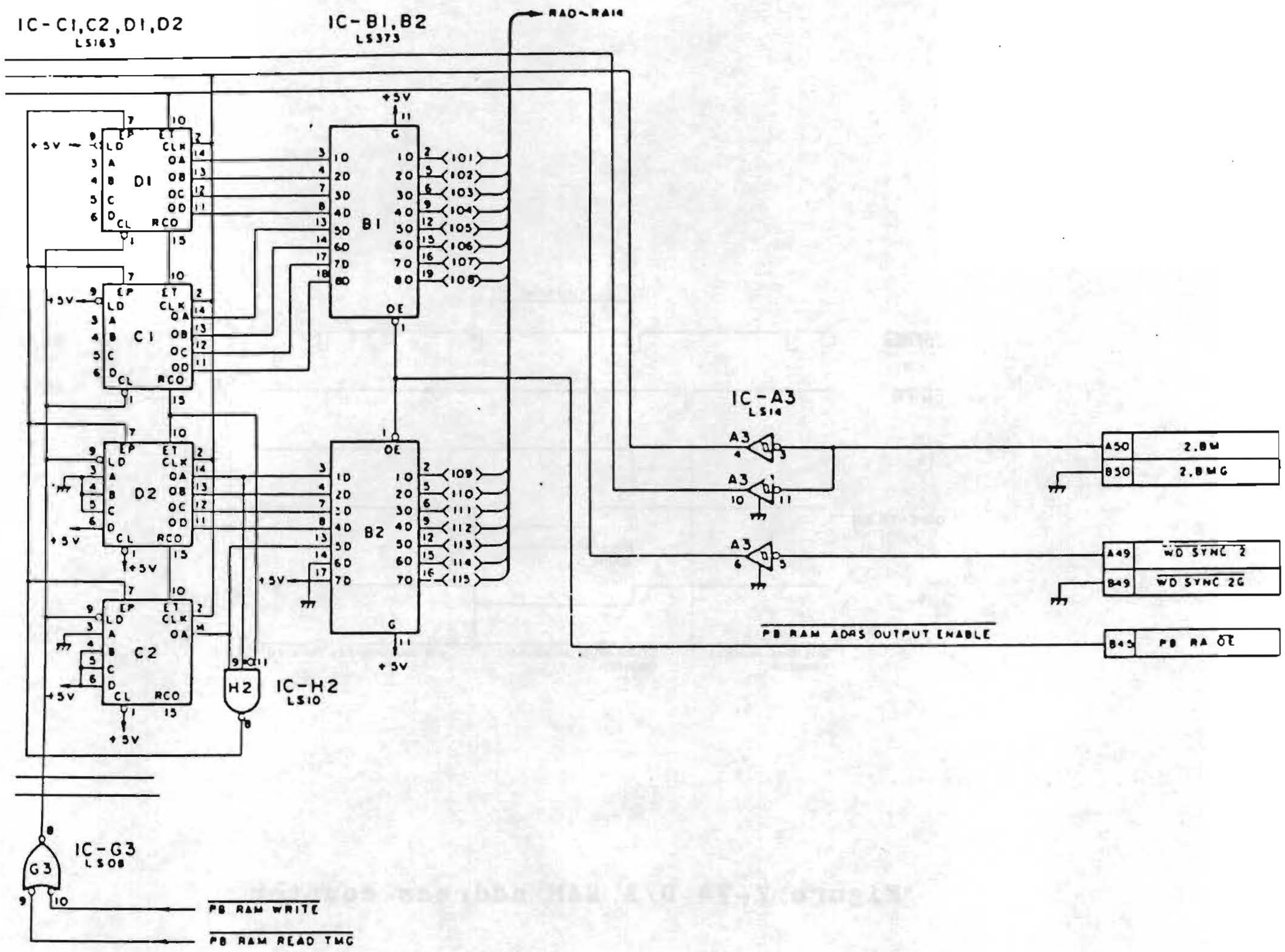


Figure 7-76 PB RAM Address Counter

The PB RAM ADDRESS COUNTER is the COUNTER providing the AREA of 2560 WORD, and it counts up one time due to the PB RAM WRITE and PB RAM READ TMG. (Figure 7-78).

	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
START	0	1	0	0	0	0	0	0	0	0	0	0	0
↓													
END	1	0	0	0	1	1	1	1	1	1	1	1	1

Figure 7-78 Start and End Addresses

11. SYNC RAM ADDRESS COUNTER

This circuit is composed of the SYNC RAM ADDRESS COUNTER, the RAM CLEAR ADDRESS COUNTER to write "0" in all the area of the RAM of MEM board, and those OUTPUT BUFFERS. Refer to Figure 7-79.

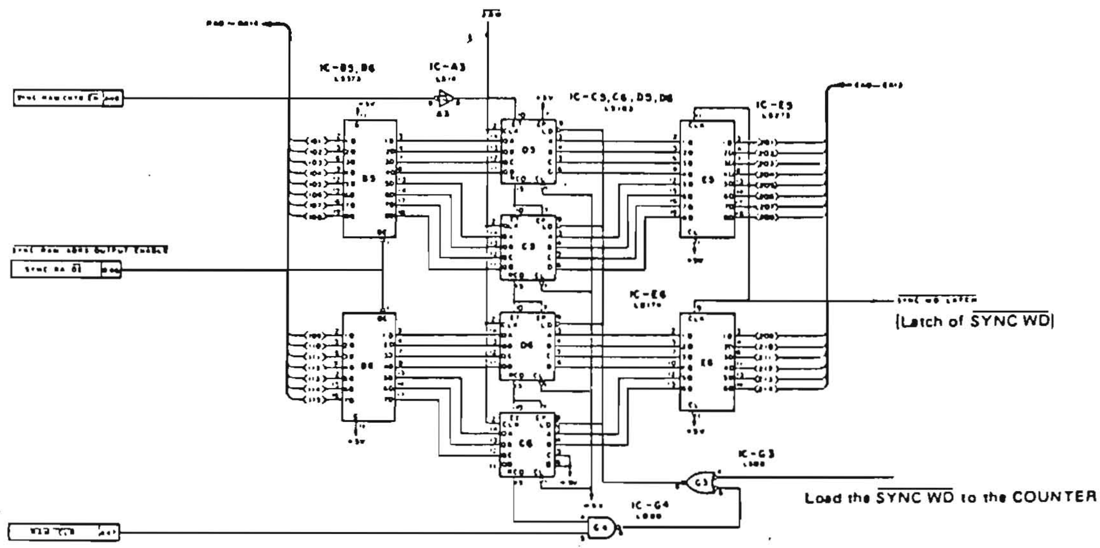


Figure 7-79 SYNC RAM address counter

Here, the D5, C5, D6 and C6 use both as the SYNC RAM ADDRESS COUNTER and the RAM CLEAR ADDRESS COUNTER.
The SYNC RAM ADDRESS COUNTER, which provides and AREA of 11776 WORDS is used as the RING COUNTER due to being loaded with the SYNC WD.
On the other hand, the RAM CLEAR COUNTER is used due to the RAM CLEAR MODE.
Load the SYNC WD
In case of the RAM CLEAR, all the ADDRESSES are counted up from the ADDRESS, and are accessed only one time without fail.
Figure 7-80.

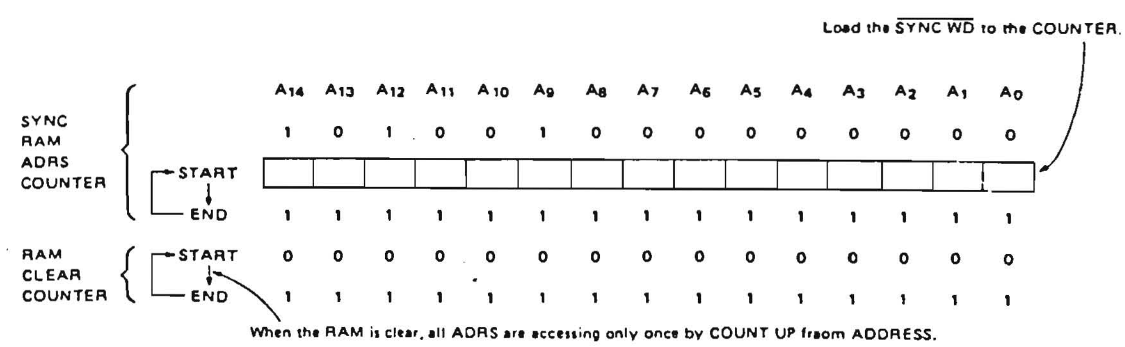


Figure 7-80 RAM Counter Start and End Addresses

12. EDIT POINT WORD COUNTER

This circuit is composed of the EDIT WORD COUNTER counting the WORD number in the FRAME when the EDIT POINT (OUT-POINT or IN-POINT) is pressed and its OUTPUT BUFFER, THE CROSS FADE START WORD COUNTER counting the WORD in the FRAME of the CROSS FADE START POINT (EDIT POINT) of (PREVIEW or AUTO EDIT) in EDIT, and the INPUT F.F. latching the value to load to THE COUNTER. Each counter is used together here. Refer to Figure 7-81.

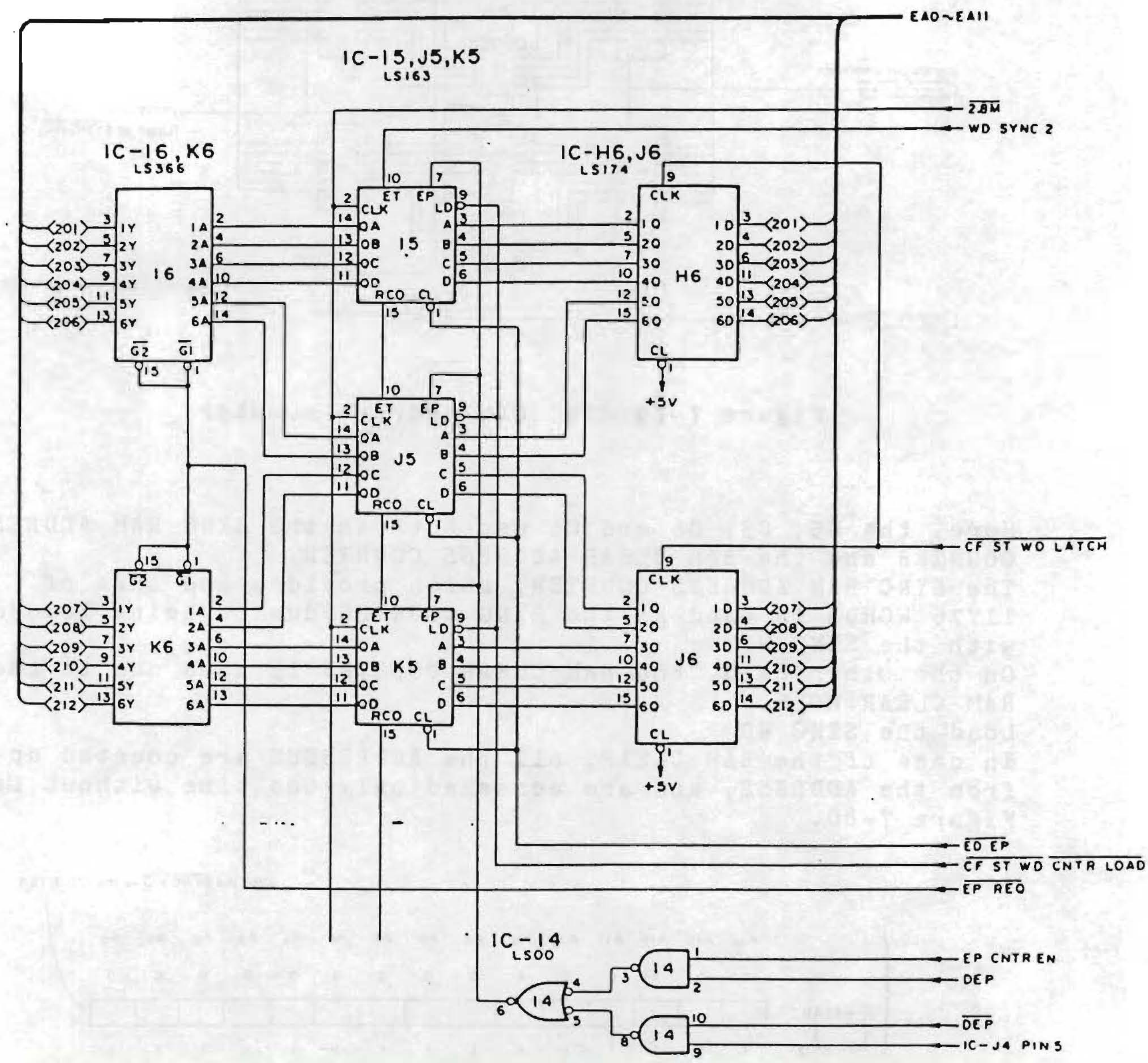


Figure 7-81 EDIT Point word counter circuit

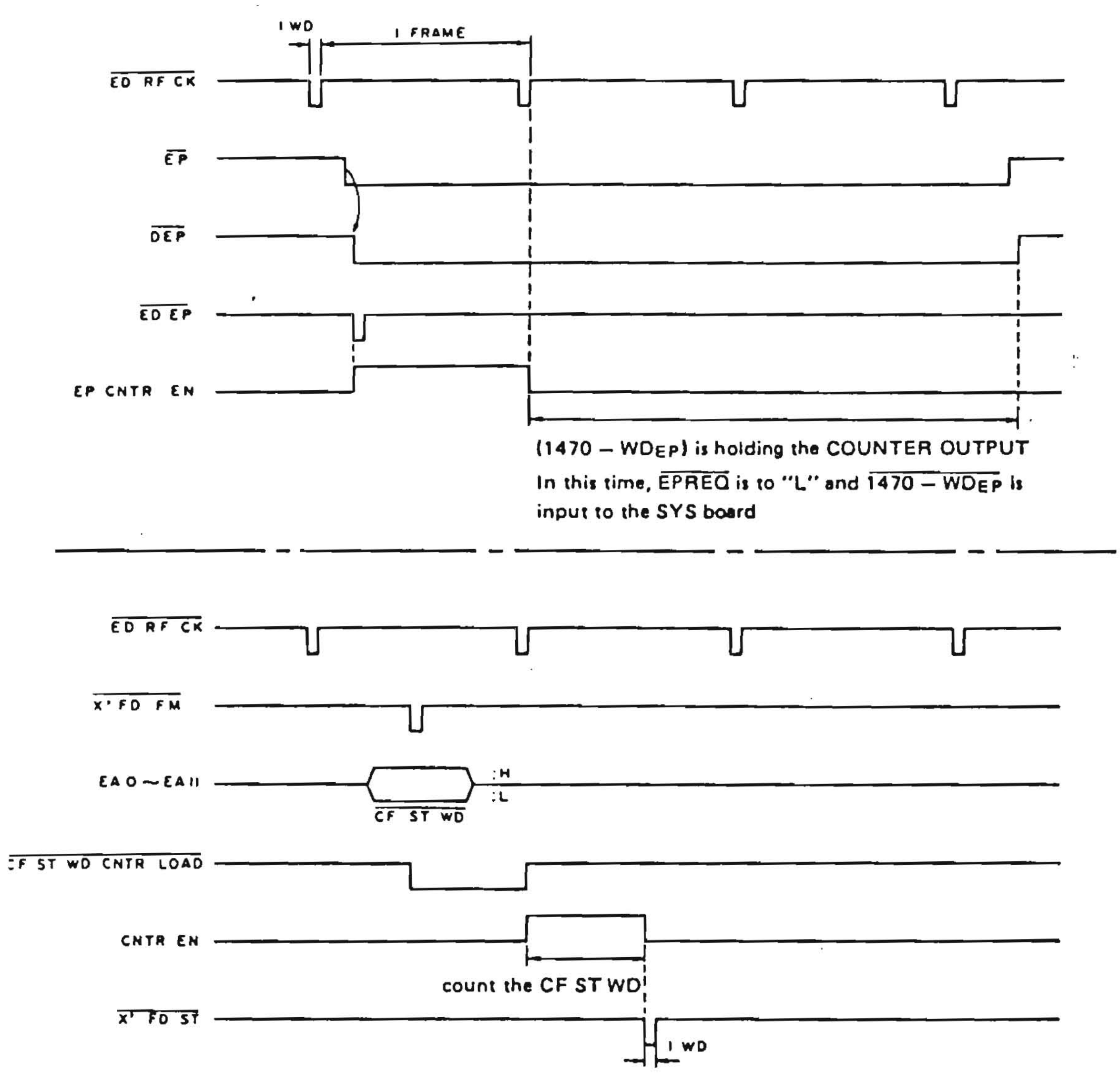


Figure 7-82 Timing of Figure 7-81

13. EDIT MODE CONTROLLER

This circuit sends the signal to the SC-B board after converting the EDIT MODE (EDTM 0 - 3 = 1) in the EDITOR MODE received from the SYS board into the EDIT 1 - 4 of WD unit.

The other mode is sent to the SC-B board after reforming to the signal of the FRAME unit and, also in relation to the signal of the VIDEO SELECT, the circuit makes the PCM processor SELECT MODE due to the EDT board in case of the EDIT MODE. Refer to Figure 7-83.

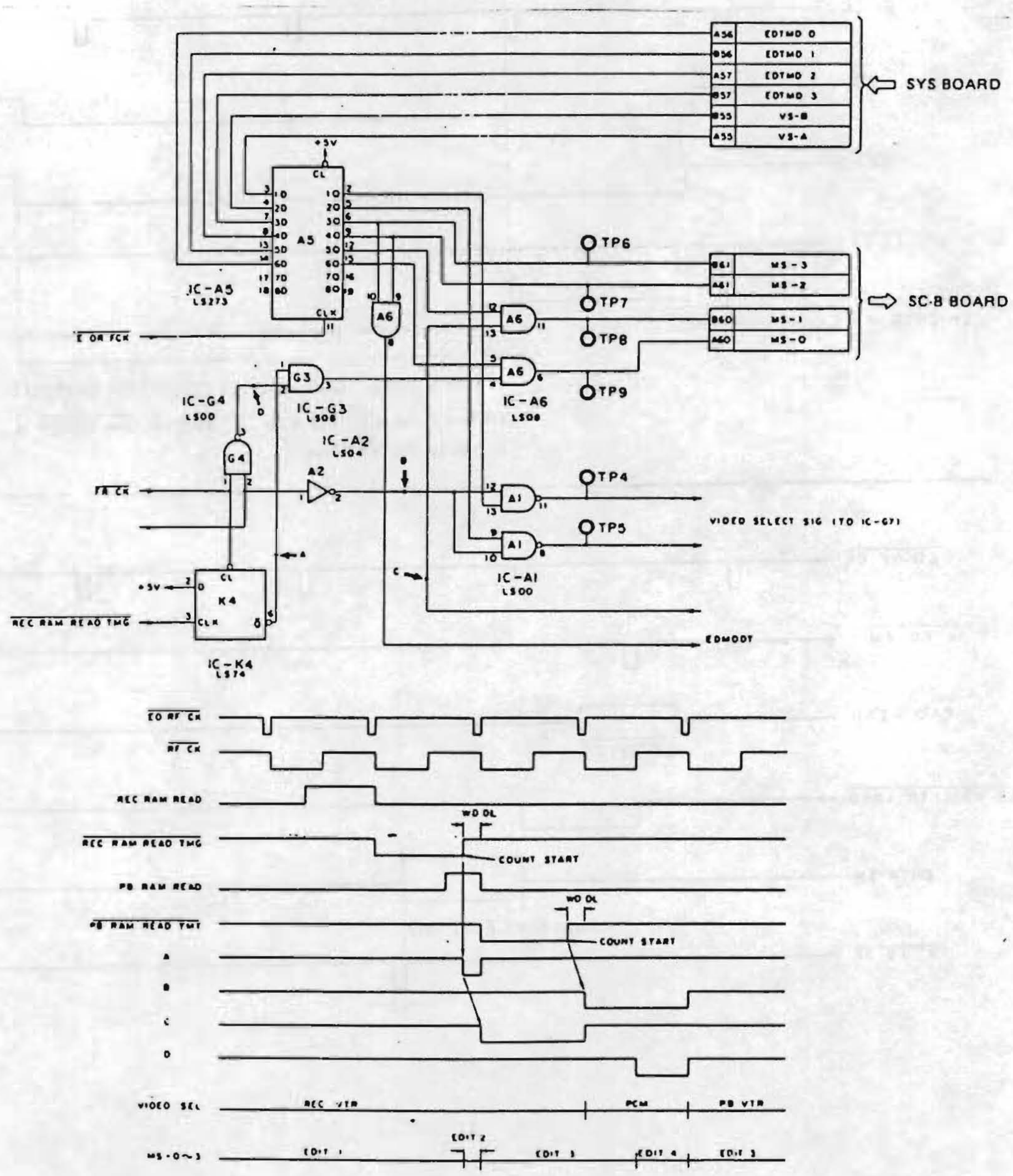


Figure 7-83 EDIT mode controller

Figure 7-84 shows the general timing chart In the EDIT MODE (EDIT 1-4)

Figure 7-84 the SUMMARY of the TIMING IN the EDIT MODE.

Table 7-10-3 shows the operation procedure of the Mode in MS 3 = 1.

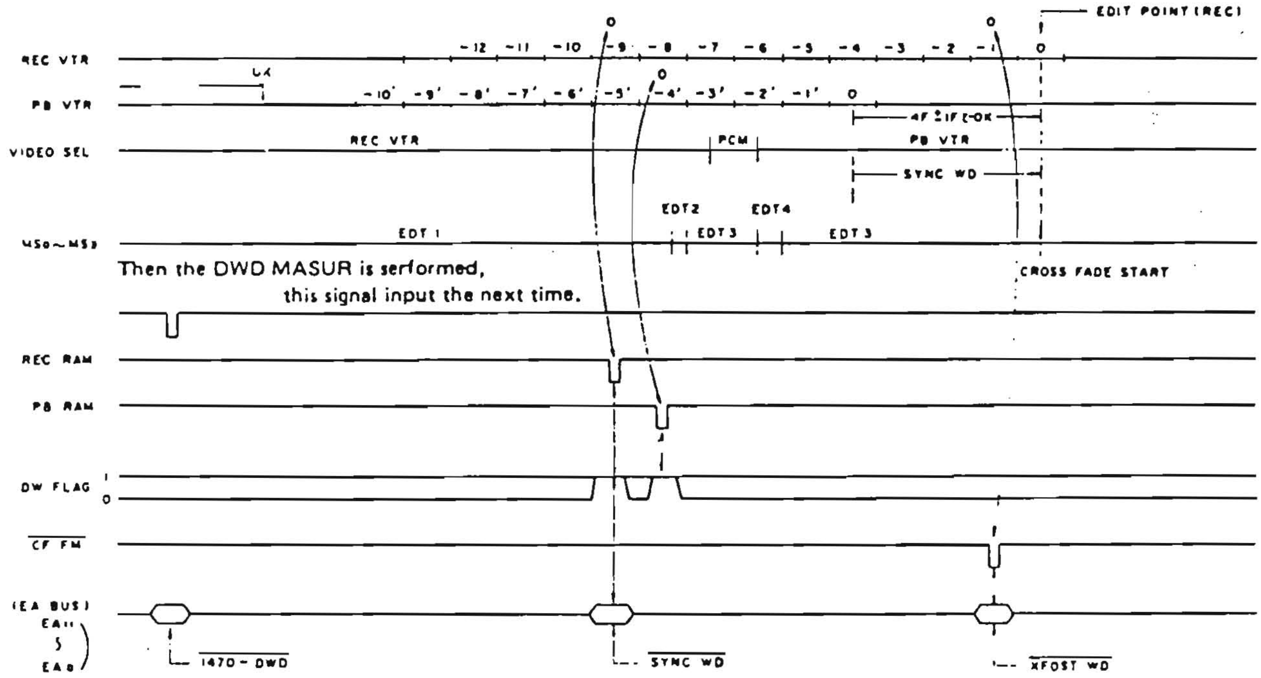


Figure 7-84 EDIT MODE Timing

	MUTE OUTPUT	EDIT 1	EDIT 2	EDIT 3
REC FF		IN BUFF	REC RAM OUT	REC RAM OUT
PB FF		(SYNC RAM OUT)	(SYNC RAM OUT)	SYNC RAM OUT
REC RAM IN	――――	――――	――――	――――
PB RAM IN	――――	――――	――――	――――
D/A RAM IN		(X'FADE OUT)	X'FADE OUT	X'FADE OUT
SYNC RAM IN		(IN BUFF)	(IN BUFF)	IN BUFF
D/A FF	RD INJ.	X'FADE OUT	IN BUFF	D/A RAM OUT
ENC FF	RD INJ.	(X'FADE OUT	X'FADE OUT	X'FADE OUT
RD CHECK				

	EDIT 4	REC RAM WRITE	PB RAM WRITE	DLY MESUR
REC FF	REC RAM OUT			IN BUFF
PB FF	(SYNC RAM OUT)			
REC RAM IN	――――	IN BUFF	――――	――――
PB RAM IN	――――	――――	IN BUFF	――――
D/A RAM IN	X'FADE OUT			
SYNC RAM IN	(IN BUFF)			
D/A FF	D/A RAM OUT	RD INJ.	RD INJ.	RD INJ.
ENC FF	PB RAM OUT			RD INJ.
RD CHECK				X'FADE OUT

Table 7-10-2 EDIT Mode Operation

7.11. TIME CODE CIRCUIT (TLC BOARD)

7.11.1 General

The TLC printed board has one S MPTE TIME CODE GENERATOR and three SMPTE TIME CODE READERS and AUTO LOCATORS. The GENERATOR can select DROP-FRAME or FULL-FRAME via a switch mounted on the printed board. Values can be preset from the keyboard. In the AUTO-EDIT mode, continuous recording of time codes is possible by automatically locking to the REC-VTR READER. The READER corrects errors by collating time code data with frame clock extracted from the reference video signals, and with CTL. Therefore, it can read normal values even if time code data is missing for several frames. The TLC board comprises a Z-80 CPU used as generator, reader, and locator.

7.11.2 Configuration

Figure 7-85 shows a block diagram of the TCL board. As Figure 7-8-5 depicts, this board consists of a 9.8304 MHz quartz crystal oscillator (1), clock generator (2), Z-80 CPU (3), CPR addresss decoder (4), CPU main program ROM (5), CPU working RAM (6), Data I/O (7) to the SYS board, CPU interrupt controller (8),flag I/O (9) to show the time code status, time code generator (10) to convert data received from the CPU into SMPTE format, time code data RAMs (14), (15) and (16) to temporarily store time code read for input to the CPU, and time code data separators (11), (12) and (13) to extract time code data from input code signals.

Figure 7-85 Block diagram of TLC board

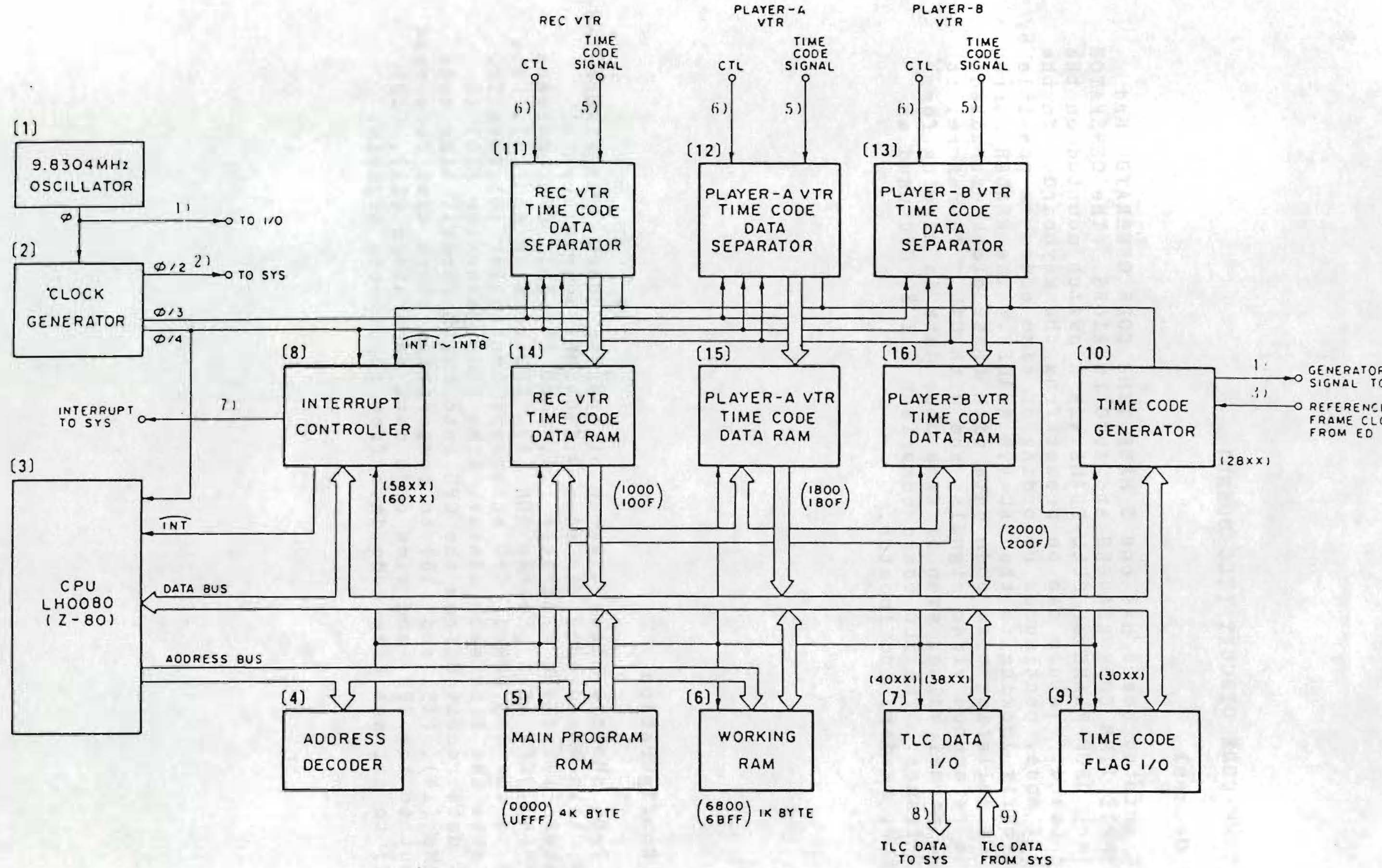


Figure 7-85 Block Diagram of TLC Board

7.11.3 Explanation of Circuits

7.11.3.1 Input and Output Signals

1 o (9,83M) to I/O board

A 9.8304 MHz clock signal

2 o/2 (CK2CPU) to SYS board

A 4.9152 MHz clock signal
As with the TLC board, the SYS board demultiplies this clock by two and clocks the CPU (Z-80) at a frequency of 2.4576 MHz.

3 **REFERENCE FRAME CLOCK (RF CK) from EDT board.**

This clock is extracted from reference input video signals (ex. VIDEO OUT of PCM-1600) and is the most important signal on this board. INT1, which has the higher priority among CPU interrupt signals, is generated from the trialing edge of this signal.

4 **GENERATOR SIGNAL (TCGN) to EDT board.**

5 **TIME CODE SIGNALS (TCDT1, TCDT2 and TCDT3) from EDT board.**

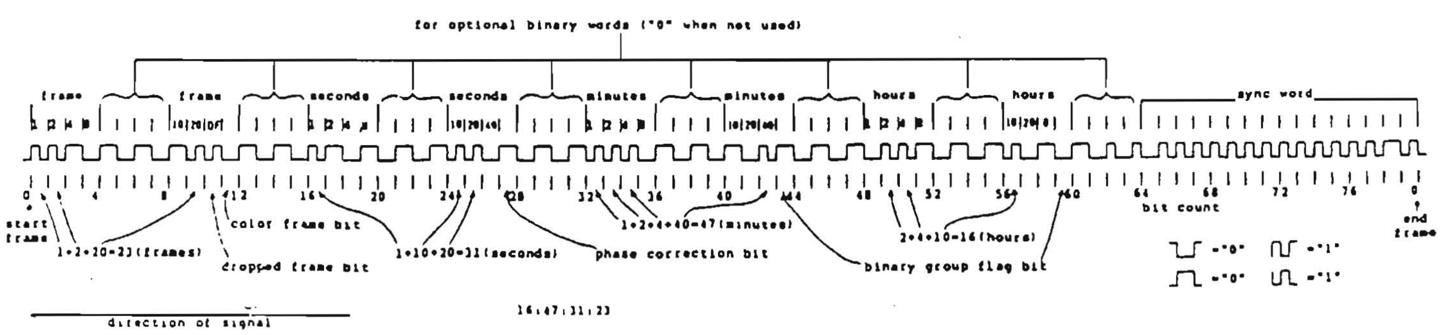
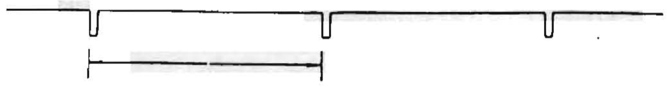


Figure 7-86 Standard SMPTE Time Code (1 frame)

The signals TCGN, TCDT1, TCDT2, TCDT3 are TTL level signals as shown in Figure 2-6-2.
TCGN: Time code generator signal
TCDT1: Recorder VTR Time code signal
TCDT2: Player-A VTR Time code signal
TCDT3: Player-B VTR Time code signal

6 **CTL (RCTL, PACTL AND PBCTL) from VTR**



Equivalent to one frame on tape
RCTL: Recorder VTR CTL signal
PACTL:Player-A VTR CTL signal
PBCTL:Player-B VTR CTL signal

7 **INTERRUPT (TC. INT)to SYS board.**

An interrupt signal generated by the TLC board for data exchange between the TLC and SYS boards.

8 **TLC DATA (TC0-TC7) to SYS board.**
This is data supplied from the TLC board to the SYS board. 32 bytes of data are sent every frame. Table 7-11-1 shows the various types of data.

BYTE \ DATA	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	COMMENTS
1		dropped frame bit	x10 Frames			x1 Frame			REC VTR TC (Frame)
2		x10 Sec				x1 Sec			REC VTR TC (Sec)
3		x10 Min				x1 Min			REC VTR TC (Min)
4		x10 Hour				x1 Hour			REC VTR TC (Hour)
5									REC VTR User's Bit
6									REC VTR User's Bit
7				User's Bit					REC VTR User's Bit
8									REC VTR User's Bit
9		dropped frame bit	x10 Frames			x1 Frame			PLAYER-A VTR TC (Frame)
10		x10 Sec				x1 Sec			PLAYER-A VTR TC (Sec)
11		x10 Min				x1 Min			PLAYER-A VTR TC (Min)
12		x10 Hour				x1 Hour			PLAYER-A VTR TC (Hour)
13									PLAYER-A VTR User's Bit
14									PLAYER-A VTR User's Bit
15				User's Bit					PLAYER-A VTR User's Bit
16									PLAYER-A VTR User's Bit
17		dropped frame bit	x10 Frame			x1 Frame			PLAYER-B VTR TC (Frame)
18		x10 Sec				x1 Sec			PLAYER-B VTR TC (Sec)
19		x10 Min				x1 Min			PLAYER-B VTR TC (Min)
20		x10 Hour				x1 Hour			PLAYER-B VTR TC (Hour)
21									PLAYER-B VTR User's Bit
22									PLAYER-B VTR User's Bit
23				User's Bit					PLAYER-B VTR User's Bit
24									PLAYER-B VTR User's Bit
25		dropped frame bit	x10 Frame			x1 Frame			GENERATOR TC (Frame)
26		x10 Sec				X1 Sec			GENERATOR TC (Sec)
27		x10 Min				x1 Min			GENERATOR TC (Min)
28		x10 Hour				x1 Hour			GENERATOR TC (Hour)
29	Speed A	Speed B	REW	FF	REV	FWD	PAUSE	STOP	REC VTR COMMAND
30	Speed A	Speed B	REW	FF	REV	FWD	PHASE	STOP	PLAYER-A VTR COMMAND
31	Speed A	Speed B	REW	FF	REV	FWD	PHASE	STOP	PLAYER-B VTR COMMAND
32									FLAG BYTE

Table 7-11-1 Time Code Table

• FLAG BYTE

TC0	(EDT POINT – TC) Compared Result:		TC1	TC0
TC1		<	0	1
		>	1	0
		=	1	1
TC2	REC VTR Auto Locator End Flag			
TC3	PLAYER-A VTR Auto Locator End Flag			
TC4	PLAYER-B VTR Auto Locator End Flag			
TC5	REC VTR TC Error Flag			
TC6	PLAYER-A VTR TC Error Flag			
TC7	PLAYER-B VTR TC Error Flag			

Table 7-11-2 Flag Byte Chart

9 TLC DATA (TG0-TG7) from SYS board.

This is data sent by the SYS board to the TLC board, and 29 bytes are sent immediately following TC0 through TC7.

BYTE \ DATA	TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0	COMMENTS
1		x10 Frame				x1 Frame			REC VTR Auto Locate Target (Frame)
2		x10 Sec				x1 Sec			REC VTR Auto Locate Target (Sec)
3		x10 Min				x1 Min			REC VTR Auto Locate Target (Min)
4		x10 Hour				x1 Hour			REC VTR Auto Locate Target (Hour)
5		x10 Frame				x1 Frame			PLAYER-A VTR Auto Locate Target (Frame)
6		x10 Sec				x1 Sec			PLAYER-A VTR Auto Locate Target (Sec)
7		x10 Min				x1 Min			PLAYER-A VTR Auto Locate Target (Min)
8		x10 Hour				x1 Hour			PLAYER-A VTR Auto Locate Target (Hour)
9		x10 Frame				x1 Frame			PLAYER-B VTR Auto Locate Target (Frame)
10		x10 Sec				x1 Sec			PLAYER-B VTR Auto Locate Target (Sec)
11		x10 Min				x1 Min			PLAYER-B VTR Auto Locate Target (Min)
12		x10 Hour				x1 Hour			PLAYER-B VTR Auto Locate Target (Hour)
13		x10 Frame				x1 Frame			EDIT POINT Compare Data (Frame)
14		x10 Sec				x1 Sec			EDIT POINT Compare Data (Sec)
15		x10 Min				x1 Min			EDIT POINT Compare Data (Min)
16		x10 Hour				x1 Hour			EDIT POINT Compare Data (Hour)
17		x10 Frame				x1 Frame			Generator TC Initial Data (Frame)
18		x10 Sec				x1 Sec			Generator TC Initial Data (Sec)
19		x10 Min				x1 Min			Generator TC Initial Data (Min)
20		x10 Hour				x1 Hour			Generator TC Initial Data (Hour)
21									Generator User's Bit Initial Data (F
22									Generator User's Bit Initial Data
23				User's Bit					Generator User's Bit Initial Data
24									Generator User's Bit Initial Data
25	Speed B	Speed A	REW	FF	REV	FWD	PAUSE	STOP	REC VTR STATUS
26	Speed B	Speed A	REW	FF	REV	FWD	PAUSE	STOP	PLAYER-A VTR STATUS
27	Speed B	Speed A	REW	FF	REV	FWD	PAUSE	STOP	PLAYER-B VTR STATUS
28								•	CONTROL BYTE A
29								••	CONTROL BYTE B

Table 7-11-3 TLC Data (TGO – TG7)

*CONTROL BYTE A

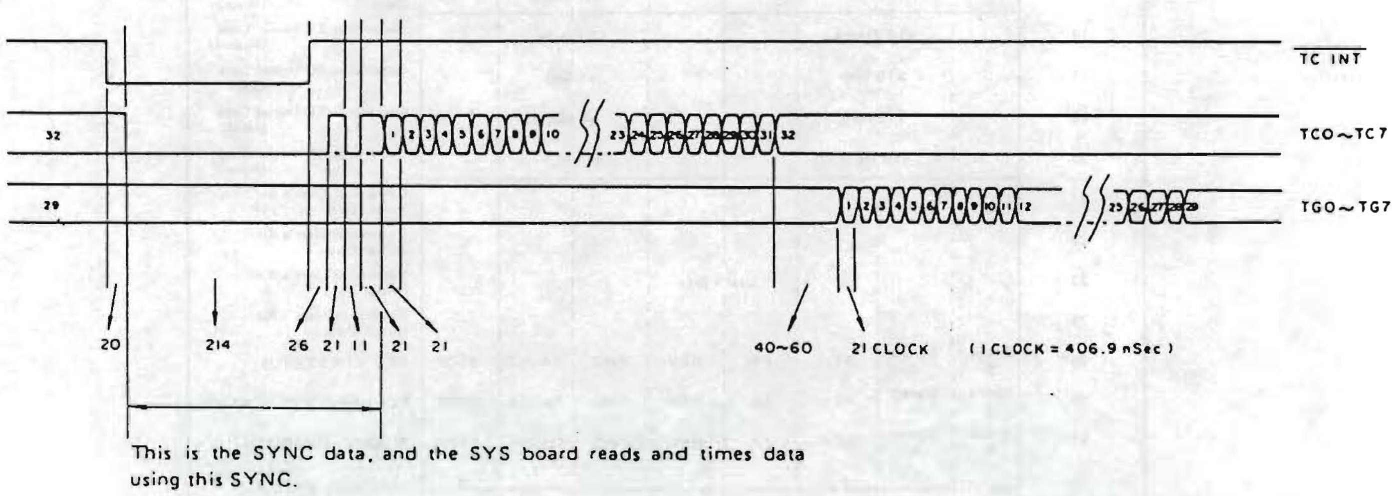
TG0	REC VTR Auto Locate MODE SET
TG1	PLAYER-A VTR Auto Locate MODE SET
TG2	PLAYER-B VTR Auto Locate MODE SET
TG3	VALID EDIT POINT DATA
TG4	GENERATOR DATA SET
TG5	User's Bit DATA SET
TG6	SYNC MODE
TG7	CODE LOCK MODE (JUM CODE)

** CONTROL BYTE B

TG0	PLAYER SELECT	0:PLAYER-A	1:PLAYER-B
TG1	EDIT POINT	0:RECORDER	1:PLAYER
TG3	EDIT POINT SW (PLAYER)		
TG4	EDIT, PREVIEW MODE		
TG5	SELECT Auto Locate Direction	0:FWD 1:REV	
TG6	NOT USE		
TG7	NOT USE		

*** When the Recorder VTR or Player VTR EDIT POINT is pushed, the edit point is maintained high for one frame. Thus the TLC board determines the time code drift point.

TC INT, TC0 ~ TC7 and TG0 ~ TG7 Timing.



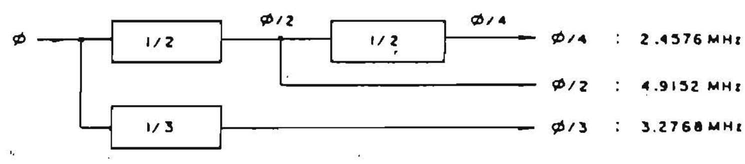
TCINT, TC0-TC7 and TG0-TG7 Timing.

7.11.3 Function of Each Block

1 **9.8304 MHz Oscillator**

This is an oscillator comprising a 9.8304MHz quartz crystal unit and TTL7404. The clock of this oscillator is used as master clock (0) for the TLC board.

2 **Clock Generator**



Clock Divider Block Diagram

o/2: A clock of twice the frequency is used to change the duty ratio of the CPU clock on the SYS Board to 50%.

o/4: CPU clock. Interrupt controller clock.

o/3, o/4: TIME CODE DATA SEP Clock

3 **CPU**

Z-80 is clocked at 2.4576MHz (o/4).
T Cycle = 406.9 ns

4 **Address Decoder**

The TLC board has a memory-mapped I/O configuration. Address decoding uses A_{14}, A_{13}, A_{12} and A_{11} and the data area is divided every 2 kilobytes.

ADDRESS	DATA AREA	DEVICE	CONTENTS D7	D6	D5	D4	D3	D2	D1	D0
0000 ~ 07FF	2k byte	2716 EPROM	MAIN PROGRAM 1 (TLC-1)							
0800 ~ 0FFF	2k byte	2716 EPROM	MAIN PROGRAM 2 (TLC-2)							
1000 ~ 100F	16 digit	2101 RAM					REC VTR TC DATA			
1800 ~ 180F	16 digit	2101 RAM					PLAYER-A VTR TC DATA			
2000 ~ 200F	16 digit	2101 RAM					PLAYER-B VTR TC DATA			
2800	6 bit	LS373 TTL	SW & GENERATOR TIMING		NORM/CHECK	DF/NDF	LG	LF	LE	LD
3000	3 bit	LS373 TTL	TC FLAG INPUT					PL-B VTR	PL-A VTR	REC VTR
3800 ~ 381C	29 byte	LS373 TTL	TLC DATA INPUT TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0
4000 ~ 401F	32 byte	LS377 TTL	TLC DATA OUTPUT TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
4800	3 bit	LS377 TTL	TC FLAG OUTPUT					PL-B VTR	PL-A VTR	REC VTR
5000 ~ 500A	10 byte	LS377 TTL	GENERATOR DATA OUTPUT							
5800	4 bit	8214 INTERRUPT CONTROLLOR	CURRENT STATUS RESISTER				SGS	B_2	B_1	B_0
6000	1 bit	LS74 TTL	INTERRUPT OUTPUT to SYS WR: 0 RD: 1							
6800 ~ 6BFF	1k byte	2114 RAM	WORKING RAM							
7000 ~ 77FF	2k byte		BLANK							
7800 ~ 7FFF	2k byte	2716 EPROM	TEST PROGRAM for CHECK							

Table 7-11-4 Memory Map

5 Main Program ROM (Addresses are 0000_H to $OFFF_A$)

The software of the TLC board is contained in two 2716 EPROMs (TLC-1 and TLC-2) each of which has a memory capacity of 2 kilobytes.

The software of the TLC board comprises a 57-byte main routine and eight interrupt routines. As its name inplies, the time code data handled by the TLC board restricts data input and output so that time is controlled by interrupts. The eight interrupt routines have the following priorities:

1) FRAME CLOCK INTERRUPT ROUTINE (Started by $\overline{\text{INTI}}$)

2) GENERATOR INTERRPUT ROUTINE (Started by $\overline{\text{INT2}}$)

3) RECORDER (VTRI) TIME CODE INTERRUPT ROUTINE (Started by $\overline{\text{INT3}}$)

4) PLAYER-A (VTR2) TIME CODE INTERRUPT ROUTINE (Started by $\overline{\text{INT4}}$)

5) PLAYER-B (VTR3) TIME CODE INTERRUPT ROUTINE (Started by $\overline{\text{INT5}}$)

6) RECORDER (VTR1) CTL INTERRUPT ROUTINE (Started by $\overline{\text{INT6}}$)

7) PLAYER-A (VTR2) CTL INTERRUPT ROUTINE (Started by $\overline{\text{INT7}}$)

8) PLAYER-B (VTR3) CTL INTERRUPT ROUTINE (Started by $\overline{\text{INT8}}$)

NOTE: Figure 7-87 gives the algorithm for time code corrections

READ DATA (D-AREA)	$D_{i-1}+1$ (B-AREA)	CORRECTED DATA (A-AREA)	COUNTER-A (D = A)	COUNTER-B (D = A, D = B)	COMMENTS
15	15	15	0	0	
16	+1 16	+1 16	0	0	
17	17	17	0	0	
18	18	18	0	0	
7	19	19	1	0	
5	8	20	2	0	
9	6	21	3	0	BURST ERROR MODE
20	10	22	4	0	
100	21	23	5	0	
101	101	24	6	1	
102	102	25	7	2	
103	103	26	8	3	
104	104	27	9	4	
105	105	28	10	4	JUMP MODE
106	106	29	11	6	
107	107	30	12	7	
108	108	31	13	8	
109	109	32	14	9	
110	110	110 33	15	10	
111	111	+1 111	0	0	
112	112	112	0	0	
113	113	113	0	0	
114	114	114	0	0	
115	115	115	0	0	
100	116	116	1	0	
200	101	117	2	0	BURST ERROR MODE
358	201	118	3	0	
119	359	119	0	0	
120	120	120	0	0	

Figure 7-87 Algorith for time code corrections

6 WORKING RAM (Address 6800_H to $6BFF_A$)

This has a working area of one kilobyte comprising two static RAMs 2114 (8114) with a capacity of 4 bits X 1k.

7 TLC DATA I/O

This is an I/O FF for transfer of data between the TLC and SYS boards. TC0 to TC7 are outputs to supply VTR time code values (excluding user's bits) VTR commands, and flags indicating an AUTO LOCATE state to the SYS board. SYNC is supplied to derive timings for receiving this data at the SYS board. (Addresses 3800_H to $381C_H$)

TG0 to TG7 are time code inputs for VTR auto locate target edit points, setting generator (including user's bits), and flangs to show the VTRs status and auto locate and edit states. (Addresses 4000_H to $401F_H$)

8 INTERRUPT CONTROLLER

This block consists of two circuits. One is an interrupt circuit to the SYS Board, and the other is an interrupt circuit for the CPU On the TLC board.

8a) SYS Board interrupt generator.

The setting and resetting of this FF is controlled by software. (Addresses 6000_H)

8b) CPU Interrupt controller

As shown in Figure 7-88, this circuit comprises two 4-bit FFs (74LS279X2) to latch 8-level interrupt signals $\overline{\text{INT1}}$ to INT8, PICU (priority interrupt control unit) to encode latched signals in order of priority and to output as CPU interrupts, an 8-bit FF(8212) to hold encoded signals until the CPU acknowledges interrupts and to output these signals to the CPU data bus, and a 3 8 decoder (74LS138) to reset the interrupt latch circuit.

The 8-level interrupts $\overline{\text{INT1}}$ through $\overline{\text{INT8}}$ are latched in the FFs (IC-D6, D7) until input to PICU (IC-C7). PICU encodes the highest priority input and compares it with the contents of the current status register (CSR) set by the software inside PICU. An INTERRUPT PULSE is generated if the priority is higher than CSR contents and simultaneously the encoded interrupt is output. The $\overline{\text{INTERRUPT PULSE}}$ is a very narrow active-low pulse and turns the $\overline{\text{INT}}$ signal of the next

8-bit FF (8212) to low by its trailing edge, latching the encoded data.

IC-C5 turns the CPU interupt signal $\overline{INT}$ low and waits for the interrupt acknowledge signal from the CPU. IC-C5 adds five bits to the three bit interrupt encoded at the CPU data bus to supply a total of eight bits (interrupt vector) read by the CPU, at the same time resetting $\overline{INT}$ to high. The encoded 3-bit signal is decoded by IC-D5, and the interrupt signals acknowledged by the CPU from the latched interrupt signals are reset in the latch FF to high.

The CPU interrupt acknowledge signal sets the interrupt priority acknowledged in the beginning of the interrupt routine in the PICU CSR, and PICU acknowledges only those interrupts whose priority is higher than that of the interrupt routine currently processing. At the end of this interrupt routine, acknowledging more interrupts, the priority is set in the PICU CSR so that interrupts are performed according to priority. On this board, the setting of CPU interrupts in Mode 2 and 00_H is set in the interrupt register (I register).

Table 7-11-6 shows the relationship between interrupts and interrupt addresses:

The addresses of the PICU CSR is 5800H, and the lower four bits are used as data.

$\overline{SGS}$ always sets 0.

Three bits, $\overline{B_2}$ to $\overline{B_0}$ control the data priority from PICU, For instance, by setting

$\overline{SGS} = 0$

$\overline{B_2} = 0$

$\overline{B_1} = 0$

$\overline{B_0} = 0$

$\overline{INT4}$ through $\overline{INT8}$ no longer accept interrupts.

Table 7-11-6 Interrupt Addresses

Interrupts	I Register Contents								Interrupt Vectors							
	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
$\overline{INT1}$	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
$\overline{INT2}$	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
$\overline{INT3}$	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
$\overline{INT4}$	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
$\overline{INT5}$	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
$\overline{INT6}$	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0
$\overline{INT7}$	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
$\overline{INT8}$	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

High Priority (INT1) ↔ Low Priority (INT8)

These three bits (A_3, A_2, A_1) are output by PICU

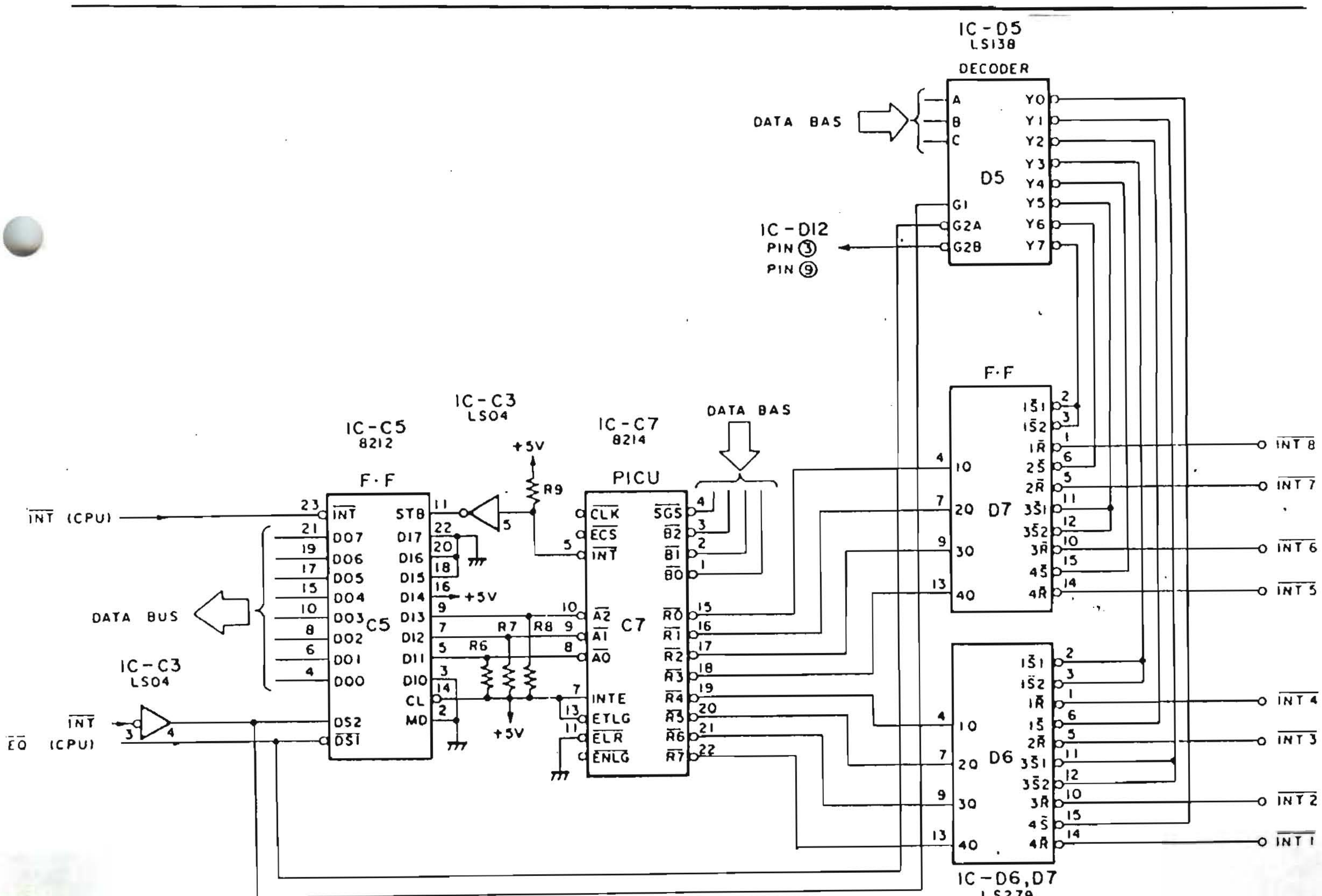
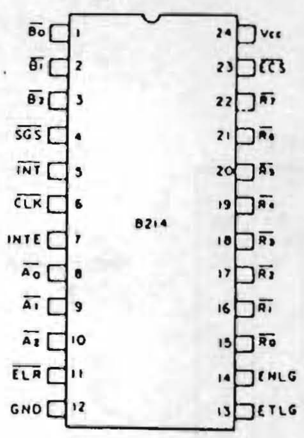
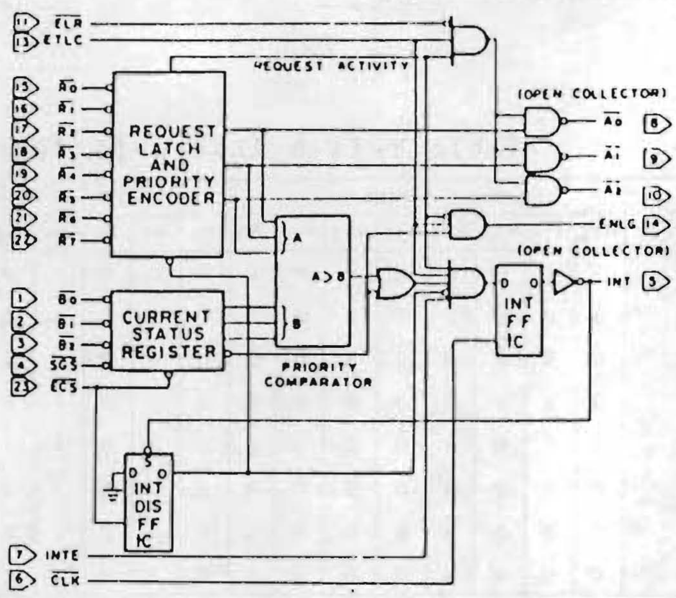


Figure 7-88 Interrupt Controller

PIN CONFIGURATION



LOGIC DIAGRAM

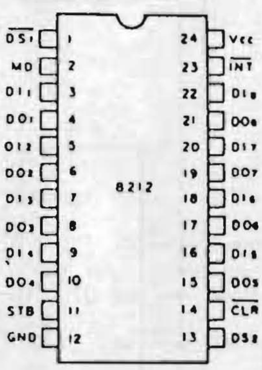


PIN NAMES

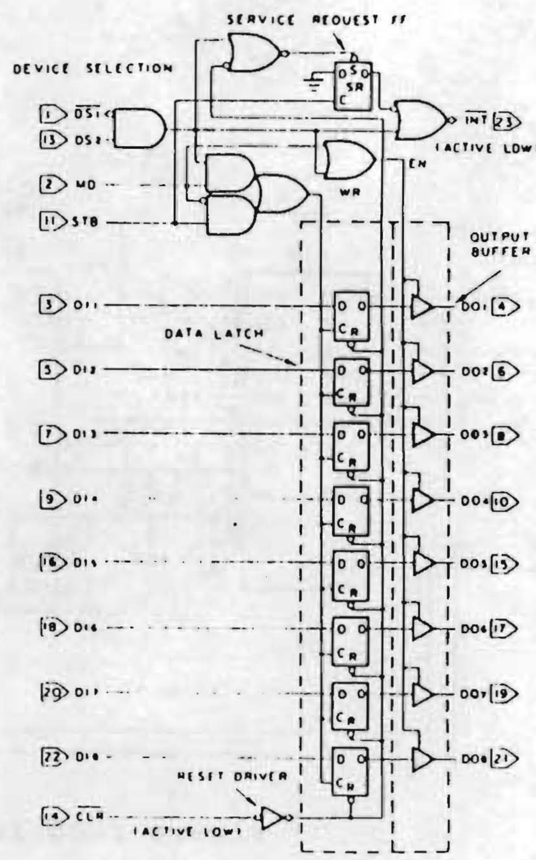
INPUTS	
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS
$\overline{SGS}$	STATUS GROUP SELECT
$\overline{ECS}$	ENABLE CURRENT STATUS
INTE	INTERRUPT ENABLE
$\overline{CLK}$	CLOCK (INT F-F)
$\overline{ELR}$	ENABLE LEVEL READ
ETLG	ENABLE THIS LEVEL GROUP
OUTPUTS	
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS } OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT LOW) } OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP

Figure 7-89 8214 Priority Interrupt Control Unit

PIN CONFIGURATION



LOGIC DIAGRAM



PIN NAMES

DI_1 - DI_8	DATA IN
DO_1 - DO_8	DATA OUT
$\overline{DS_1}$ - DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

Figure 7-90 8212 8-bit I/O Port

A clock (GCK) locked to $\overline{\text{RFCK}}$ is made from the $\overline{\text{RFCK}}$ INPUT by the EDT board and frame synchronized with a PLL circuit and a 160 counter, which is formed with hexadecimal and a decimal counter in series. The generator timings are formed from the outputs (1/2 LA to LG) of the 160 counter. (Refer to Figure 7-92)

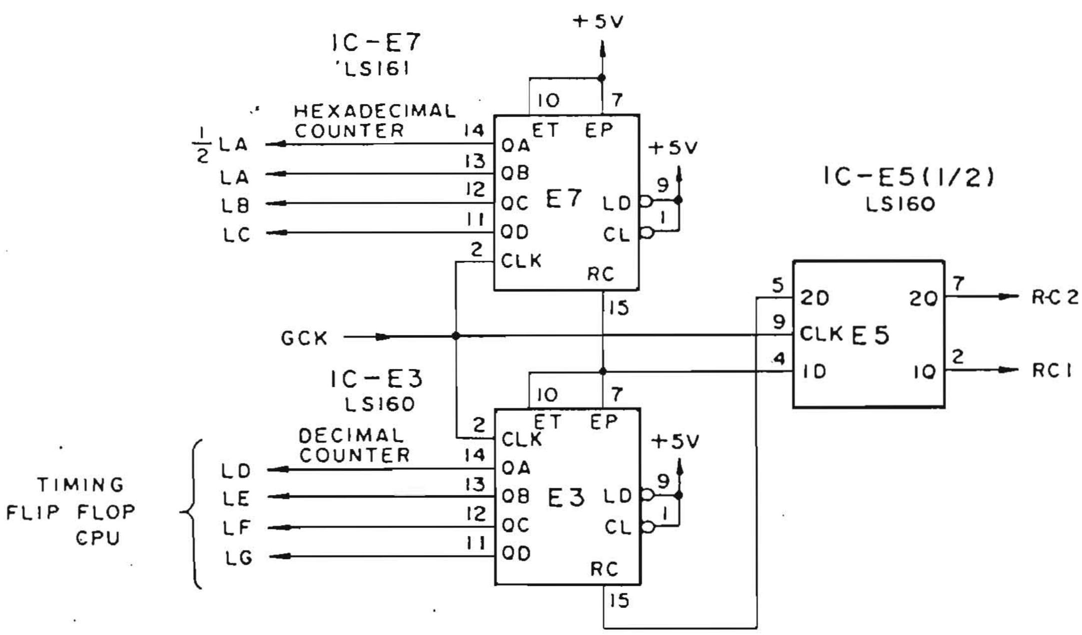


Figure 7-92 Timing Circuit

RC1 is a pulse appearing ten times per frame. $\overline{\text{INT2}}$ is produced from the rising edge of RC1. $\overline{\text{INT1}}$ is produced from the training edge of $\overline{\text{RFCK}}$.

$\overline{\text{INT2}}$ alone does not provide position information on the exact slot in the frame (ten slots). LD through LG data is supplied to the CPU through the timing flip flop. The CPU refers to LD though LG and sends generator data; depending on whether LD is "L" or "H" in the hardware section they are latched by A12 and A13, respectively.

LG	LF	LE	LD	OUT DATA	LATCH FLIP-FLOP
0	0	0	0	SECOND	A12
0	0	0	1	U_1	A13
0	0	1	0	MINUTE	A12
0	0	1	1	U_2	A13
0	1	0	0	HOUR	A12
0	1	0	1	U_3	A13
0	1	1	0	1111 1100	A12
0	1	1	1	1011 1111	A13
1	0	0	0	FRAME	A12
1	0	0	1	U_0	A13

Time Code Counter Table

When 16-bit data is latched by IC-A12 and IC-A13 the data is loaded in a parallel-in, serial-out shift register, to become a serial NRZ signal. This signal produces a bi-phase OUTPUT signal.

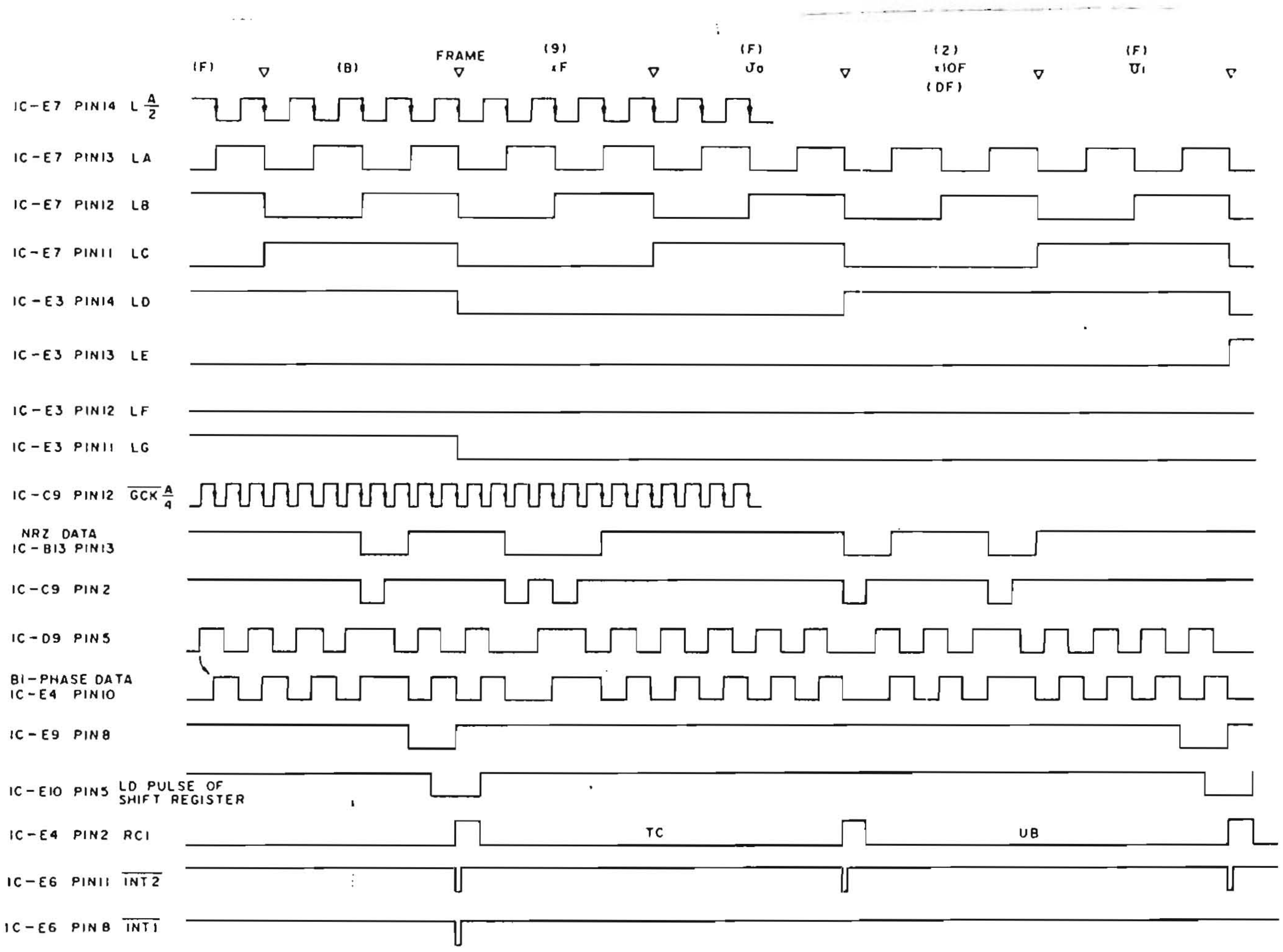


Figure 7-93 Timing of Timecode Generator

11 REC VTR Time Code Data Separator

In this block the bit clock is extracted from the time code signals obtained by converting time code signals from the VTRs into TTL Level on the EDT Board. Data and SYNC are separated by this bit clock.

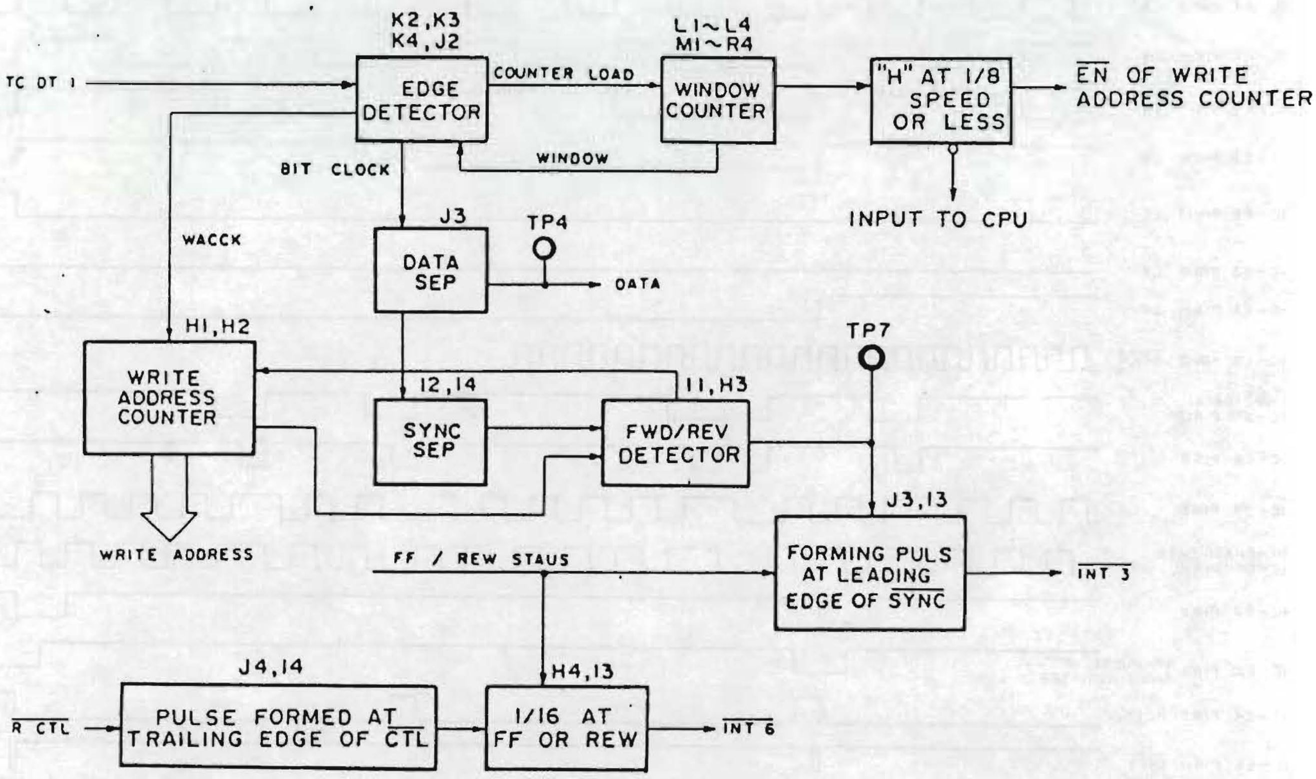


Figure 7-94 REC VTR Time Separator

The shift register (IC-K4) and EXCLUSIVE or (IC-K3) locate the edge of time code signal input. (See Figure7-95 IC-K3). The WE signal writes data in the RAMs with the 407 ns pulse from IC-K3 pin 3.

IC-K3 pin 11 outputs clear pulses for the up-counters (IC-M1 to IC-M4) which count data bit intervals, and IC-K3 pin 6 supplies load pulses to preset the output of the up-counters in the down-counters (IC-L1 to IC-L4).

There counters make windows to extract the data bit clocks. The down-counters operate at a frequency 4/3 that of the up-counters. Therefore, the down-counters count down till 0 at a speed of 3/4 of a bit interval and open the gates for the next bit clocks (IC-K2 pin 12). Thus, edges caused by data changes in the center of a bi-phase bit are cancelled.

Therefore, as in the case with IC-J3 pin 9, the extracted data becomes "H" in the center of a bit when 1, remaining "L" when 0, and becomes a waveform cleared by "L" at both edges of the bit.

It is unlikely that "1" will continuously appear in time codes except in SYNC locations. Therefore, by locating a place with twelve consecutive 1's, SYNC can be found (IC-I2, I4). Using the rising edges, a load pulse for the write address counter (WACT) is formed IC-I3 pin 8. Refer to Figure 7-96)

The address counter consists of a hexadecimal and a decimal up-down counter. Counting up is performed during FWD, and counting down, during REV. The following values are loaded:

	LS191 (H1)				LS190 (H2)			
	A	B	C	D	A	B	C	D
FWD	0	1	0	1	1	0	0	1
REV	1	0	1	0	0	0	0	1

RAM WRITE ADDRESS
A_0 A_1 A_2 A_3

RAM Write Addressing

Therefore, the output from IC-H2 QD will become "L" after counting six clocks of WACCK: FWD will result if data is

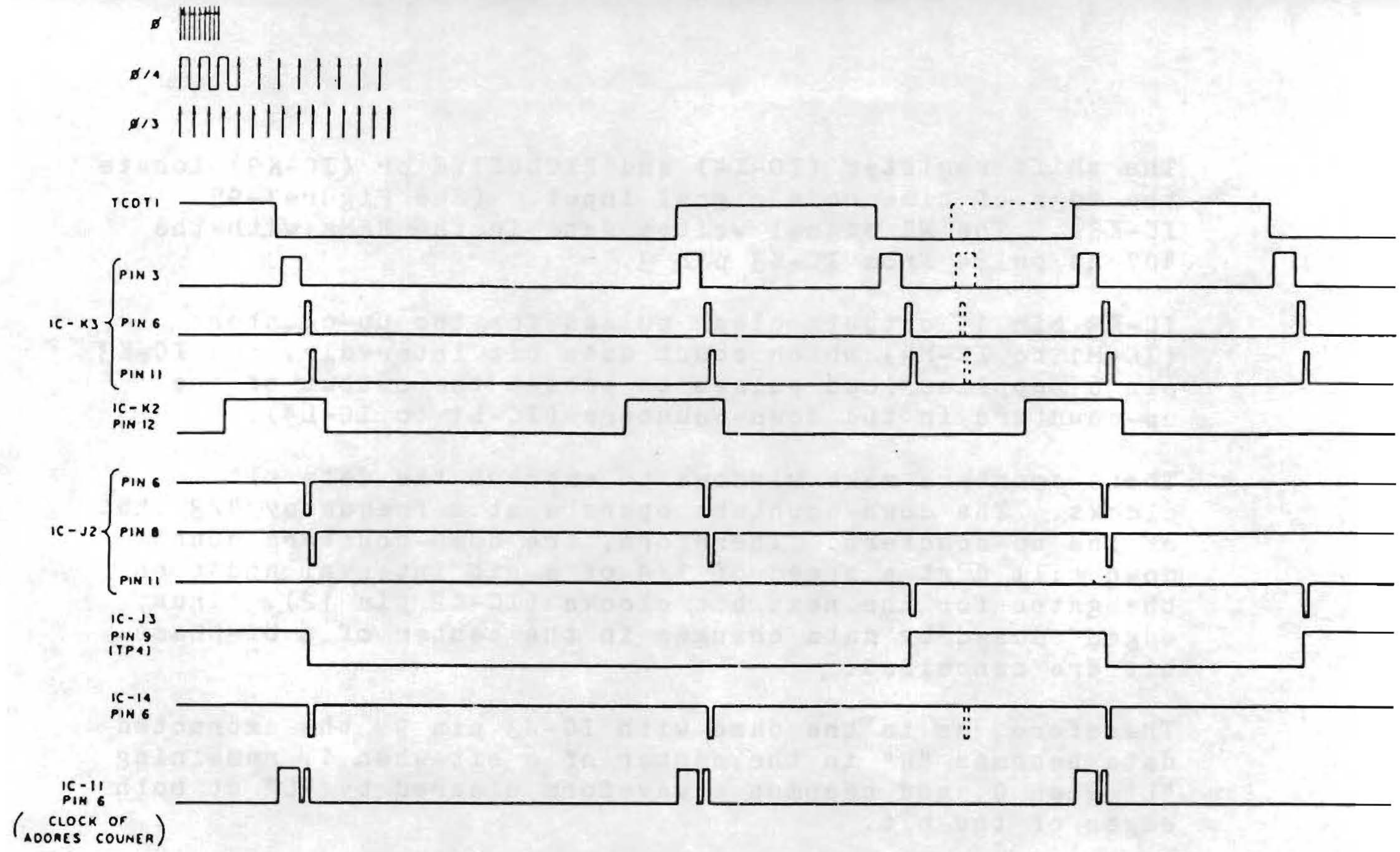


Fig. 2-6-10. Timing of REC VTR time code data separator (1)

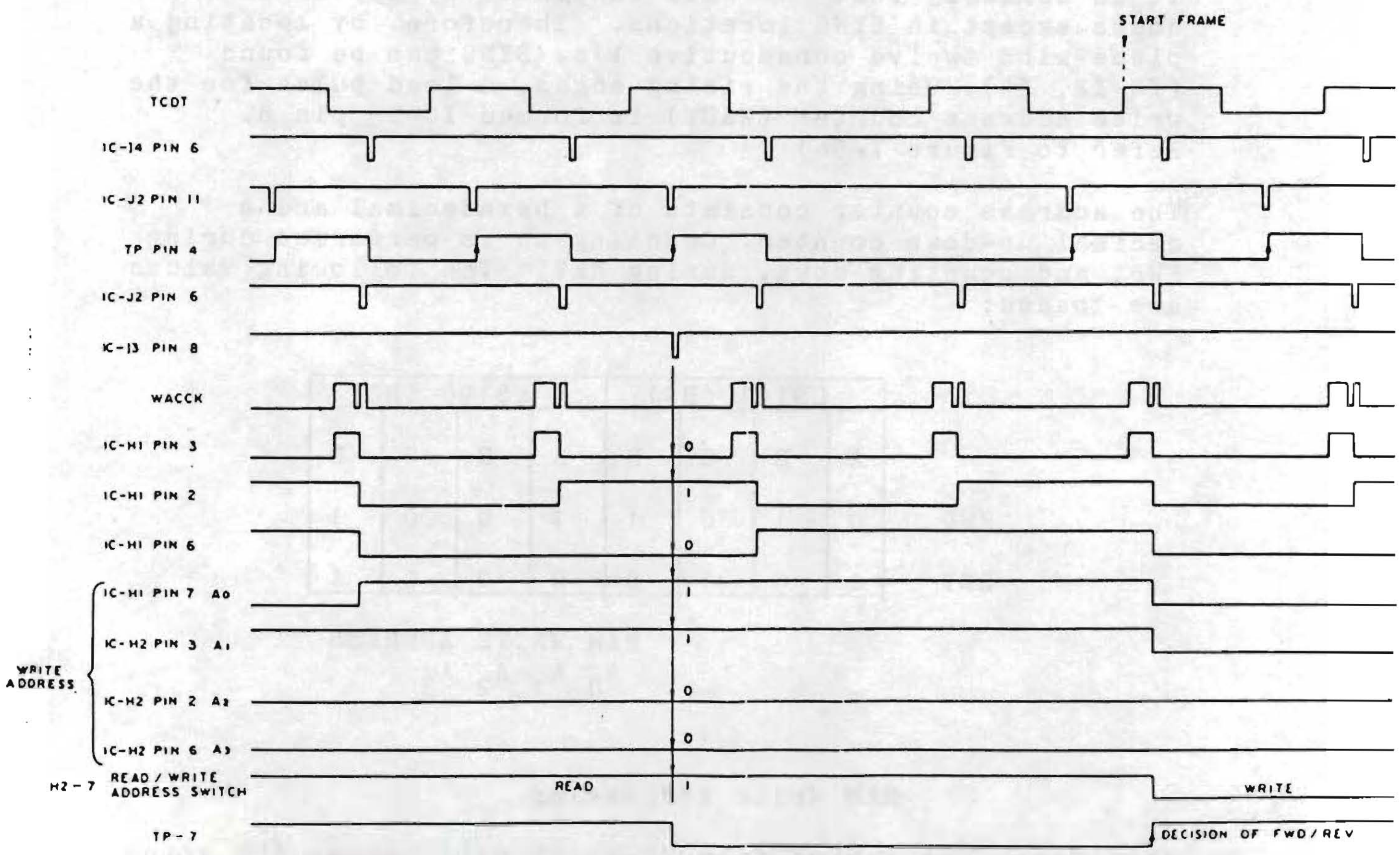


Figure 7-96 Timing for REC VTR Timecode Data Separator

"H" at the trailing edge, while REV will result if data is "L". (The rising edge of TP7 corresponds to this trailing edge.) $\overline{\text{INT3}}$ is made from the rising edge of TP7.

The write addresses A_0 to A_3 becomes all "0"s during FWD, and all "1"s during REV, counted up and down, respectively. In FWD or in REV, pre-decided time codes are written in pre-decided addresses.

WACT counting stops, and data is prohibited from the RAMs when the VTR speed drops below 1/8, or when time code data is exhausted.

16 time code SYNC Bits are arranged as shown below:

DATA <- | 0 0 1 1 1 1 1 1 1 1 1 1 1 1 0 1 | -> DATA

12 consecutive 1s

Start Frame

REV if 0 FWD if 1

12 PLAYER-A VTR Code Data Separator

The same as #11 (REC VTR Time Code Data Separator).

13 PLAYER-B VTR Code Data Separator

The same as #11 (REC VTR Time Code Data Separator).

14 REC VTR Time Code RAM

As shown in Figs. 7-97 and 7-98. two RAMs are available in this block, and they alternately read and write, permitting the CPU to read at all times.

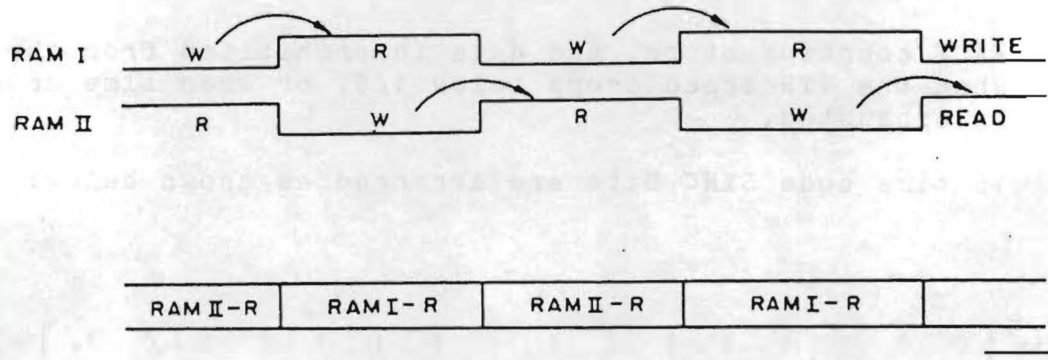


Figure 7-97 RAM Read and Write Cycles

A capacity of 4 bits x 16 for the RAMs is sufficient. However, RAMs with a capacity for 4 bits x 256 are used.

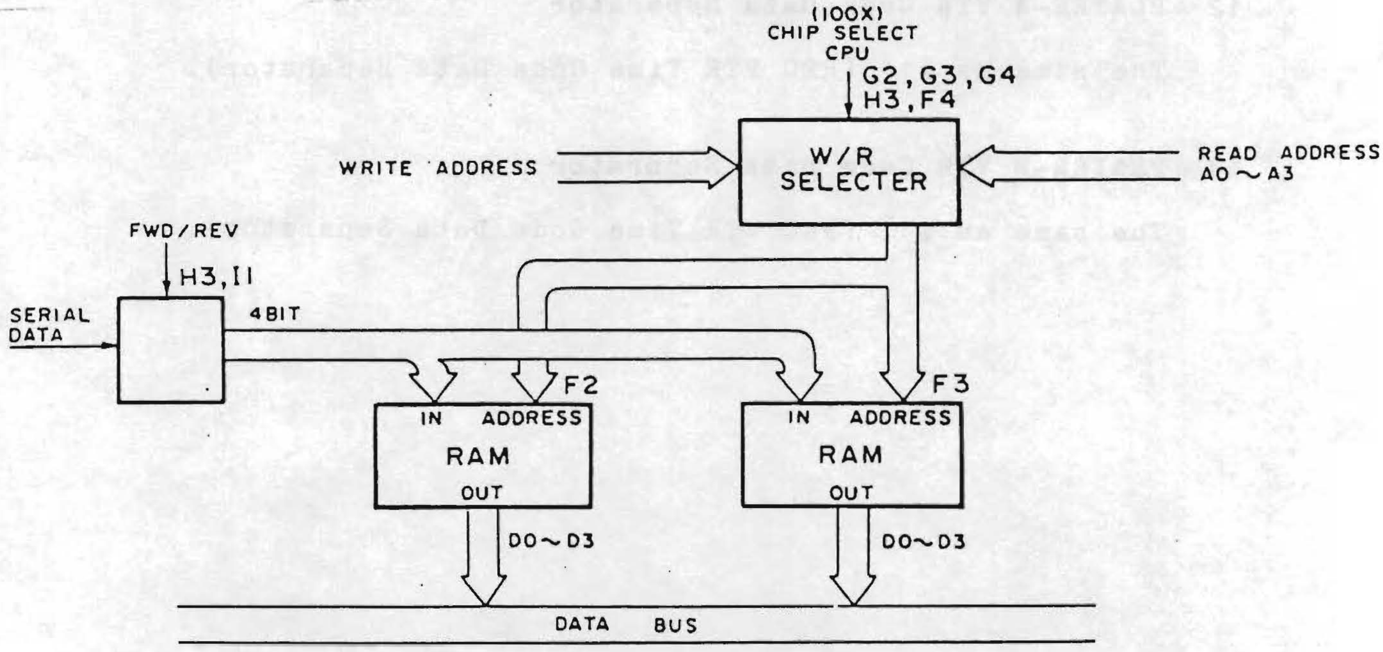


Figure 7-98 REC VTR Timecode RAM

15 PLAYER-A VTR Time Code RAM

The same as #14 (REC VTR TIme Code RAM).

16 PLAYER-B VTR Time Code RAM

The same as #14 (REC VTR TIme Code RAM).

7.12 SYSTEM CONTROL CIRCUIT (SYS BOARD)

7.12.1 General

This circuit generates the remote control signals for the VTR corresponding to the switch data from the keyboard of the DAE-1100 and it outputs control or operating signals to the digital signal processing block and edit control block. The generation of these control signals is based on the SMPTE time code and consequently there is a time code input from the Time Code Board (TLC Board).

The keyboard time display and function display data is also output through the system control circuit. The remote control input and outputs are intended for the professional type U-matic VTR. The control signals, operation data and display data are generated by a Z-80 microprocessor and are output via the I/O ports.

7.12.2 Configuration

Figure 7-99 shows a block diagram of the system control circuit. The switch signals from the keyboard are input to the system control circuit but are as shown in Figure7-100 strobed into the circuit relative to the Transmission Sync (SYNC: f_{SYNC} =37.5 Hz) and Transmission Clock (CKTRS: f_T = 9600 Hz).

Signal transmission between the keyboard and the editor itself is in the form of a differential signal conforming to the EIA Standard RS-422 driver/receiver protocol. The input switch signal is encoded in a form that can be input to the microprocessor. This 8-bit data (d_0 - d_7) corresponds to the keyboard functions as shown in Table 7-12-1.

The switch signal generates an interrupt to the CPU and the encoded switch data is fetched from the data bus by the CPU, decoded and the appropriate commands are output via the output port.

The time code and Auto Locate signals etc are synchronized by software and transmitted and received between TLC Boards; to do this the instruction cycle time for the CPUs on both boards has to be the same. To facilitate this the System Control Circuit is supplied with a half-frequency master clock form the TLC Board.

The clocks are related as follows:

Master Clock: f_o = 9.8304mHZ

CPU Clock: $f_{CPU} + F_{004}$ = 2.4576 mHz

Transmission Clock to keyboard:

$$f_T = f_{CPU/256} = f_{o/1024} = 9600 \text{ Hz}$$

Transmission Sync to keyboard:

$$f_{SYNC} = f_{T/256} = f_{o/262144} = 37.5 \text{ Hz}$$

The response time to the EDIT POINT and Search Mode's manual signals has to be very fast. As shown in Table 7-12-1, data is transmitted during a period of 1.67msec every 16 slots, and so control is not performed by software but by a hardware circuit. Data for the keyboard display is output by the CPU and stored temporarily in the display RAM. It is clocked out to the keyboard by the transmission clock.

The output of the GAIN OFFSET FADER on the keyboard is 8 bits (correspondingly to 256 positions) and this is transmitted serially synchronously with SYNC and CKTRS as shown in Figure 7-100. This serial fader data is converted to parallel data in the System Control Circuit (SC-A Board) and then parallel data is transferred to Search control Circuit (SC-A Board). The recorders, player A and player B require I/O ports for the VTR remote control outputs and status inputs. These output ports latch the data from the data bus of CPU and supply the signals to the remote control drivers.

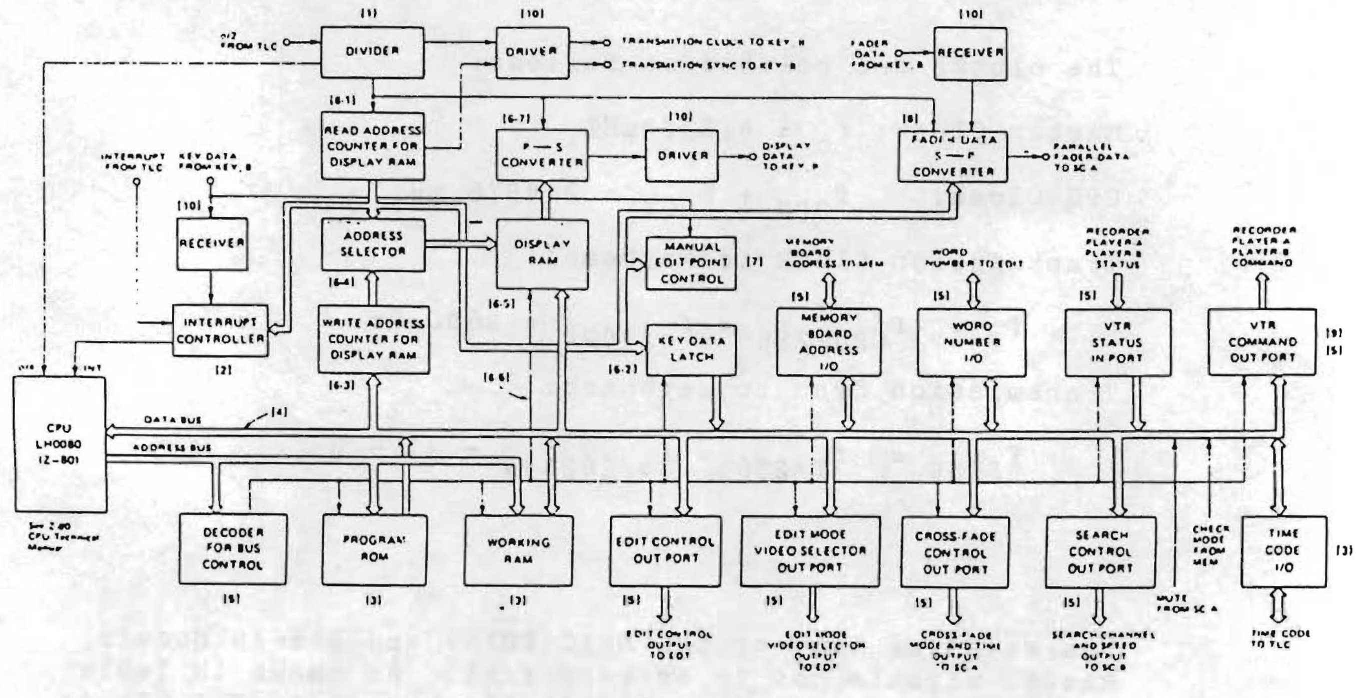
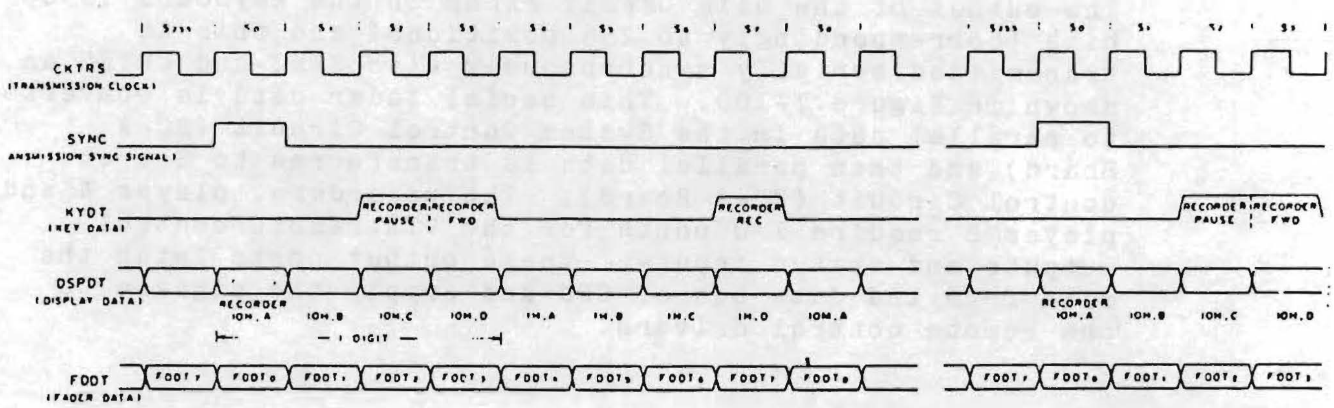


Figure 7-99 System Control Circuit Block Diagram



Note: • The KYDT shown is when the PAUSE, FWD or REC keys have been pressed.

• SRCCK1 and SRCCK2 are output without any timing relationship with CKTRS or SYNC.

Figure 7-100 Timing Chart

d7 ~ d5 / ~ d0	RECORDER 0 0 0	PLAYER A 0 0 1	PLAYER B 0 1 0	EDIT KEY 0 1 1	TEN KEY 1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0	STOP	STOP	STOP	PLAYER	TEN KEY 0			
0 0 0 1	PAUSE	PAUSE	PAUSE	RECORDER	1			
0 0 1 0	FWD	FWD	FWD		2			
0 0 1 1	REVERSE	REVERSE	REVERSE		3			
0 1 0 0	FF	FF	FF	PREVIEW	4			
0 1 0 1	REW	REW	REW	REVIEW	5			
0 1 1 0	REC (CUT IN)	REC	REC	AUTO EDIT	6			
0 1 1 1	AUTO LOCATE	AUTO LOCATE	AUTO LOCATE		7			
1 0 0 0	CUT OUT			P.R.T 5sec	8			
1 0 0 1	EDIT			P.R.T 10sec	9			
1 0 1 0				P.R.T 30sec	READER AUTO LOCATOR			
1 0 1 1					CLEAR			
1 1 0 0		PLAYER A	PLAYER B	IN				
1 1 0 1				OUT				
1 1 1 0	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT
1 1 1 1	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL
0 0 0 0	ASSEMBLE			SEARCH SPEED ×1/2				
0 0 0 1	INSERT VIDEO			SEARCH SPEED ×1				
0 0 1 0	ANALOG CH1							
0 0 1 1	ANALOG CH2							
0 1 0 0	SPEED ×1	SPEED ×1	SPEED ×1	SEARCH MONITOR MIX				
0 1 0 1	SPEED ×2	SPEED ×2	SPEED ×2	SEARCH MONITOR CH1				
0 1 1 0	SPEED ×1/5			SEARCH MONITOR CH2				
0 1 1 1								
1 0 0 0	READER	READER	READER	CROSS FADE UP				
1 0 0 1	USER'S BIT	USER'S BIT	USER'S BIT	CROSS FADE DOWN				
1 0 1 0	AUTO LOCATOR	AUTO LOCATOR	AUTO LOCATOR					
1 0 1 1	GENERATOR							
1 1 0 0	HOLD							
1 1 0 1								
1 1 1 0	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT
1 1 1 1	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL

Note: d_0 – d_7 correspond to address lines A_1 – A_8 in the circuit diagram.

Table 7-12-1 Key Information

d7 ~ d5 / d4 ~ d0	RECORDER TIME DISP 0 0 0	PLAYER A TIME DISP 0 0 1	PLAYER B TIME DISP 0 1 0	SEARCH DIAL DISP 0 1 1	KEY LED 1 0 0	KEY LED 1 0 1	KEY LED 1 1 0	1 1 1
0 0 0 0 0	10H, A	10H, A	10H, A	SEARCH, P0	RECORDER STOP	PLAYER STOP	EDIT IN	
0 0 0 0 1	B	B	B	P1	PAUSE	PAUSE	EDIT OUT	
0 0 0 1 0	C	C	C	P2	FWD	FWD	RECORDER	
0 0 0 1 1	D	D	D	P3	REVERSE	REVERSE	PLAYER	
0 0 1 0 0	1H, A	1H, A	1H, A	P4	FF	FF		
0 0 1 0 1	B	B	B	P5	REW	REW		
0 0 1 1 0	C	C	C	P6	REC	REC	SEARCH	
0 0 1 1 1	D	D	D	P7	AUTO LOCATE	AUTO LOCATE		
0 1 0 0 0	10M, A	10M, A	10M, A	P8	SPEED ×2	SPEED ×2	SEARCH MONITOR MIX	
0 1 0 0 1	B	B	B	P9	SPEED ×1	SPEED ×1	SEARCH MONITOR CH1	
0 1 0 1 0	C	C	C	P10	SPEED ×1/5	READER	SEARCH MONITOR CH2	
0 1 0 1 1	D	D	D	P11		USER'S BIT	SEARCH SPEED MANUAL	
0 1 1 0 0	1M, A	1M, A	1M, A	P12	ASSEMBLE	AUTO LOCATOR	SEARCH SPEED ×1	
0 1 1 0 1	B	B	B	P13	ANALOG CH2	PLAYER A	SEARCH SPEED ×1/2	
0 1 1 1 0	C	C	C	P14	ANALOG CH1	TIME CODE		
0 1 1 1 1	D	D	D	P15	VIDEO	SERVO		
1 0 0 0 0	10S, A	10S, A	10S, A	P16	GENERATOR	PLAYER B STOP	PREVIEW	
1 0 0 0 1	B	B	B	P17	* HOLD	PAUSE	AUTO EDIT	
1 0 0 1 0	C	C	C	P18	READER	FWD	REVIEW	
1 0 0 1 1	D	D	D	P19	USER'S BIT	REVERSE	F.R.T 5sec	
1 0 1 0 0	1S, A	1S, A	1S, A	P20	AUTO LOCATOR	FF	F.R.T 10sec	
1 0 1 0 1	B	B	B	P21		REW	F.R.T 30sec	
1 0 1 1 0	C	C	C	P22	TIME CODE	REC	TIME OFFSET IN	
1 0 1 1 1	D	D	D	P23	SERVO	AUTO LOCATE	TIME OFFSET OUT	
1 1 0 0 0	10F, A	10F, A	10F, A	P24		SPEED ×2	CROSS FADE 10msec A	
1 1 0 0 1	B	B	B	P25		SPEED ×1	B	
1 1 0 1 0	C	C	C	P26		READER	C	
1 1 0 1 1	D	D	D	P27		USER'S BIT	D	
1 1 1 0 0	1F, A	1F, A	1F, A	P28	*RECORDER NON-DROP-FRAME	AUTO LOCATOR	1msec A	
1 1 1 0 1	B	B	B	P29	*PLAYER A NON-DROP-FRAME	PLAYER B	B	
1 1 1 1 0	C	C	C	P30	*PLAYER B NON-DROP-FRAME	TIME CODE	C	
1 1 1 1 1	D	D	D	P31	0 dB	SERVO	D	

Note: 1. d_0 – d_7 correspond to address line A_1 – A_8 in the circuit diagram.
2. HOLD block lights up the 7-segment of LED's display.
3. REC N·D·F block lights up the 1-segment of LED's display.
4. PLA N·D·F block lights up the 1-segment of LED's display.
5. PLB N·D·F block lights up the 1-segment of LED's display.

Table 7-12-2 Display Information

7.12.3 CIRCUIT DESCRIPTION

7.12.3.1 THE CLOCK CIRCUIT

As data is passed between the SYS Board and the TLC Board, the CPUs on the two boards have to have the same instruction cycle time and for this purpose CK2CPU (=4.9152mHz) is supplied from the TLC Board. The CPU clock (CKCPU =2.4576mHz) and the keyboard editor transmission clock (CKTRS = 9.6kHz) are derived from this signal.

The division ratios and circuit configuration are shown in Figure 7-101.

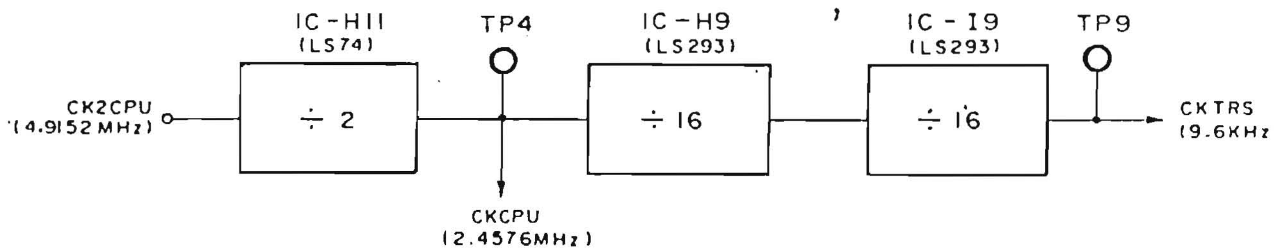


Figure 7-101 Clock Dividing Circuit

7.12.2.2 THE CPU INTERRUPT CONTROL CIRCUIT

There are two types of interrupt to the CPU: the frame period (1/30sec) time code interrupt from the TLC Board and the transmit KEY DATA interrupt from the keyboard. The time code interrupt has been given the higher priority. The CPU interrupt control circuit is shown in Figure 7-102.

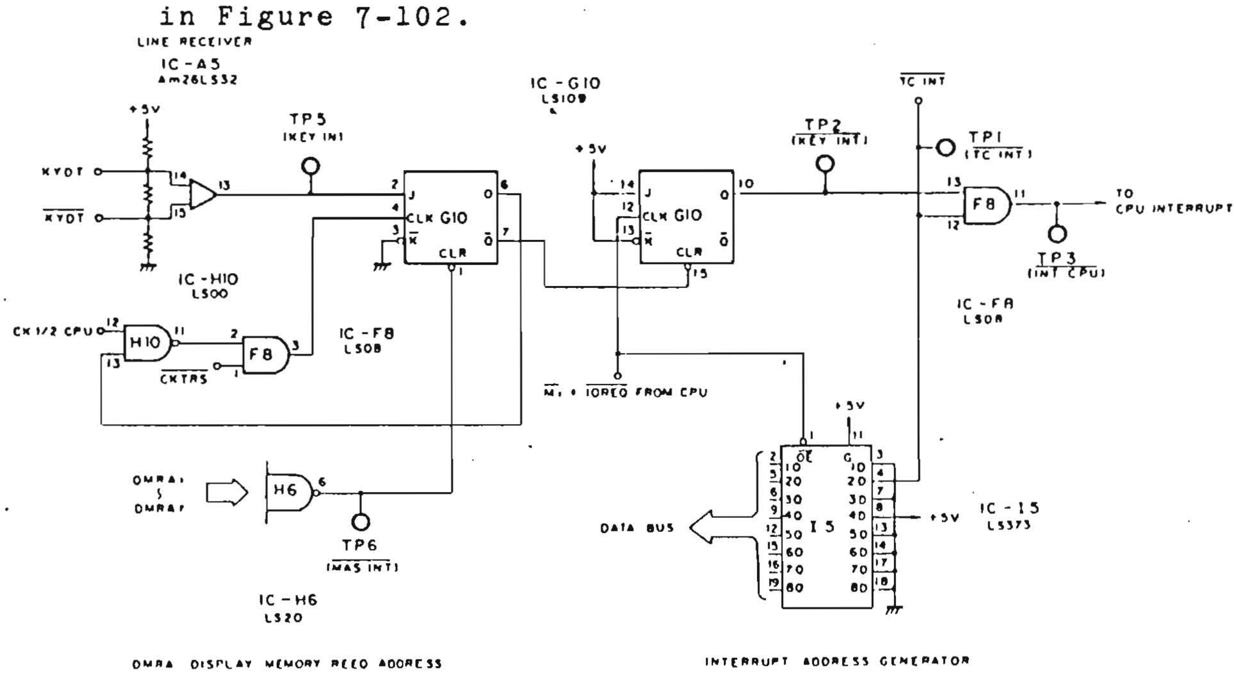


Figure 7-102 CPU Interrupt Control Circuit

The time code interrupt, TCINT, is output from the TLC Board. The interrupr address is set at 0008H and the lower 08H is output to the data bus from the interrupt address generator, IC-I5 (SN74LS373). This timing chart is outputing at M_1 + IOREQ Of CPU Board. The upper 00H of the interrupt address is generated by software in the I Timing for the KEY DATA Interrupts is given in Figure 7-100 Each function is assigned and encoded data is obtained from the Read Address Counter. If the function keys on the keyboard are pressed, the KEY DATA is sent synchronously and it is from this signal that the interrupt control signal to the lower A0H being output by IC-I5 (SN74LS373). Since it is desirable to respond quickly if EDIT POINT or MANUAL are pressed on the keyboard, transmission occurs every 16 slots, as shown in Table 2-7-1. A control signal is produced by IC-H6 (SN74LS20) to ensure that an interrupt is generated only on 01101110 (6FH) for the EDIT POINT key and on 01101111 (6FH) for the MANUAL key, not on 0EH, 1EH etc. and 0FH, 1FH etc. for the EDIT POINT and MANUAL Keys respectively. Figure 7-103A, shows the timing when the Recorder Stop key has been pressed and a time code interrupt has be generated.

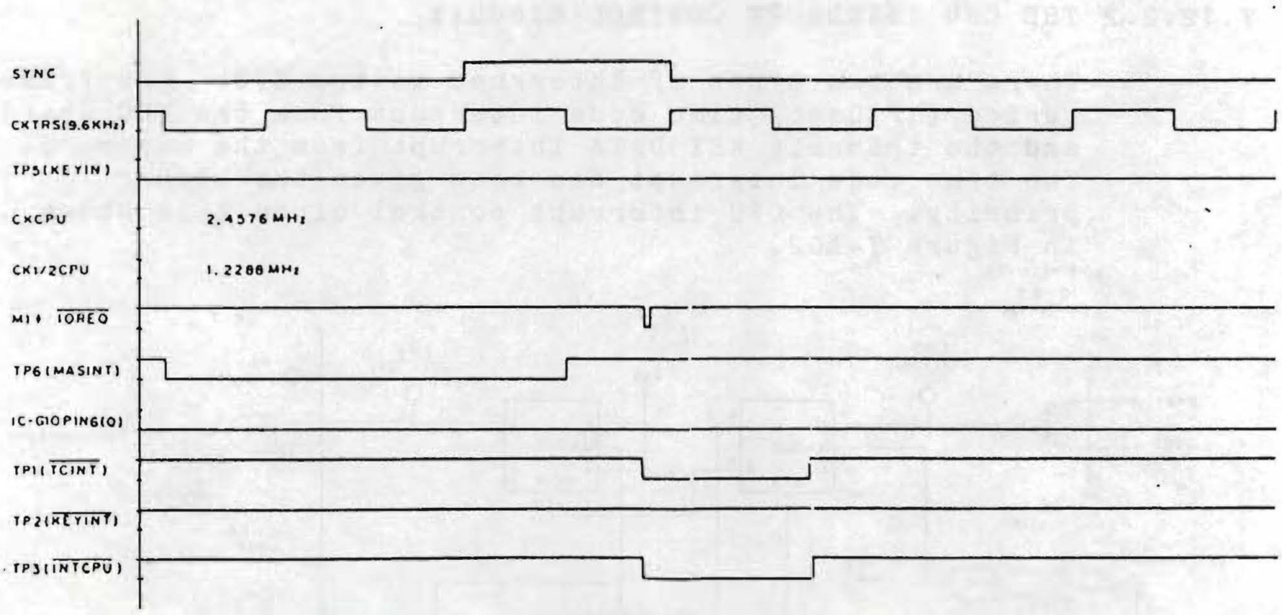


Fig. 2-7-5(A). Shows oscillographs of SYNS, CKTRS, TP5, CK1/2CPU, M1 + I/O REQ, TP6, Q, TP1 and TP3 taken on a logic analyser.

Figure 7-103A Timing Diagram

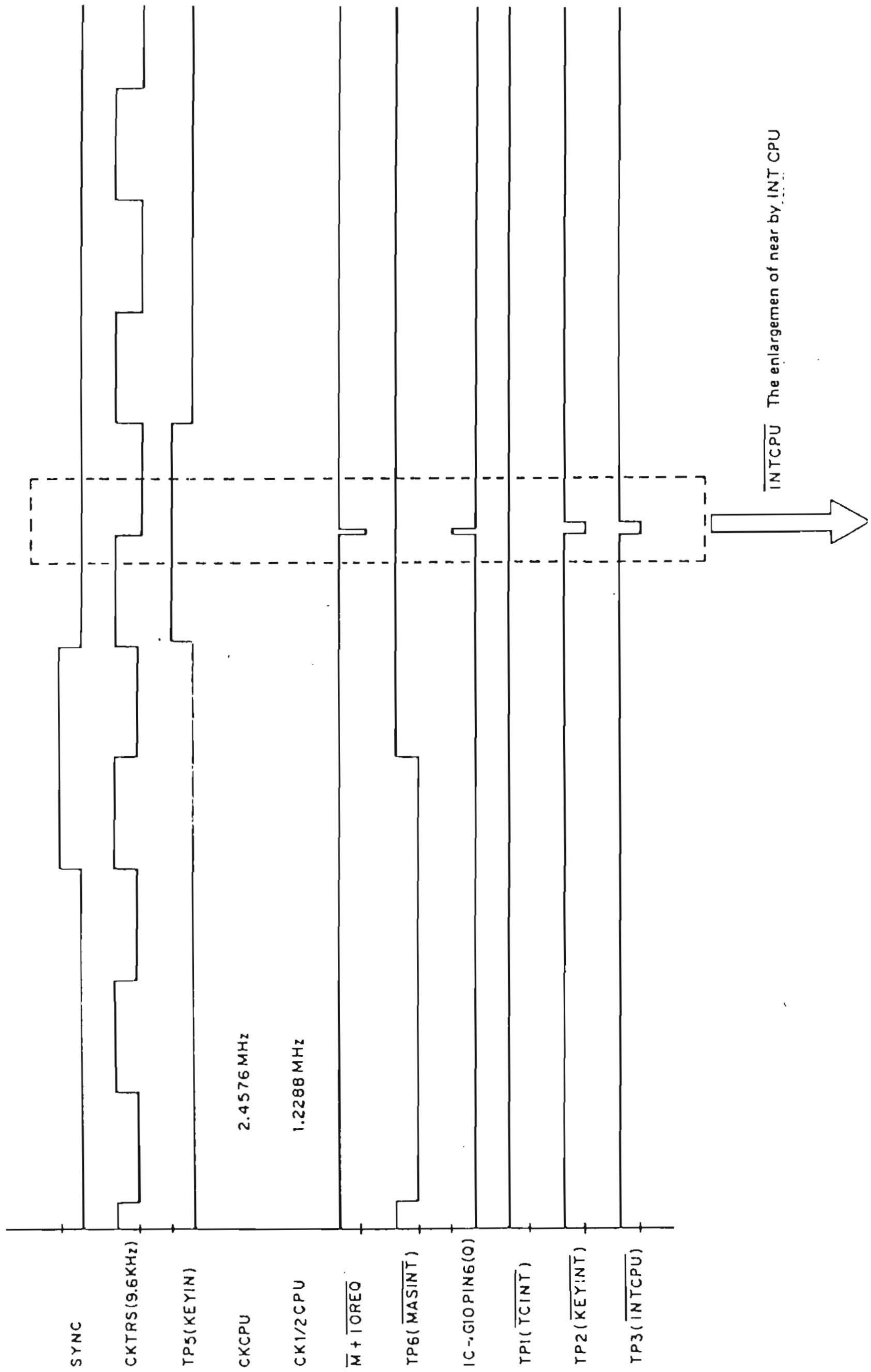


Figure 7-103(B) Timing Diagram (continued)

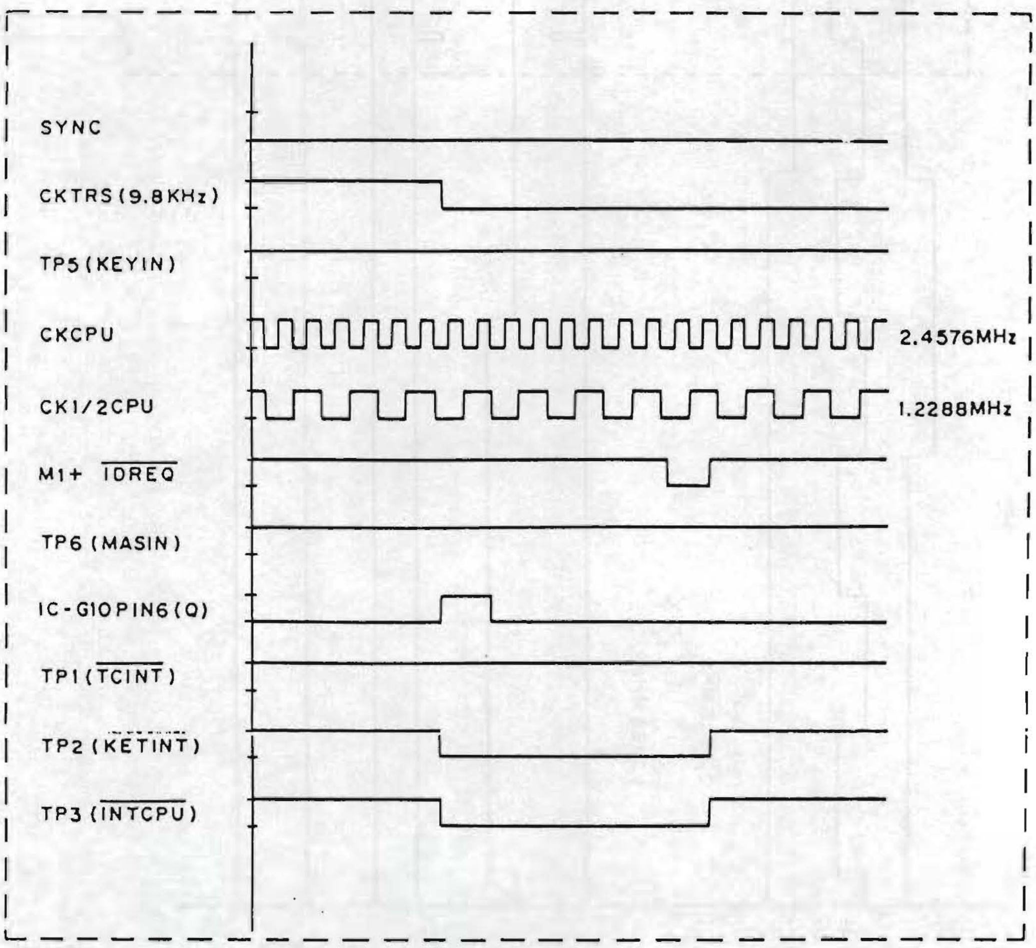


Figure 7-103(C) Timing Diagram (continued)

7.12.3 MICROPROCESSOR MEMORY CIRCUIT

The system control microprocessor is assigned memory in 2K byte blocks as shown in the emory map in Figure 7-104. The program area comprises 2716 ROMs for SYS1 - SYS4 and SYS5 - SYS8 plus 2k-bytes of 2114 RAM as a working area. As the time code interrupt and Auto Locate location etc. are also transmitted using the memory space, they are show on the memory map, the input port being shown as INTC and the output port as OUTTC.

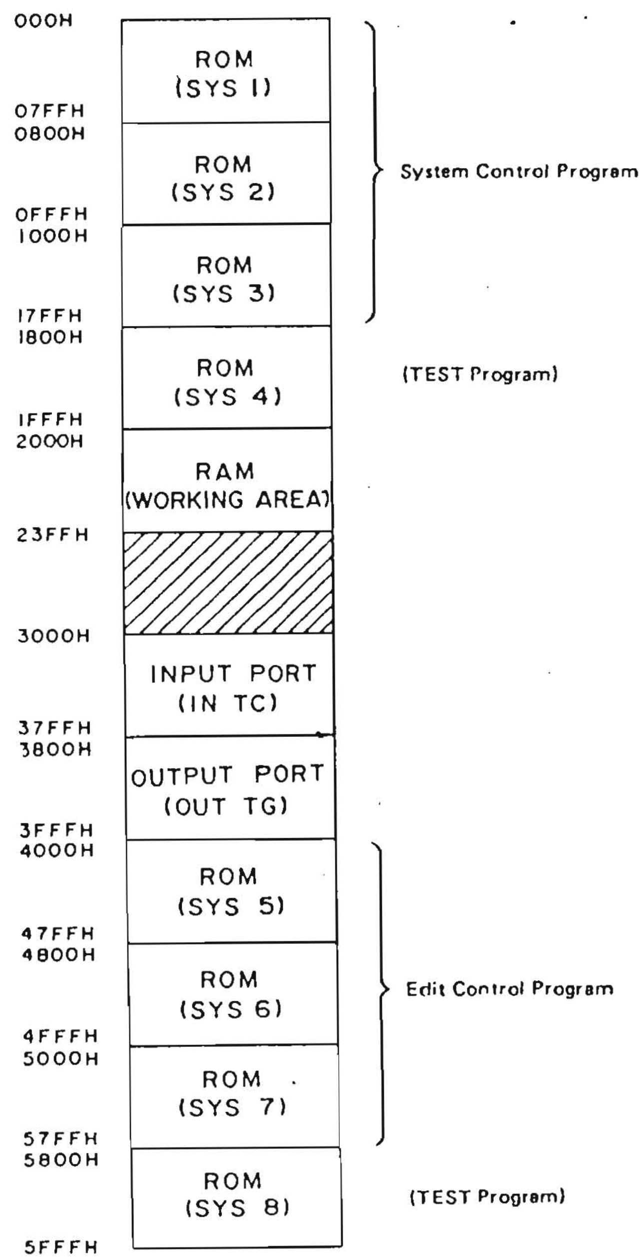


Figure 7-104 Memory Map

These memory locations are selected by address output by the CPU. Memory selection is by controlling Chip Select or OUtput using address decoders to control each memory. As the memory is separated into 2K byte blocks, decoding of address lines A_{11}, A_{12}, A_{13}, and A_{14} is used. For this purpose, SN74LS138s 3-to-8 line decoder/ multiplexers are used, located at I6 and I7. The block diagram is given in Figure 7-105.

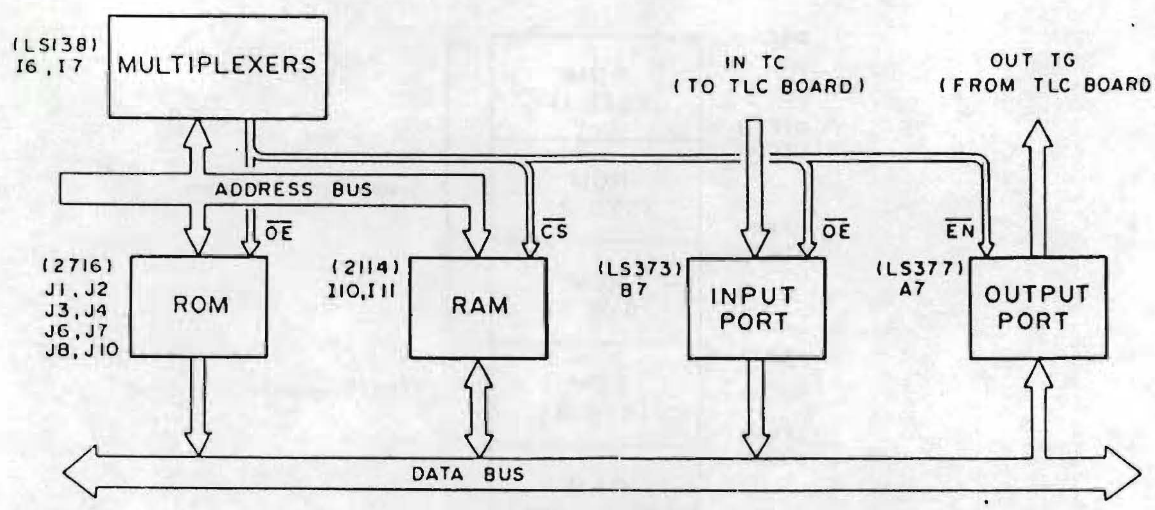


Figure 7-105 Memory Circuit

7.12.3.4 DATA AND ADDRESS BUFFERS

The Z-80 is fabricated using MOS technology and therefore cannot sink very much current. This necessitates buffering the data (d_0 - d_7) and the necessary address lines (A_0 - A_3). SN74LS365 ICs are used as the buffers (IC-E8 and IC-G8) and they supply data tot he output ports.

7.12.3.5 I/O PORT CIRCUIT

I/O ports are provided in the System Control Circuit for the necessary VTR remote control output, function status input, mode signals to other circuits blocks, memory block address inputs and outputs and word data inputs and outputs. The I/O ports are specified by the lower eight bits of the Z-80 address bus and lines A_0 - A_3 (of address lines A_0 - A_8) are decoded to provide 16 separate ports. SN74LS138 ICs are used as the decoders, the ones for the input ports being IC-G7 and IC-G4 and those for the output ports being IC-G6 and IC-G4 and those for the output ports being IC-G6 and IC-G5. The block diagram in Figure 7-106, Table 7-12-3 shows a plan of the I/O ports. Refer to the Z-80 manual.

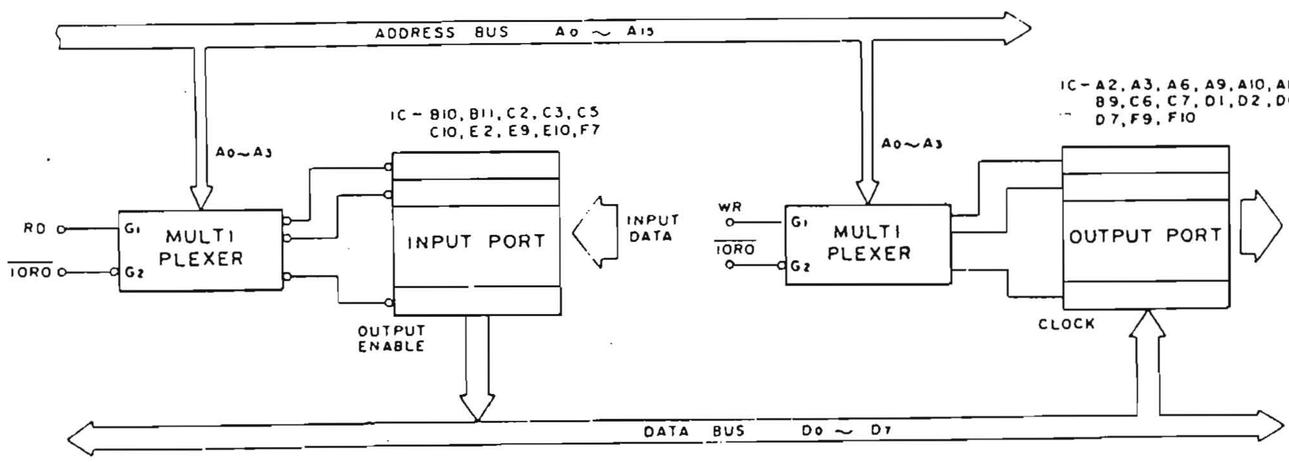


Figure 7-106 I/O Port Circuit

INPUT PORT

Address	CONTENTS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port Function
00_H	$\overline{\text{SERVO}}$	REC (CUT IN)	$\overline{\text{REW}}$	$\overline{\text{FF}}$	REV	$\overline{\text{FWD}}$	$\overline{\text{PAUSE}}$	$\overline{\text{STOP}}$	RECORDER STATUS-1
01_H	VIDEO INSERT	AUDIO CH2 INSERT	AUDIO CH1 INSERT	ASSEMBLE	x	x	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$	RECORDER STATUS-2
02_H	$\overline{\text{SERVO}}$	$\overline{\text{REC}}$	$\overline{\text{REW}}$	$\overline{\text{FF}}$	REV	$\overline{\text{FWD}}$	$\overline{\text{PAUSE}}$	$\overline{\text{STOP}}$	PLAYER-A STATUS
03_H	x	x	x	x	NORMAL / TEST	$\overline{\text{EDIT POINT}}$	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$	PLAYER-A SPEED & CONTROL
04_H	$\overline{\text{SERVO}}$	$\overline{\text{REC}}$	$\overline{\text{REW}}$	$\overline{\text{FF}}$	REV	$\overline{\text{FWD}}$	$\overline{\text{PAUSE}}$	$\overline{\text{STOP}}$	PLAYER-B STATUS
05_H	x	x	x	x	x	x	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$	PLAYER-B PSEED
06_H	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	KEY DATA
07_H	PLAYER-B $\overline{\text{STANDBY}}$	PLAYER-A $\overline{\text{STANDBY}}$	RECORDER $\overline{\text{STANDBY}}$	SEARCH $\overline{\text{MUTE}}$	0 dB	CHECK MODE-3	CHECK MODE-2	CHECK MODE-1	CHECK & STATUS
$0C_H$	EA_7	EA_6	EA_5	EA_4	EA_3	EA_2	EA_1	EA_0	LOWER EDIT ADDRESS
$0D_H$	x	x	EA_{13}	EA_{12}	EA_{11}	EA_{10}	EA_9	EA_8	UPPER EDIT ADDRESS
$0E_H$	RA_6	RA_5	RA_4	RA_3	RA_2	RA_1	RA_0	$RA_{(-1)}$	LOWER MEMORY ADDRSS
$0F_H$	RA_{14}	RA_{13}	RA_{12}	RA_{11}	RA_{10}	RA_9	RA_8	RA_7	UPPER MEMORY ADDRESS

OUTPUT PORT

Address	CONTENTS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port Function
00_H	LDD_7	LDD_6	LDD_5	LDD_4	DD_3	DD_2	DD_1	DD_0	DISPLAY DATA
01_H	TENSION	REC	REW	FF	REV	FWD	PAUSE	STOP	RECORDER COMMAND-1
02_H	VIDEO INSERT	AUDIO CH2 INSERT	AUDIO CH1 INSERT	ASSEMBLE	EDIT	COT OUT	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$	RECORDER COMMAND-2
03_H	TENSION	REC	REW	FF	REV	FWD	PAUSE	STOP	PLAYER-A COMMAND
04_H	x	x	x	x	x	x	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$	PLAYER-A SPEED CONTROL
05_H	TENSION	REC	REW	FF	REV	FWD	PAUSE	STOP	PLAYER-B COMMAND
06_H	x	x	x	x	x	x	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$	PLAYER-B SPEED CONTROL
07_H	x	x	$\overline{\text{EPKEY}}$-$\overline{\text{REL}}$	$\overline{\text{MANKEY}}$	SEARCH VAR/$\overline{\text{NORM}}$	SEARCH MAN/$\overline{\text{HLF}}$	SEARCH CH2	SEARCH CH1	SEARCH CONTROL
08_H	X' Fade TIME-2	X' Fade TIME-2	X' Fade TIME-1	X' Fade TIME-0	X' Fade $\overline{\text{START}}$	X' Fade MODE-2	X' Fade MODE-1	X' Fade MODE-0	CROSSFADE CONTROL
09_H	x	PLA/$\overline{\text{PLB}}$	VIDEO SEL-B	VIDEO SEL-A	EDITOR MODE-3	EDITOR MODE-2	EDITOR MODE-1	EDITOR MODE-0	EDITOR MODE CONTROL
$0A_H$	RARST	x	$\overline{\text{XFDFM}}$	ADRSLD $\overline{\text{REQ}}$	SYNC	$\overline{\text{DLMFM}}$	DW. FLAG	TRST	BUS CONTROL
$0B_H$	x	x	x	x	$\overline{\text{REC RAM}}$	$\overline{\text{PB RAM}}$	x	x	RAM WRITE/READ SIGNAL
$0C_H$	EA_7	EA_6	EA_5	EA_4	EA_3	EA_2	EA_1	EA_0	LOWER EDIT ADDRESS
$0D_H$	x	x	EA_{13}	EA_{12}	EA_{11}	EA_{10}	EA_9	EA_8	UPPER EDIT ADDRESS
$0E_H$	RA_6	RA_5	RA_4	RA_3	RA_2	RA_1	RA_0	$RA_{(-1)}$	LOWER MEMORY ADDRESS
$0F_H$	RA_{14}	RA_{13}	RA_{12}	RA_{11}	RA_{10}	RA_9	RA_8	RA_7	UPPER MEMORY ADDRESS

Table 7-12-3 I/O Port Description

7.12.4 I/O Port Chart Breakdown

1. Input port bits

1.1. Recorder Status input-1

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
00H	$\overline{\text{SERVO}}$	$\overline{\text{REC}}$ (CUT IN)	$\overline{\text{REW}}$	$\overline{\text{FF}}$	REV	$\overline{\text{FWD}}$	$\overline{\text{PAUSE}}$	$\overline{\text{STOP}}$

(a) REV: 1: REV. mode 0: other mode active H
(b) $\overline{\text{STOP}}$ ~ $\overline{\text{FWD}}$, $\overline{\text{FF}}$ ~ $\overline{\text{SERVO}}$: active low

1.2. Recorder Status input

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
01H	VIDEO INSERT	AUDIO CH-1 INSERT	AUDIO CH-2 INSERT	ASSEMBLE	X	X	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$

(a) SPEED-A, SPEED-B (1 = High Level 0 = Low Level)

$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$	VTR SPEED
0	0	x1
0	1	x2
1	0	x1/5
1	1	x1/20

(b) ASSEMBLE ~ VIDEO INSERT: active High

Note: Inverts the $\overline{\text{SPEED-A}}$ and $\overline{\text{SPEED-B}}$ at the remote terminal to the VTR.

1.3. Player-A Status input

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
02H	$\overline{\text{SERVO}}$	$\overline{\text{REC}}$	$\overline{\text{REW}}$	$\overline{\text{FF}}$	REV	$\overline{\text{FWD}}$	$\overline{\text{PAUSE}}$	$\overline{\text{STOP}}$

1.4. Player-A Speed and Control input

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
03H	X	X	X	X	NOR-NAL/ TEST	$\overline{\text{EDIT POINT}}$	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$

(a) $\overline{\text{EDIT POINT}}$ = EDIT POINT KEY 0
(b) NORMAL/$\overline{\text{TEST}}$ = 1 : NORMAL MODE, 0 : TEST MODE

1.5. Player-B Status input

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
04H	$\overline{\text{SERVO}}$	$\overline{\text{REC}}$	$\overline{\text{REW}}$	$\overline{\text{FF}}$	REV	FWD	$\overline{\text{PAUSE}}$	$\overline{\text{STOP}}$

1.6. Player-B Speed input

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
05H	X	X	X	X	X	X	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$

1.7. Key Data input

Key data is input during interrupts. Refer to Table 7-12-1.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
06H	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0

1.8. Check and Status Input

Input the Test Mode

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
07H	PLAYER-B STANDBY	PLAYER-A STANDBY	RECORDER STANDBY	SEARCH MUTE	0 dB	CHECK MODE-3	CHECK MODE-2	CHECK MODE-1

(a) 0 dB: Inputs 1 when Fader level is 0 dB
(b) SEARCH MUTE: Inputs 0 when the Search Mode is in the Manual state and when the Search Dial is stopped.
(c) STANDBY: Active low for Recorder, Player A and Player B standby condition.

1.9. Edit Address input

Inputs the Edit Point word address (14 bit).
EA_0 is the LSB.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0CH	EA_7	EA_6	EA_5	EA_4	EA_3	EA_2	EA_1	EA_0
0DH	X	X	EA_{13}	EA_{12}	EA_{11}	EA_{10}	EA_9	EA_8

$EA_0 \sim EA_{13}$: Active High

1.10. Memory Address Input

Inputs the lower address RA (-1) Made by the SEARCH CONTROL and the Memory Board Address (RA_0 - RA_{14}).

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0EH	RA_6	RA_5	RA_4	RA_3	RA_2	RA_1	RA_0	$RA_{(-1)}$
0FH	RA_{14}	RA_{13}	RA_{12}	RA_{11}	RA_{10}	RA_9	RA_8	RA_7

$RA_{(-1)} \sim RA_{14}$: Active High

2. Output Port Bits

2.1. Display Data output

The keyboard display data is output to the display RAM but as this has a 4 bit input, only the lower 4 bits of display data are output. The upper 4 bits D4 - D7's LDD_4- LDD_7 are data for display memory write counter, and load the counter at the time of all "H" data.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
00	LDD_7	LDD_6	LDD_5	LDD_4	DD_3	DD_2	DD_1	DD_0

DD_0 ~ DD_3: Active High

2.2 Recorder Command Output-1

Output commands to the Recorder VTR. All outputs are active high but are inverted to active low by the drivers.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
01H	TENSION	REC	REW	FF	REV	FWD	PAUSE	STOP

STOP ~ TENSION: Active High

2.3. Recorder Command Output-2

Outputs the Recorder VTR's speed and edit controls. Speed data is output as described in Section 2 but is inverted at the VTR remote control terminal and is output as SPEED-A and SPEED-B.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
02H	VIDEO INSERT	AUDIO CH2 INSERT	AUDIO CH1 INSERT	ASSEM-BLE	EDIT	CUT OUT	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$

SPEED-A ~ VIDEO INSERT: Active High

2.4. Player-A Command Output

Outputs commands to the Player-A VTR.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
03H	TENSION	REC	REW	FF	REV	FWD	PAUSE	STOP

2.5. Player-A Speed Control Output

Outputs the speed control signal to the Player-A VTR.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
04H	X	X	X	X	X	X	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$

2.6. Player-B Command Output

Output commands to the Player-B VTR.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
05H	TENSION	REC	REW	FF	REV	FWD	PAUSE	STOP

2.7. Player-B Speed Control Output

Outputs the speed control signal to the Player-B VTR.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
06H	X	X	X	X	X	X	$\overline{\text{SPEED-B}}$	$\overline{\text{SPEED-A}}$

2.8 Search Control Output

In the Search mode, the Channel, Speed and Manual key signals are output as well as the separated Edit Point key signal.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
07H	.X	X	$\overline{\text{EP KEY REL}}$	$\overline{\text{MAN-KEY}}$	SERCH VAR/$\overline{\text{NORN}}$	SERCH MAN/$\overline{\text{HLF}}$	SERCH CH2	SERCH CH2

(a) CH1, CH2
Selects the Search Mode channel

SEARCH CH1	SEARCH CH2	SEARCH CHANNEL
1	0	CH1
0	1	CH1
1	1	MIX (CH1 + CH2)

(b) SEARCH MAN/$\overline{\text{HLF}}$, VAR/NORM
In the Search Mode: outputs the normal speed (x1), half speed (x1/2) and the manual speed control signals.

MAN/$\overline{\text{HLF}}$	VAR/$\overline{\text{NORM}}$	SEARCH SPEED
0	0	x1
0	1	x1/2
1	1	MANUAL

(c) $\overline{\text{MAN KEY}}$
Software processed output when the MANUAL key is pressed.

(d) $\overline{\text{EPKEY REL}}$-
The signal showing that the Edit Point key has been released actually suffers from contact bounce; to prevent this problem, a timer delay is introduced.

2.9 Cross-fade Control Output

In the straight mode when the Source Select switch is pressed and the reproduced source is switched, the cross-fade is used and the Fade-out --> Fade-in operation takes place. The cross-fade mode is specified by three bits. The cross-fade time when editing or previewing (1 -99msec) is output.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
08H	X'Fade Time-3	X'Fade Time-2	X'Fade Time-1	X'Fade Time-0	$\overline{\text{X'Fade START}}$	X'Fade Mode-2	X'Fade Mode-1	X'Fade Mode-0

Cross Fade Addresses

2.9a. Cross-fade Mode - - 0, 1 2

Sets the Recorder and Player replay and search modes. When the cross-fade mode has been switched, a mute signal is output. The cross-fade mode is related to the Edit Mode described below.

X'Fade Mode-2	X'Fade Mode-1	X'Fade Mode-0	PLAYBACK MODE
1	1	1	STRAIGHT PLAYER
1	1	0	STRAIGHT RECORDER
1	0	1	SEARCH PLAYER
1	0	0	SEARCH RECORDER
0	X	X	MUTE

Cross Fade Mode Table

b. Cross-fade Start ($\overline{XFDS}$) output

The cross-fade start signal starts the playback mode set by the cross-fade mode. It is output, standardized by Word Sync in the System Control Circuit. The timing chart is shown in Figure__ The XFDSTRT signal is made in a similar XFDST, from the EDT Board during Preview or Auto Edit. (Interrupts not enabled)

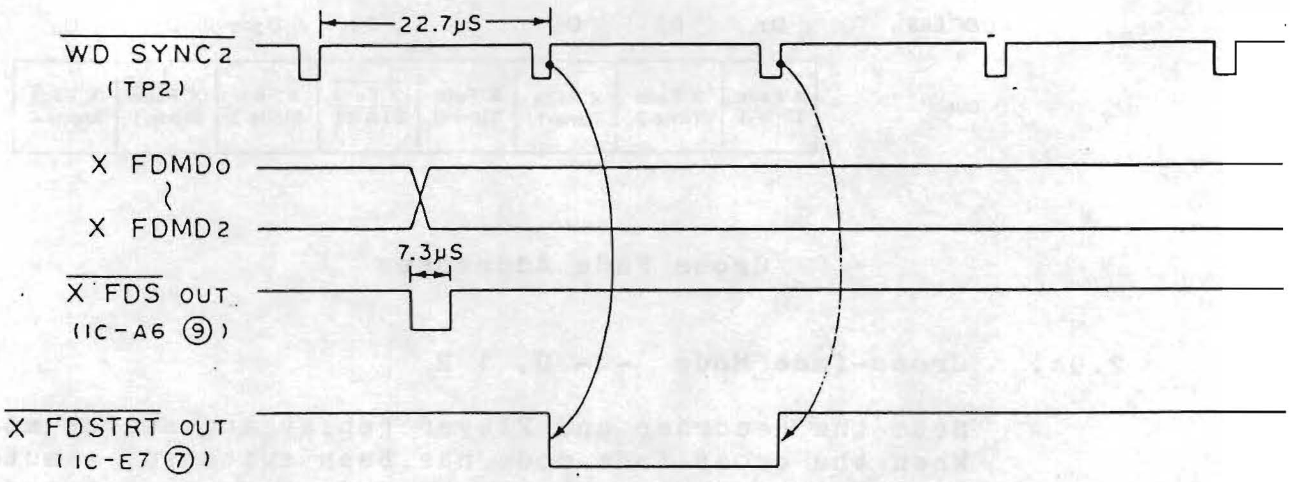


Figure 7-107 The Relationship Between Cross-fade Mode and Cross-fade Start

c. Cross-fade Time output

Ten stages of cros-fade can be selected during preview or Auto Edit. The encoded data is output as four bits.

X'Fade Time-3	X'Fade Time-2	X'Fade Time-1	X'Fade Time-0	X'Fade Time (mSec)
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	7
0	1	0	0	10
0	1	0	1	15
0	1	1	0	30
0	1	1	1	50
1	0	0	0	70
1	0	0	1	99

2.10 Editor Mode Control output

The signal path mode is specified by four bits for defining the signal processing in the editor while two bits are used to select the replay Video signal. During Preview or Auto Edit, using the VTR (BVU200B) synchronization terminal allows two VTRs to run in sync. At this time a Player-A or Player-B selection signal is also output.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
09H	X	PLA/PLB	VIDEO SEL-B	VIDEO SEL-A	EDITOR MODE-3	EDITOR MODE-2	EDITOR MODE-1	EDITOR MODE-0

Editor Mode/Video Select Addressing

a. Editor Mode 0 -3

The Editor signal flow has the following modes. All the Check Mode 0 -2 inputs to the Input Port (07H) should be high at this time. If any bits are low, will become Check Mode.

1. **Straight Mode**
   Outputs the digital output from the PCM processor as it is to the Encoder and the D/A.

2. **Search Mode**
   Produces a digital output from the memory in the Editor during a SEARCH.

3. **Clears the Memory Board RAM(1M bytes).**

4. **Mute Output Mode**
   Outputs a Mute (16-bits/CH -- all zero digital data) to the Encoder and the D/A.

5. **REC RAM Write Mode**
   Writes the data from the REcoder needed for an edit into the Memory Board.

6. **PB RAM Write Mode**
   Writes the data from the Player needed for an edit into the Memory Board.

7. **Delay Measurement Mode**
   Measures the Delay Word numer by the PCM Processor's internal memory.

8. **Edit Mode**
   At Preview or Editing times: the Edit Mode divides the Edit Control Circuit into Edit Modes 1,2,3, or 4 (refer to the Edit Control Circuit description).

the table below shows how various Editor Modes (0, 1, 2, 3) are set up, together with the corresponding Check Mode (1, 2, 3) inputs.

Editor Mode	Editor Mode Output				Check Mode Input		
	EDTMD3	EDTMD2	EDTMD1	EDTMD0	CHKM3	CHKM2	CHKM1
RAM CLEAR	0	0	0	1	1	1	1
STRAIGHT	0	0	1	1	1	1	1
SEARCH	0	1	1	1	1	1	1
CHECK 1	0	1	1	0	1	1	0
CHECK 2	0	1	0	1	1	0	1
CHECK 3	0	1	0	0	1	0	0
CHECK 4	0	0	1	0	0	1	0
CHECK 5	0	0	0	0	0	0	0
MUTE OUTPUT	1	0	0	0	1	1	1
DELAY MEASUREMENT	1	0	0	1	1	1	1
PB RAM WRITE	1	0	1	0	1	1	1
REC RAM WRITE	1	0	1	1	1	1	1
EDIT	1	1	1	1	1	1	1

Editor Mode Table

b. Video Select A/B output

As it is necessary to be able to switch the video inputs from the Recorder, Player-A and Player-B when editing and playing, a two bit Video Select signal is output.

VIDEO SEL-B	VIDEO SEL-A	VIDEO SELECT
0	0	PCM Processor
0	1	RECORDER
1	0	PLAYER-A
1	1	PLAYER-B

Video Select Table

c. Player A or B output

During Preview and Editing operation Player-A and Player-B are synchronized and a signal is used to show which player is being synchronized (Player A or B). This signal is high for Player-A and low for Player-B.

2.11 Bus Control output

For setting the Edit Point, both the EA (Edit Address) bus the RA (Ram Address) bus are used and a control signal is output.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0AH	$\overline{\text{RARST}}$	X	$\overline{\text{XFDFM}}$	$\overline{\text{ADRS-LDRER}}$	SYNC	$\overline{\text{DLMFM}}$	DWFLAG	TRST

Status Flag Word

a. **TRST (EA bus tr-state request)**
This is the control signal for the EA bus which exchanges frame word number data. H level .... outputs data from the SYS board to the EDT Board.

b. **DWFLAG (Demand Word Flag)**
The EA bus exchanges word numbers in order to synchronize the Edit Point word and the Delay Word number, DWFLAG is the EA bus data flag. For details refer to the Edit Control Circuit description.

c. **DLMFM (Delay Measuring Frame)**
During Preview and Auto Edit, this measures the PCM Processor Delay Word before the RAM write mode. The measurement takes place on the next frame after this signal output. It is output active low.

d. **$\overline{\text{ADRS LD REQ}}$**
After changing from Manual Search to x1 or x1/2, or after changing from Straight mode to Search mode, the Memory Start Point or Center address is formed and this signal is output. Output is active low.

e. **SYNC (Synchronize)**
During Preview or Auto Edit, the player VTR is synchronized. While synchronization is taking plave, this signal is output high.

f. **$\overline{\text{XFDFM}}$ (Crossfade Frame)**
This frame is output at low level one frame prior to the crossfade position for the RECORDER and PLAYER during the Preview or Auto Edit.

g. **$\overline{\text{RARST}}$ (RAM Read Start)**
This is used for reading words from RAM (Memory board) to timing in the edit control circuit description. The output is so a to show active-low.

2.12 RAM WRITE/READ Signal Output

In the Edit mode, these are timing pulses for writing into and reading from the REC RAM and the PB RAM. The writing and rading of the REC RAM and PB RAM are started in the next frame. They are active low.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0BH	X	X	X	X	$\overline{\text{REC RAM}}$	$\overline{\text{PB RAM}}$	X	X

2.13 EDIT ADDRESS Output

Data necessary for editing is output to the EA BUS. The word address is composed of 14 bits. The EA_0 is in the LSB.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0CH	EA_7	EA_6	EA_5	EA_4	EA_3	EA_2	EA_1	EA_0
0DH	X	X	EA_{13}	EA_{12}	EA_{11}	EA_{10}	EA_9	EA_8

2.14 MEMORY ADDRESS Output

The memory board addresses (RA_0 through RA_{14}) are output to the SC-A board. At this time, $RA_{(-1)}$, one bit below RA_0 is also output.

ADDRESS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0EH	RA_6	RA_5	RA_4	RA_3	RA_2	RA_1	RA_0	$RA_{(-1)}$
0FH	RA_{14}	RA_{13}	RA_{12}	RA_{11}	RA_{10}	RA_9	RA_8	RA_7

7.12.5 KEYBOARD INPUT/OUTPUT CIRCUIT

As described in 7-100 CONFIGURATION, the keyboard switch signals are received as serial data in sync with the transmission clock CKTRS (9.6kHz) and the transmission synchronizing signals SYNC (37.5 Hz). Display data is also transmitted in the same form. The encoder for inputting the switch signals into the CPU is clocked at the same frequency as the read address counter of the display data transmission buffer memory, so a single unit can be used for these two functions.

As the display data from the microprocessor is output in the lower four bits; D_0 through D_3 of the data bus D_0 through D_7, write address count is increased when output port address 00H is selected.
Since writing has priority with the display data memory (IC-G1), a latch is used to convert display data between parallel and series. Figure 7-108 shows the circuit configuration.

7.12.5.1 Read Address Counter/Encoder

This is an 8-bit (2 x 4 bits) counter counting at $\overline{\text{CKTRS}}$, comprising IC-H3 and H4 (SN74LS163). It generates transmission synch from the carry output (IC-H3, pin 15) of the 8-bit copunter. The timing chart is shown in Figure 7-109.

7.12.5.2 KEY DATA LATCH

As shown in Figure 7-109, Keyboard KYDT and encoder data ($DMRA_0$ - $DMRA_7$ are about 180° out of phase. The latch circuit serves to ensure data input to the CPU for an interrupt.

7.12.5.3 WRITE ADDRESS COUNTER

When an interrupt signal goes to the CPU, the display data memory does not necessarily receive data in synchronization with it. Therefore, it forms write addresses incremented with multiplexed output port address signals.

In order to output RECORDER 10-hour display data in the 0-slot (00H) of the output timing, ther IC-G2 latch display must be cancelled, and for this, 8xH is loaded when RECORDER 10 hours are output.

Figure 7-110 shows the timing chart. The reference timing here is CKCPU (2.4576mHz).

7.12.5.4 ADDRESS SELECTOR

This selctor switches the display data memory REad/Write Addresses between ICI1, and I2. It is switched with Output Enable ($\overline{OE}$) from SN74LS373.

7.12.5.5 DISPLAY MEMORY

In order to convert the display data controlled by software into fixed cycle display data, display data is written into the display memory and read out at a fixed frequency.

7.12.5.6 DISPLAY MEMORY CONTROL

This control generates read/write address switching signals, and memory write enable ($\overline{WE}$) signals.

7.12.5.7 P/S CONVERTER

As the display memory for outputting 4-bit display data gives write priority, a data latch IC-G2 (SN7rLS175) is used to laod data into the shift register for P/S conversion in the subsequent stage. When the read address is $DMRA_0 = 0$, $DMRA_1 = 1$, many latch clocks IC-F2 (SN74LS175) through IC-G2 (SN74LS175) are output. SN74LS195 (IC-G3) is used as a P/S conversion shift register.

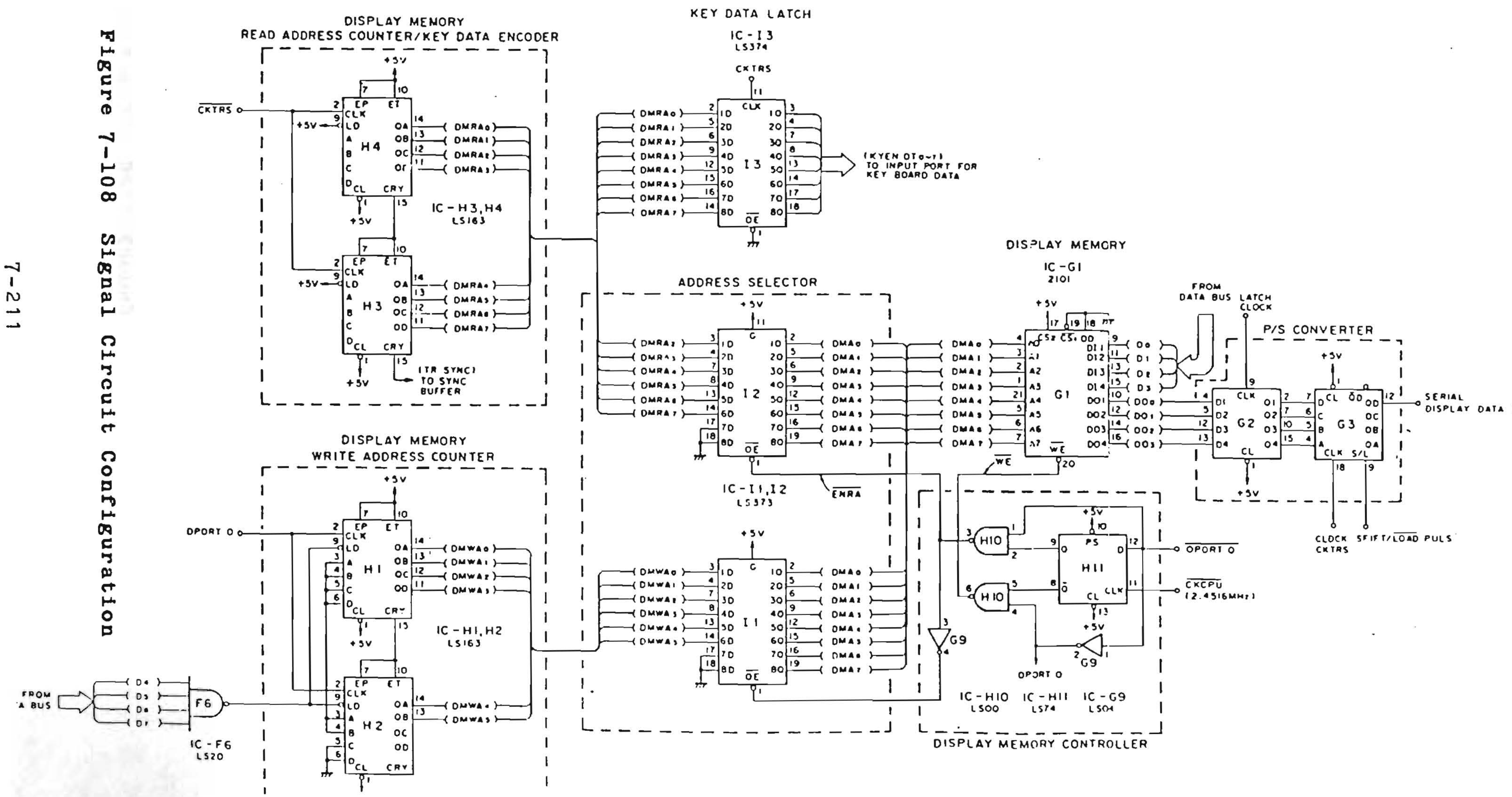


Figure 7-108 Signal Circuit Configuration

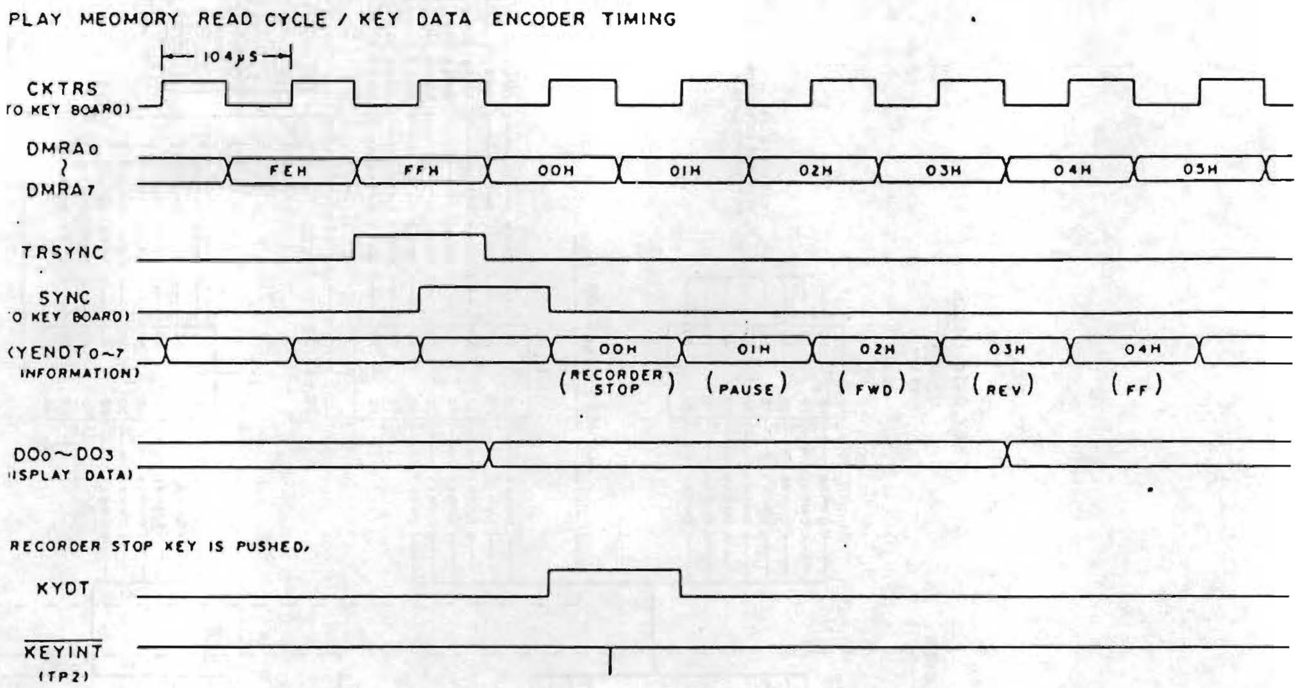


Figure 7-109 Display Memory Read Cycle/Key Data Encoder Timing

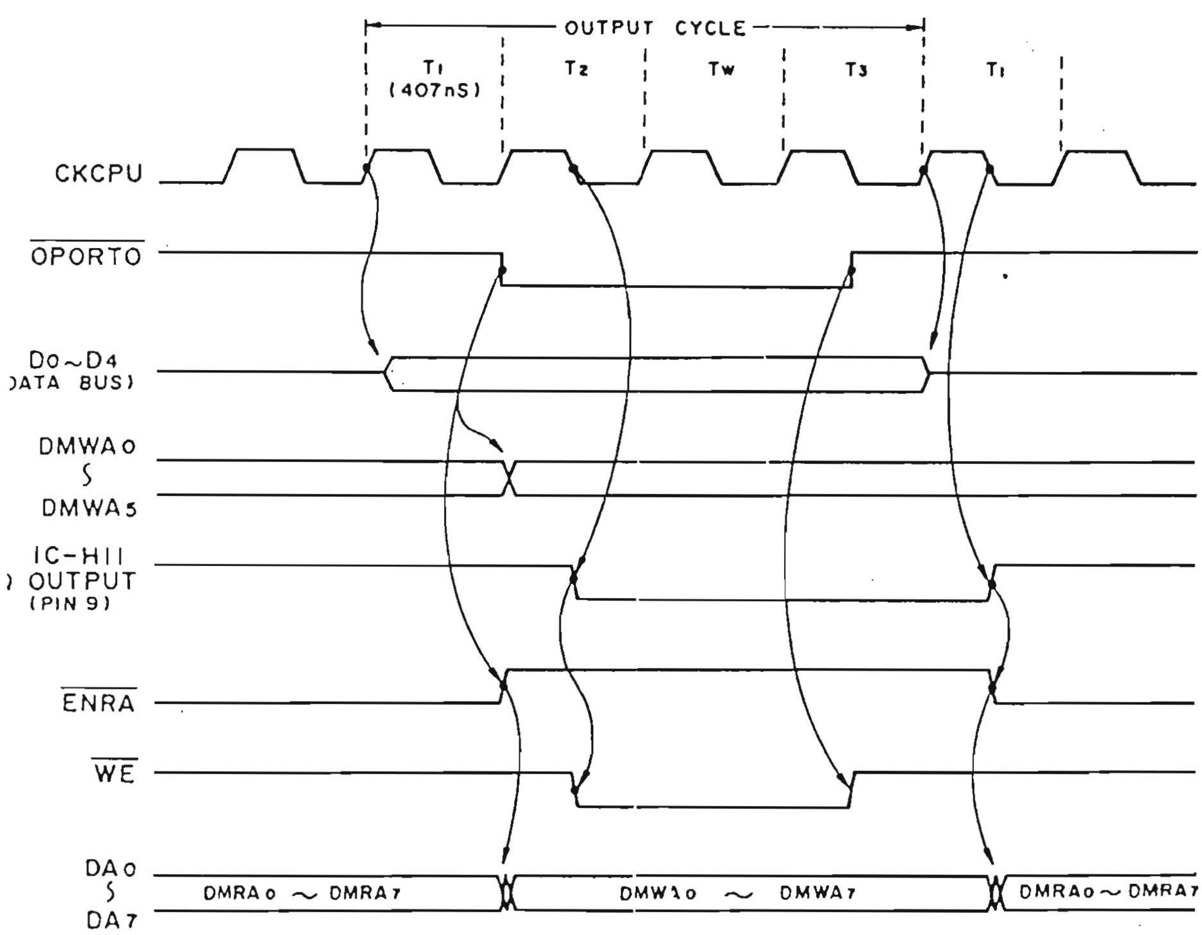


Figure 7-110 Display Memory Write Cycle Timing

7.12.6 EDIT POINT, MANUAL SIGNAL CIRCUIT

Quick response time is required for the EDIT POINT and SEARCH MODE MANUAL switch. As can be seen in the switching information in Table 7-12-1, EDIT POINT (KEY DATA: XXXX1110) and MANUAL (KEY DATA: XXXX1111) are received at 16-slot intervals; that is at 1.67 msec.

The leading eadges of EDIT POINT and MANUAL are detected by hardware. The circuit is shown in Figure 7-111, and the timing chart is shown in Figure 7-112.

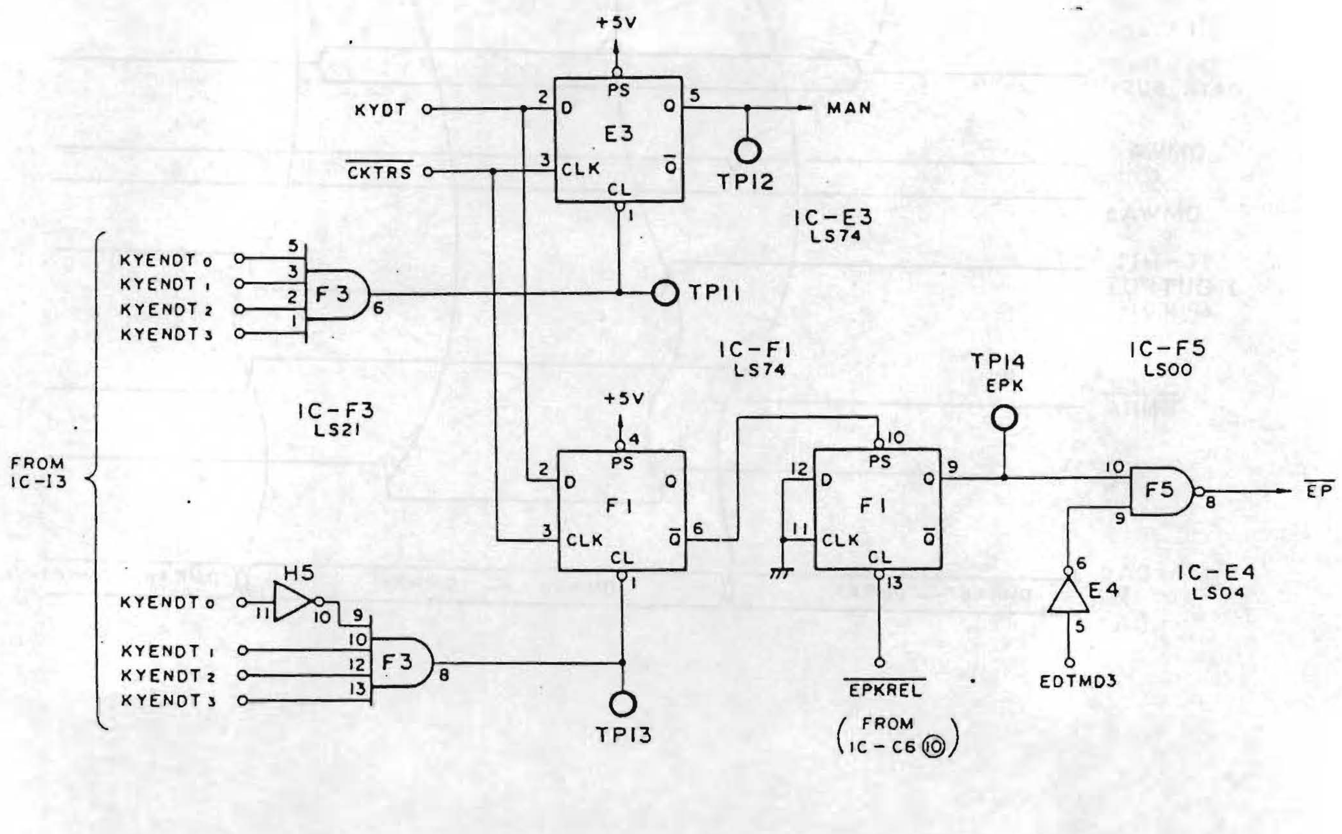


Figure 7-111 Edit Point Manual Signal Circuit

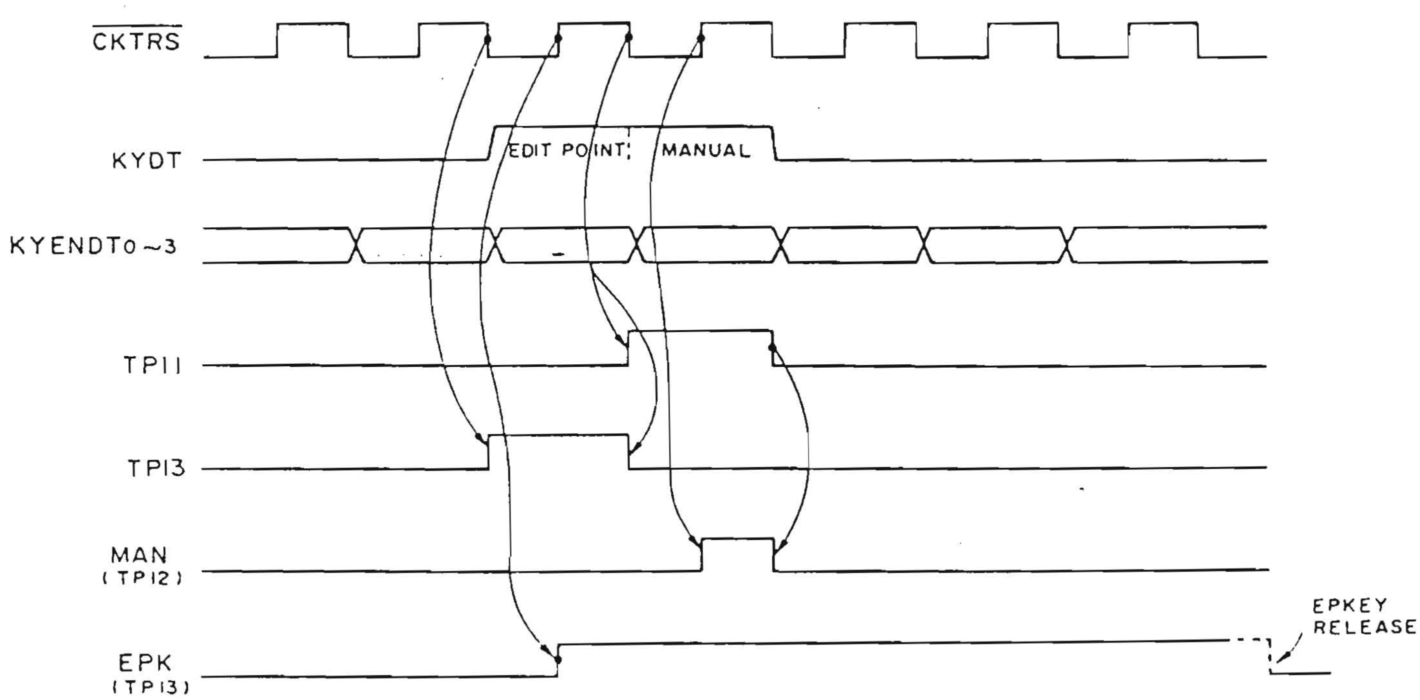


Figure 7-112 Timing of Manual Signal Circuit

7.12.7 FADER DATA CIRCUIT (S/P CONVERSION)

As shown in Figure 7-100, fader data for controlling keyboard level is also sent as special dat athat correcpionds to the timing determined by CKTRS and SYNC. As fader level is in 8 bits, 256-step data is received. Serial data is converted into 8-bit parallel data and output to the SC-A board. This circuit is shown in Figure 7-113 and the timing chart is shown in Figure 7-114 .

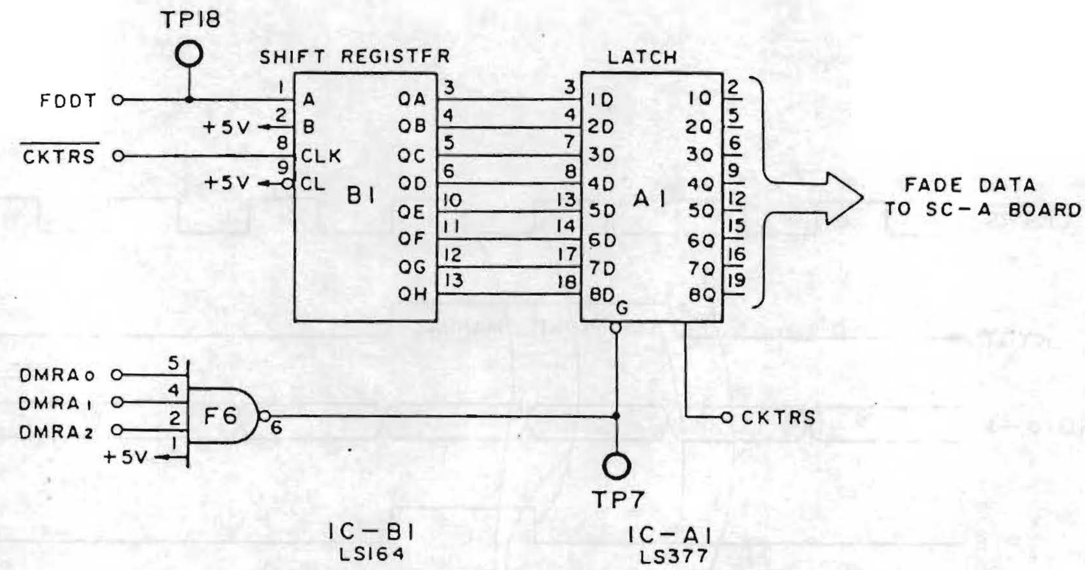


Figure 7-113 Fader Data Circuit (S/P Conversion)

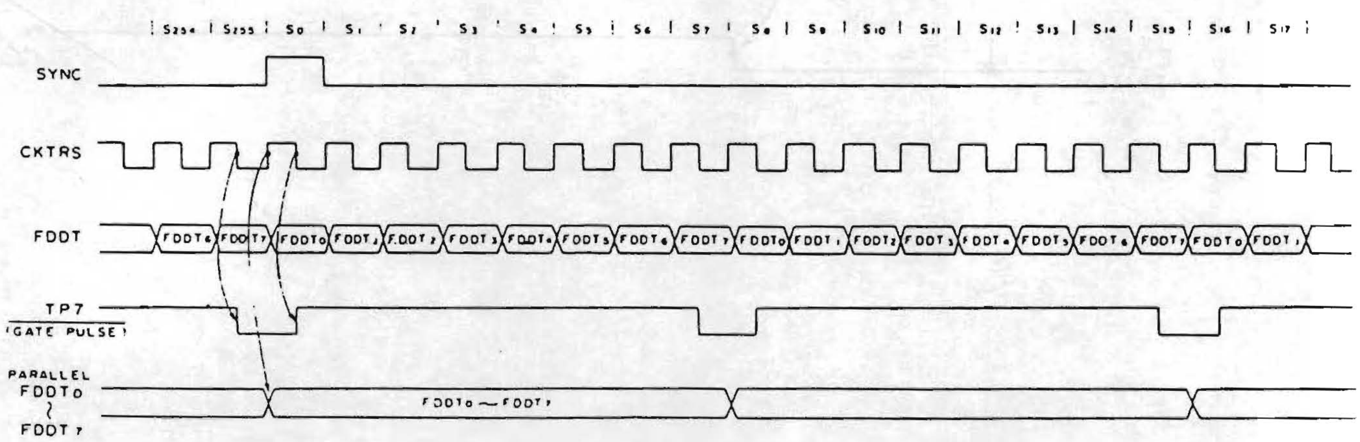
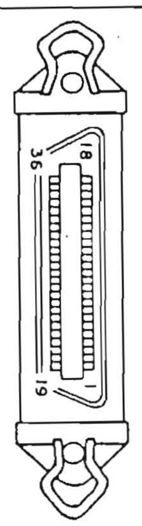


Figure 114 - Timing for S/P Conversion

7.12.8 VTR REMOTE CONTROL OUTPUT CIRCUIT

The VTR control signal is output through an output port of the microprocessor but the remote control output is via open collector inverters (SN74LS05). Figure 7-115 shows the BVU-200B remote control terminals and it should be noted that all these outputs are active low.



1. UNREG 5V
2. FF-COMMAND
3. FWD-COMMAND
4. REW-COMMAND
5. EJECT-COMMAND
6. STOP-COMMAND
7. PAUSE-COMMAND
8. REC-COMMAND
9. CUT IN-COMMAND
10. EDIT-COMMAND
11. CUT OUT-COMMAND
12. FF-STATUS
13. FWD STATUS
14. REW-STATUS
15. STAND BY-STATUS
16. STOP-STATUS
17. PAUSE-STATUS-1
18. REC-STATUS
19. CUT IN-STATUS
20. V-INS
21. A1-INS
22. A2-INS
23. REVERSE
24. SPEED A
25. SPEED B
26. CTL-PULSE
27. TACH
28. CAPSTAN
29. SYNCHRONIZE
30. STILL-TENSION
31. ABCP
32. PAUSE-STATUS-2
33.
34.
35. GND
36. GND

SPEED B	SPEED A	VTR SPEED
1	1	x 1
1	0	x 2
0	1	x 1/5
0	0	x 1/20

Figure 7-115 The BVU-200B Remote Control Connector Pin-out

7.12.9 KEY BOARD INTERFACE

The signal interface bwetween the editor KEYBOARD and the main unit receives and sends differential signals from the driver/receiver of EIA RS-422. Between the keyboard and the main unit, the following signals are exchanged. The driver/receiver circuit is provided with a 150 Ohm terminal resistor at the receiving end. Refer to Figure 7-116.

Signal name	Signal description	Signal direction	Note
CKTRS	Sending clock	Main unit ⟶ keyboard	9600 Hz
SYNC	Transmission sync signal	⟶	37.5 Hz
KYDT	Switch data	⟵	
DSPDT	Display data	⟶	
FDDT.	Fader data	⟵	8 bit Serial
SRCCK1	SEARCH CLOCK 1	⟵	Input to SC-A board
SRCCK2	SEARCH CLOCK 2	⟵	

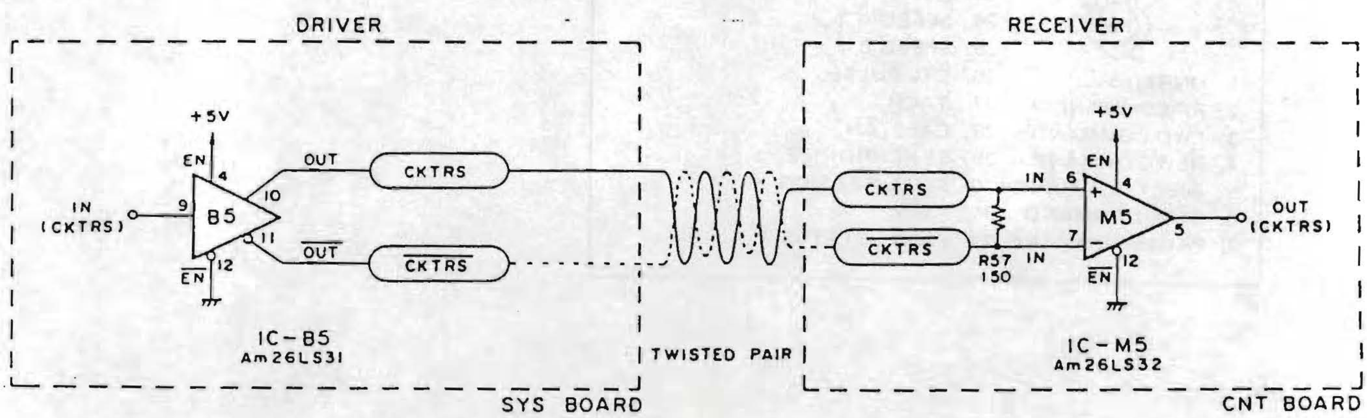


Figure 7-116 Keyboard Interface Circuit

7.12.10 POWER ON/OFF CIRCUIT

To start the CPU at address 0000H when the power supply is turned on, a reset circuit is provided, and this signal is also used as a reset signal for the interrupt control cirucit.

When the power supply is turned on, the VTRs are kept in the STOP condition by software. Figure 7-117 shows the reset circuit for the power supply switching time.

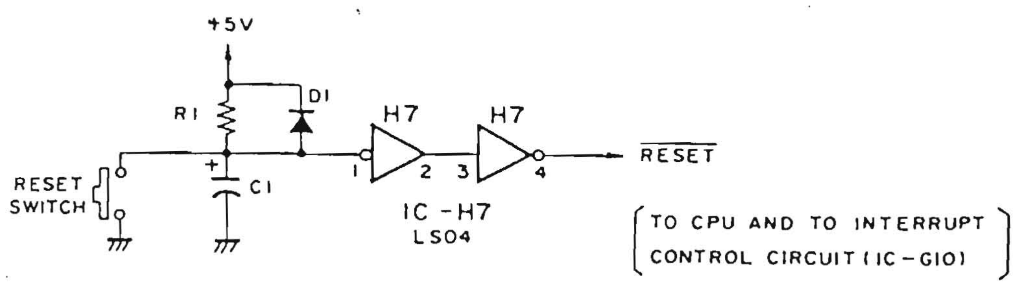


Figure 7-117 Reset Circuit

When **DAE-1100** power is turned off with the VTR power on, STOP signals are output to prevent the VTR from entering other modes such as FF etc. Its circuit is shown in Figure 7-118. As can be seen, while power is supplied to the VTR, the STOP command is output to the remote-control output through a wired-OR to the VTR's of recorder, Player-A and Player-B.

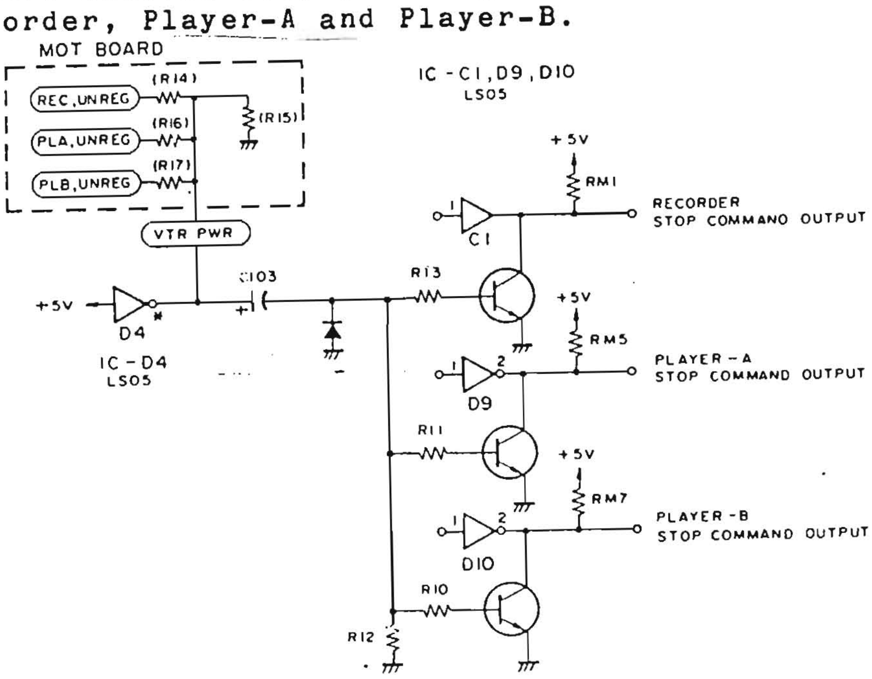


Figure 7-118 VTR Stop Circuit

7.13 KEYBOARD CIRCUIT
(SW-1, SW-2, CNT, SR-PW and SD Board)

7.13.1 General

The keyboard circuit sends switch signals to the slot decided by the transmission clock CRTRS and the transmission synch puls SYNC from the system control circuit in the main unit, receives display signals and displays them. Switches and displays are as follows: remote control switches for the recorder, Player-A and Player-B; function display and time code display; edit control switches for the search function, to trigger edit points, and preview or auto edit.

The search dial and search clock circuit are installed on the keyboard. Two phases (90° phase difference) are produced then and transmitted. The fader, which aligns levels when a level difference occurs at an edit point, is effective only for the player. It is 8-bit digital type. Fader data is serially converted and output.

Power (+14V to +18V) is supplied to the keyboard from the main unit, +5V for the digital system and +/-12V for the analog system are produced in the keyboard by the DC-DC converter to supply power to each keyboard.

7.13.2 Configuration

The keyboard block diagram (except the power supply block) is shown in Figure 7-119.

The row and column matrix is formed for the switch data and displays. Timings are produced by the transmission clock CKTRS and transmission synch pulse SYNC.

Key data is delivered to the main unit in the slot decided by CKTRS and SYNC. The key data can be output in the slot corresponding to each switch by addressing the CKTRS counter output. At the seam time, one point in the key matrix becomes active by addressing the appropriate row and column. The key data is transmitted as a differential signal by the EIA Standard RS-422 driver (Am26LS31).

The display data is received in the slot decided by CKTRS and SYNC. Differential display data is received by the RS-422 receiver (Am26LS32) and converted serial/parallel (1 to 4 line), then stored in the 64 x 4 bit RAM. It is necessary to store the display data time-slices are transmitted in 26.7msec cycles. Each time-slices consists

of eight four-bit blocks. Taking the time code display as an example, each digit takes one block and the four bits in one block are seven segment decoder data.

The display RAM and display matrix are controlled from the address counter which is also used to produce the key matrix.

The search clock is produced optically with slit-plate (1000 slits) rotor and stator by the SEARCH dial. This clock is amplified and changed to a square wave at mid-level by the clamping circuit, then output through the 12RS-422 driver. In the search clock, the rotor and stator slits are made so that the phase difference is 90° to enable detection of the detection of rotation.

The digital fader which controls the player regenerating level to +6dB - +6 to - uses 8 bits to obtain level information in 256 steps. Levels close to 0dB are changed in 0.2 dB steps.

Power supply to each block is +5V and +/-12V converted by DCV-to-DC converter from the +14V to +18V supplied by the main unit. +5V is supplied to the digital system and +/-12V to the analog system.

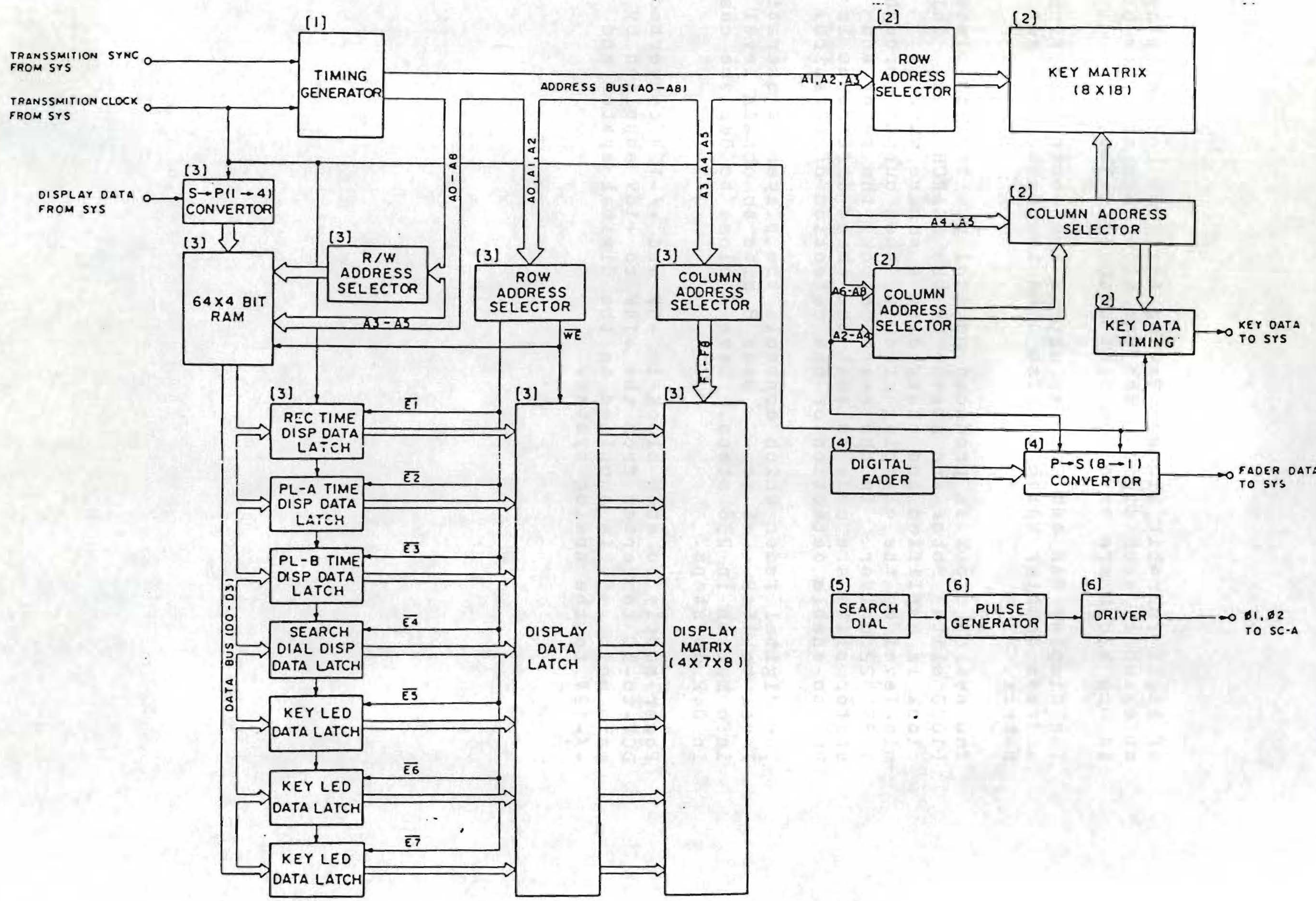


Figure 7-119 Keyboard Block Diagram

7.13.3 Circuit Description

1. Keyboard Input-Output Signals

The form of the keyboard input-output signals is as follows:

Keyboard input-output signals are transmitted or received at the frequencies shown in Table 7-119 and timing shown in Figure 7-120. Figure 7-121 shows input-output signals at the keyboard connectors.

a. **CKTRS and SYNC:**
One slot of transmission data is from the leading edge of CKTRS to the next leading edge so that the end of the transmission clock and idle synch pulses come inthe cneter of the SYNC opulse. So is one SYNC pulse width, thus slots are $S_1, S_2 .... S_{255}$.

b. **KYDT (Key data):**
KYDT becomes high in transmission line when a key is pushed. In response to a key entry, key data corresponds to the slots shown in Table 7-13-2. For example, S_1 is for Recorder Stop Information and S_2 is for the Recorder Pulse information. In Table 2-8-2, d_0 to d_7 are defined as follows:

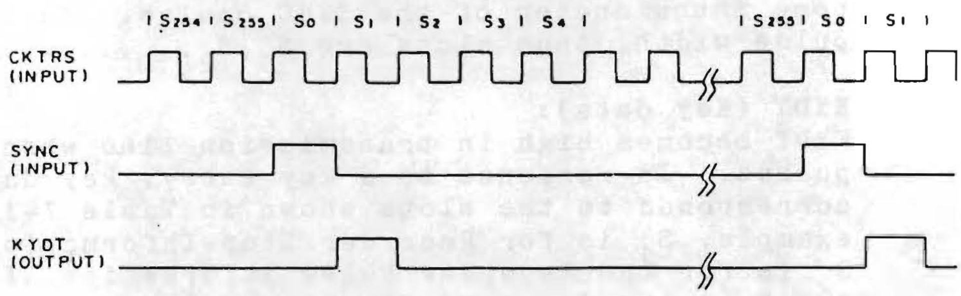
$$S_n^{KY} = \text{Key data for nth /slot}$$

$$h = \sum_{i-0} di2i = 1$$

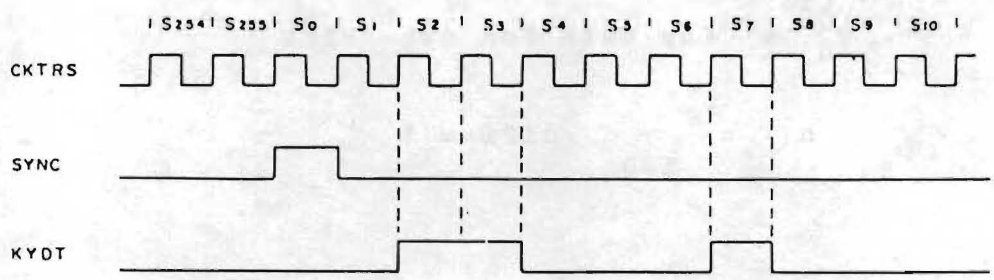
Signal	Frequency
Transmission clock frequency (CKTRS)	9,600 Hz
Idle synch frequency (SYNC)	37.5 Hz
Number of transmission data slots	256

Table 7-13-1 Signal Frequency

(A) RECORDER "STOP" KEY PRESSED



(B) RECORDER "PAUSE" "FWD" "REC" KEY PRESSED



Timing Diagram

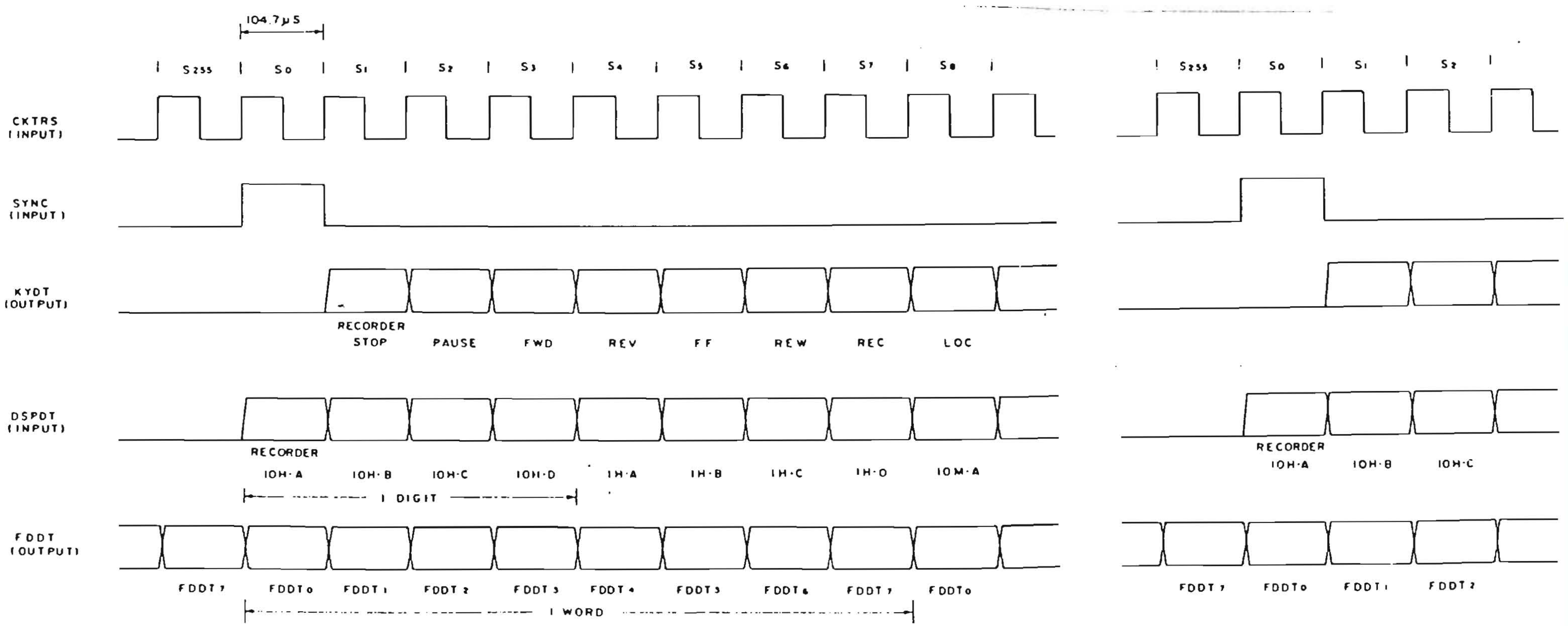
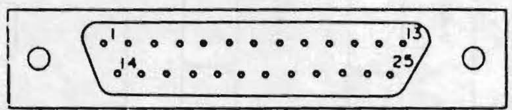


Fig. 7-120 I/O Signal Timing Chart

KEYBOARD CONNECTER



PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	FG(FRAME GRAND)	15	KYDT
2		16	$\overline{\text{KYDT}}$
3		17	FDDT
4		18	$\overline{\text{FDDT}}$
5		19	SRCCK1
6		20	$\overline{\text{SRCCK1}}$
7	SG(SIGNAL GRAND)	21	SRCCK 2
8		22	$\overline{\text{SRCCK 2}}$
9	SYNC	23	SG
10	$\overline{\text{SYNC}}$	24	+15V
11	CKTRS	25	+15V
12	$\overline{\text{CKTRS}}$		
13	DSPDT		
14	$\overline{\text{DSPDT}}$		

NOTE: 13 14 = PIN 13 AND PIN 14 ARE TWISTED PAIRS

Figure 7-121 Pin-out of Keyboard Connector

7.13.3 Circuit Description continued

c. **DSPDT (Display Data):**
The display data drives time display 7 seg. LEDs and function display lamp. For the time display LEDs transmission data is in 4 slots and 1-digit display data is transmitted in BCD. The function displays is switched to ON or OFF corresponding to high or low.

High --> 7 seg. data becomes 1. Function display data lamp is illuminated.

Low --> 7 seg. data becomes 0. Function display data lamp goes off.

S_0 is 2^0 for the received 4-bit data for the 1-digit (10 hours) rcorder time display. S_0 to S_3 enable a display of 10-hours. S_{123} contains the Recorder "Stop" display data.

In Table 2-8-3, d_0 to d_7 are defined as follows:

$$S_n^{DSP} = \text{nth/slot display data}$$

$$n = \underset{i=0}{} d_i 2^i$$

For time display the following expression is used:

HOURS	MINUTES	SECONDS	FRAMES
XX	XX	XX	XX

10H 1H 10M 1M 10S 1S 10F 1F

Each digit is represented as A, B, C and D.

$A = 2^0$ $B = 2^1$ $C = 2^2$ $D = 2^3$

eg. $IF = A_{IF} + B_{IF} + C_{IF} + D_{IF}$

The SEARCH dial display (32-point LED bar display) is expressed as P_0 to P_{31} from the left end of the keyboard

o o oooo.......ooo SEARCH Dial
P_0 P_1 P_{31} Display LED

Top View

$S_n^{KY} = S^{KY} \sum_{i=0} d_i 2^i + 1 \cdot S_0^{KT} =$

d4 ~ d0 \ d7 ~ d5	RECORDER 0 0 0	PLAYER A 0 0 1	PLAYER B 0 1 0	EDIT KEY 0 1 1	TEN KEY 1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0 0	STOP	STOP	STOP	PLAYER	TEN KEY 0			
0 0 0 0 1	PAUSE	PAUSE	PAUSE	RECORDER	1			
0 0 0 1 0	FWD	FWD	FWD		2			
0 0 0 1 1	REVERSE	REVERSE	REVERSE		3			
0 0 1 0 0	FF	FF	FF	PREVIEW	4			
0 0 1 0 1	REW	REW	REW	REVIEW	5			
0 0 1 1 0	REC (CUT IN)	REC	REC	AUTO EDIT	6			
0 0 1 1 1	AUTO LOCATE	AUTO LOCATE	AUTO LOCATE		7			
0 1 0 0 0	CUT OUT			P.R.T 5sec	8			
0 1 0 0 1	EDIT			P.R.T 10sec	9			
0 1 0 1 0				P.R.T 30sec	READER AUTO LOCATOR			
0 1 0 1 1					CLEAR			
0 1 1 0 0		PLAYER A	PLAYER B	IN				
0 1 1 0 1				OUT				
0 1 1 1 0	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT
0 1 1 1 1	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL
1 0 0 0 0	ASSEMBLE			SEARCH SPEED x1/2				
1 0 0 0 1	INSERT VIDEO			SEARCH SPEED x1				
1 0 0 1 0	ANALOG CH1							
1 0 0 1 1	ANALOG CH2							
1 0 1 0 0	SPEED x1	SPEED x1	SPEED x1	SEARCH MONITOR MIX				
1 0 1 0 1	SPEED x2	SPEED x2	SPEED x2	SEARCH MONITOR CH1				
1 0 1 1 0	SPEED x1/5			SEARCH MONITOR CH2				
1 0 1 1 1								
1 1 0 0 0	READER	READER	READER	CROSS FADE UP				
1 1 0 0 1	USER'S BIT	USER'S BIT	USER'S BIT	CROSS FADE DOWN				
1 1 0 1 0	AUTO LOCATOR	AUTO LOCATOR	AUTO LOCATOR					
1 1 0 1 1	GENERATOR							
1 1 1 0 0	HOLD							
1 1 1 0 1								
1 1 1 1 0	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT	EDIT POINT
1 1 1 1 1	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL	MANUAL

Table 7-13-2 Key Information

Received Slot No.			Display	
DSP S0	to	DSP S31	Recorder time-display	(8 digits)
S32	to	S63	Player A display	(")
S64	to	S95	Player B display	(")
S96	to	S127	Search dial bar display	(32 points)
S128	to	(Note) 151	Recorder key display	
S156			Recorder full-frame display (The right end DP(1F) of time display is illuminated.)	
S157			Player A full-frame display	
S158			Player B full-frame display	
S160	to	S175	Player A key display	
S176	to	S191	Player B key display	
S192	to	S215	EDIT key display	
S216	to	S222	Cross-fade time display	(2 digits)

* "Hold" is displayed with decimal points.

Note: To display "Hold", the decimal point for the first 7 digits (except 1F) of Recorder time display is illuminated.

Table 7-13-3 Display Information

$S_n^{DSP} = \sum_{l=0}^{7} d_l 2^l$ $S_0^{DSP} - S_7^{O}$

d7 ~ d5 / d4 ~ d0	RECORDER TIME DISP 0 0 0	PLAYER A TIME DISP 0 0 1	PLAYER B TIME DISP 0 1 0	SEARCH DIAL DISP 0 1 1	KEY LED 1 0 0	KEY LED 1 0 1	KEY LED 1 1 0	1 1 1
0 0 0 0 0	10H, A	10H, A	10H, A	SEARCH, P0	RECORDER STOP	PLAYER STOP	EDIT IN	
0 0 0 0 1	B	B	B	P1	PAUSE	PAUSE	EDIT OUT	
0 0 0 1 0	C	C	C	P2	FWD	FWD	RECORDER	
0 0 0 1 1	D	D	D	P3	REVERSE	REVERSE	PLAYER	
0 0 1 0 0	1H, A	1H, A	1H, A	P4	FF	FF		
0 0 1 0 1	B	B	B	P5	REW	REW		
0 0 1 1 0	C	C	C	P6	REC	REC	SEARCH	
0 0 1 1 1	D	D	D	P7	AUTO LOCATE	AUTO LOCATE		
0 1 0 0 0	10M, A	10M, A	10M, A	P8	SPEED ×2	SPEED ×2	SEARCH MONITOR MIX	
0 1 0 0 1	B	B	B	P9	SPEED ×1	SPEED ×1	SEARCH MONITOR CH1	
0 1 0 1 0	C	C	C	P10	SPEED ×1/5	READER	SEARCH MONITOR CH2	
0 1 0 1 1	D	D	D	P11		USER'S BIT	SEARCH SPEED MANUAL	
0 1 1 0 0	1M, A	1M, A	1M, A	P12	ASSEMBLE	AUTO LOCATOR	SEARCH SPEED ×1	
0 1 1 0 1	B	B	B	P13	ANALOG CH2	PLAYER A	SEARCH SPEED ×1/2	
0 1 1 1 0	C	C	C	P14	ANALOG CH1	TIME CODE		
0 1 1 1 1	D	D	D	P15	VIDEO	SERVO		
1 0 0 0 0	10S, A	10S, A	10S, A	P16	GENERATOR	PLAYER B STOP	PREVIEW	
1 0 0 0 1	B	B	B	P17	* HOLD	PAUSE	AUTO EDIT	
1 0 0 1 0	C	C	C	P18	READER	FWD	REVIEW	
1 0 0 1 1	D	D	D	P19	USER'S BIT	REVERSE	P.R.T 5sec	
1 0 1 0 0	1S, A	1S, A	1S, A	P20	AUTO LOCATOR	FF	P.R.T 10sec	
1 0 1 0 1	B	B	B	P21		REW	P.R.T 30sec	
1 0 1 1 0	C	C	C	P22	TIME CODE	REC	TIME OFFSET IN	
1 0 1 1 1	D	D	D	P23	SERVO	AUTO LOCATE	TIME OFFSET OUT	
1 1 0 0 0	10F, A	10F, A	10F, A	P24		SPEED ×2	CROSS FADE 10msec A	
1 1 0 0 1	B	B	B	P25		SPEED ×1	B	
1 1 0 1 0	C	C	C	P26		READER	C	
1 1 0 1 1	D	D	D	P27		USER'S BIT	D	
1 1 1 0 0	1F, A	1F, A	1F, A	P28	*RECORDER NON-DROP-FRAME	AUTO LOCATOR	1msec A	
1 1 1 0 1	B	B	B	P29	*PLAYER A NON-DROP-FRAME	PLAYER B	B	
1 1 1 1 0	C	C	C	P30	*PLAYER B NON-DROP-FRAME	TIME CODE	C	
1 1 1 1 1	D	D	D	P31	0 dB	SERVO	D	

Table 7-13-4 Display Information

d. **FDDT (Fader data)**
Parallel fader data (FDDT 0 - 7) is converted into serial data and output by the RS-422 driver. The serial fader data consecutively and cyclically outputs FDDT 0 from the S_0 slot.

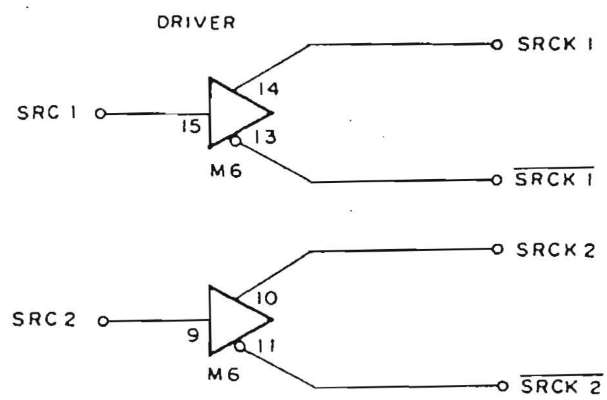
S_8n = data of FDDT0 n = 0, 1, 2....

$S_8n + 1$ = data of FDDT1

$S_8n + 7$ = data of FDDT7

e. **SRCCK 1 and SRCCK 2 (Search mode clock):**

SRCCK 1 and SRCCK 2 have no time relationship with CKTRS, SYNC, etc. SRC1 and SRC2 are output via the driver to become SRCCK1 and SRCCK2.



IC-M6
Am26LS31PC

7.13.4 FUNCTION OF EACH BLOCK

7.13.4.1 Timing Generator

The timing generator circuit is composed of a counter circuit producing the control addresses for the switch matrix circuit, display matrix circuit, etc. from the transmission clock CKTRS and transmission synch pulse SYNC.

Since key data and disply are transmitted or received in 256 bits, response to each slot is possible with the 8-bit counter. CKTRS has a 50% duty cycle, therefore, in the matrix circuit, CKTRS is one of the addresses.

The counter diagram is shown in Figure 7-122. CKTRS and SYNC are received by the EIA Standard RS-422 receiver (AM26LS32). Electrostatic protection is provided at the receiving end with a resistor and capacitor.

The counter is a synchronous clear counter (SN74LS163). SYNC is input to the clear terminal to dear the counter with the rising edge of the CKTRS pulse.

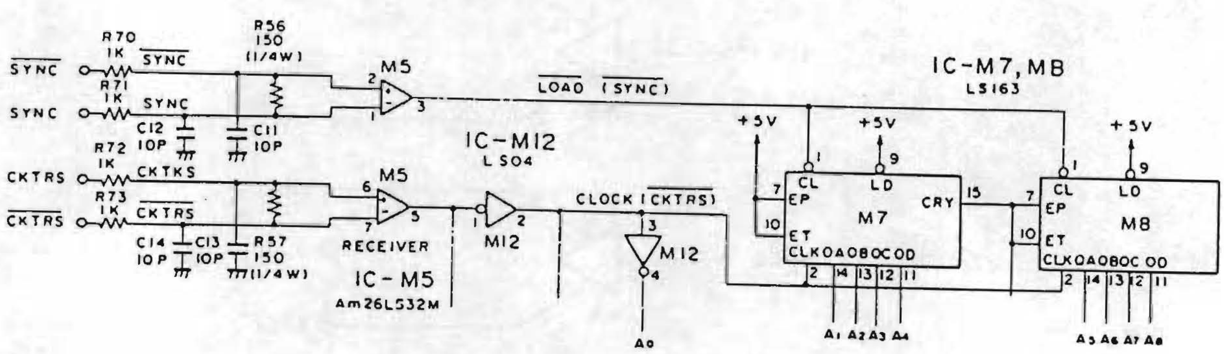


Figure 7-122 Timing Generator

7-13.4.1 Key Data Generator

A matrix is formed for keyboard switches key data is in 256 slots and each data function is defined. Therefore, the timing genrator counter output is used as the address. The last 3 bits (A_1 to A_8) form the column selector.

The key data generator circuit is shown in Figure 7-123. A row of the key matrix is divided into eight by the 3-to-8 line decoder (IC-M15:SN74LS156) and scanned in the direction of the row. In the column direction, a 4-block column is selected by the 4-line-to-1-line selector (IC-M17, M-18:SN74LS253) via the column address. The ten-key block is composed of IC-M32 and M36. These 5 blocks are scanned in the direction of a column by selecting a block with the 4-to-10-line decoder (IC-M16:SN74LS42).

The key data which has been decided by row and column is arranged in flip-flop (IC-M31:SN74LS74) and output in synch with the transmisssion clock CKTRS. The output data is sent to the main unit via RS-422 driver (IC-M6:Am26LS31).

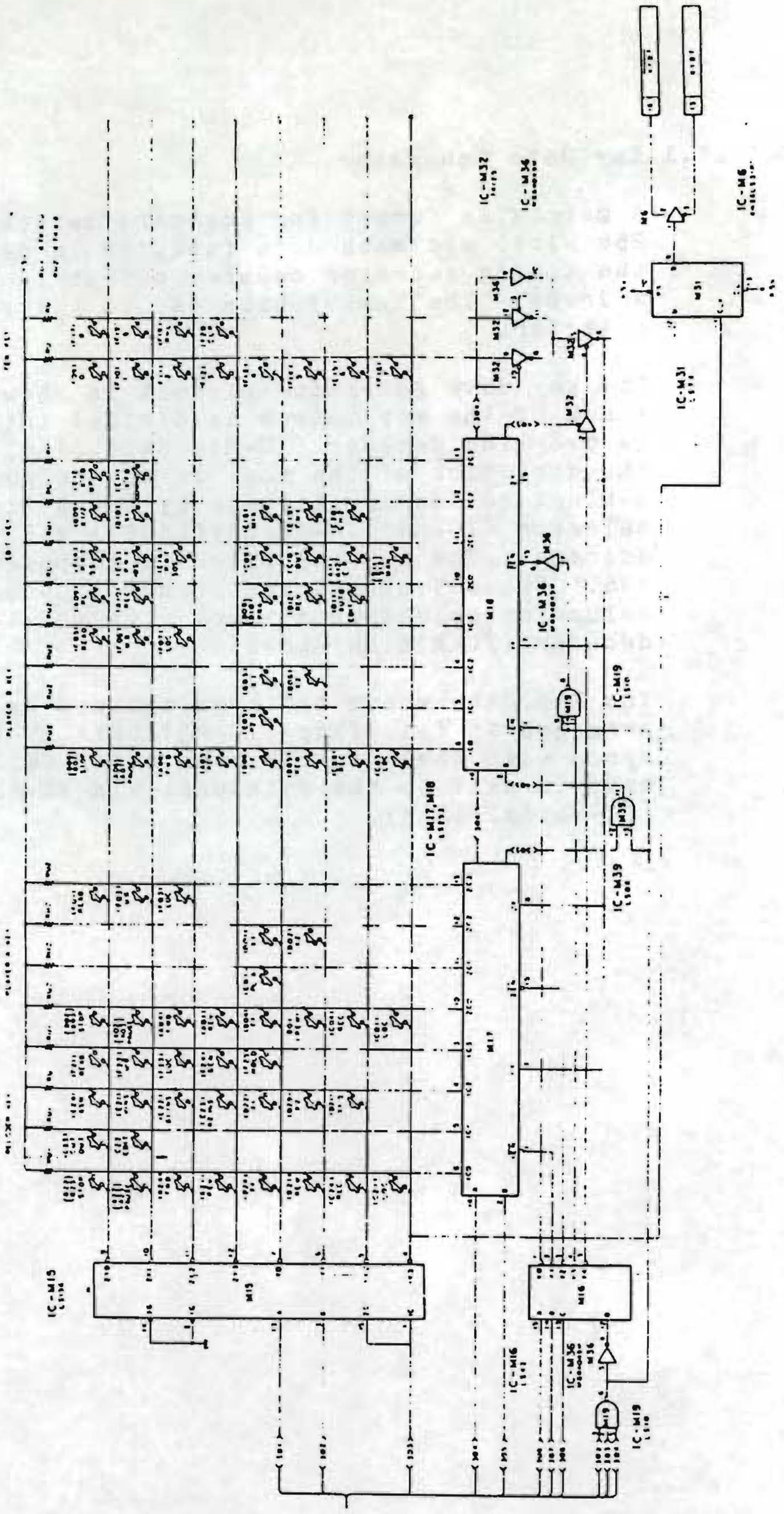


Figure 7-123 Key Data Generator

7.13.4.3 Display Circuit

As shown in Table 7-13-3, display data is serially transmitted from the Recorder time display data. Since there are many different data sources which are displayed in the display block, a time-sharing display is used to simplify the display driver. Accordingly, memory is used in the ciruit to control the display data timing. The timing chart is show in Figure 7-124, the circuit diagram is and of this section (2-*0 and the block diagram in Figure 7-125.

7.13.4.3.1 Display Data Store

This display data is received by the receiver (IC-M5: Am26LS32) which has a spurious input protection circuit. The data is converted by the 1-to-4-line S/P converter (IC-M11: SN74LS194), then stored in the 256-bit (64x4 bits) RAM. Writing address is in the sequence A_3 A_4 A_5 A_6 A_7 A_8. For reading, addresses A_3 A_4 A_5 A_0 A_1 A_2 are read from the relevant time-sharing block. Therefore, writing cycle is at 37.5Hz and reading cycle is at 300Hz so that there is no flicker. The read/write address selector is composed of IC-M9 (SN74LS157).

7.13.4.3.2 Display Data Latch Circuit

The 7-segment LED time display and the LED dot display are classified into VTR and Edit blocks. However, the display data read from RAM does not match the display timing. Thus a latch is installed to control the cathode of the display matrix. The latch circuit consists of a latch input for read data from RAM an output and that is actually controlling the cathode for display timing. The latch clock is supplied from the row address selector.

IC-M31 (SN74LS74) is a latch for developing 'Hold' by illuminating the decimal point LED for the Recorder time code generator, etc.

7.13.4.3.3 LED Anode and Cathode Drive Circuit

The time display and function display are composed of 8 columns and is anode driven. This is accomplished by decoding IC-M14:SN74LS145) addresses A_3 A_4 A_5. In the 8-column timing generator. The decoded output is supplied to the anode driver, which is a PNP transistor (2SA1020), to supply current to the anodes of the 7-segment LEDs and dot LEDs. The cathodes of the 7-segment LEDs are driven by 7-segment decoder (IC-M1, M2, SW-1 board, IC-M3, M4: SW-2 board).

7.13.4.3.3 LED Anode and Cathode Drive Circuit continued

The dot (decimal point) LED rows are controlled by the latch output with an open-collector inverter.

7.13.4.3.4 Display LED

The display block consisting of the 7-segment LEDs and dot LEDs are divided into 7 blocks as shown in Figure 7-125.

7-segment LEDs with common anodes are used and the data is displayed, time-shared for each digit.

The dot LEDs are separated into rows and columns. The anodes and cathodes are controlled by the matrix.

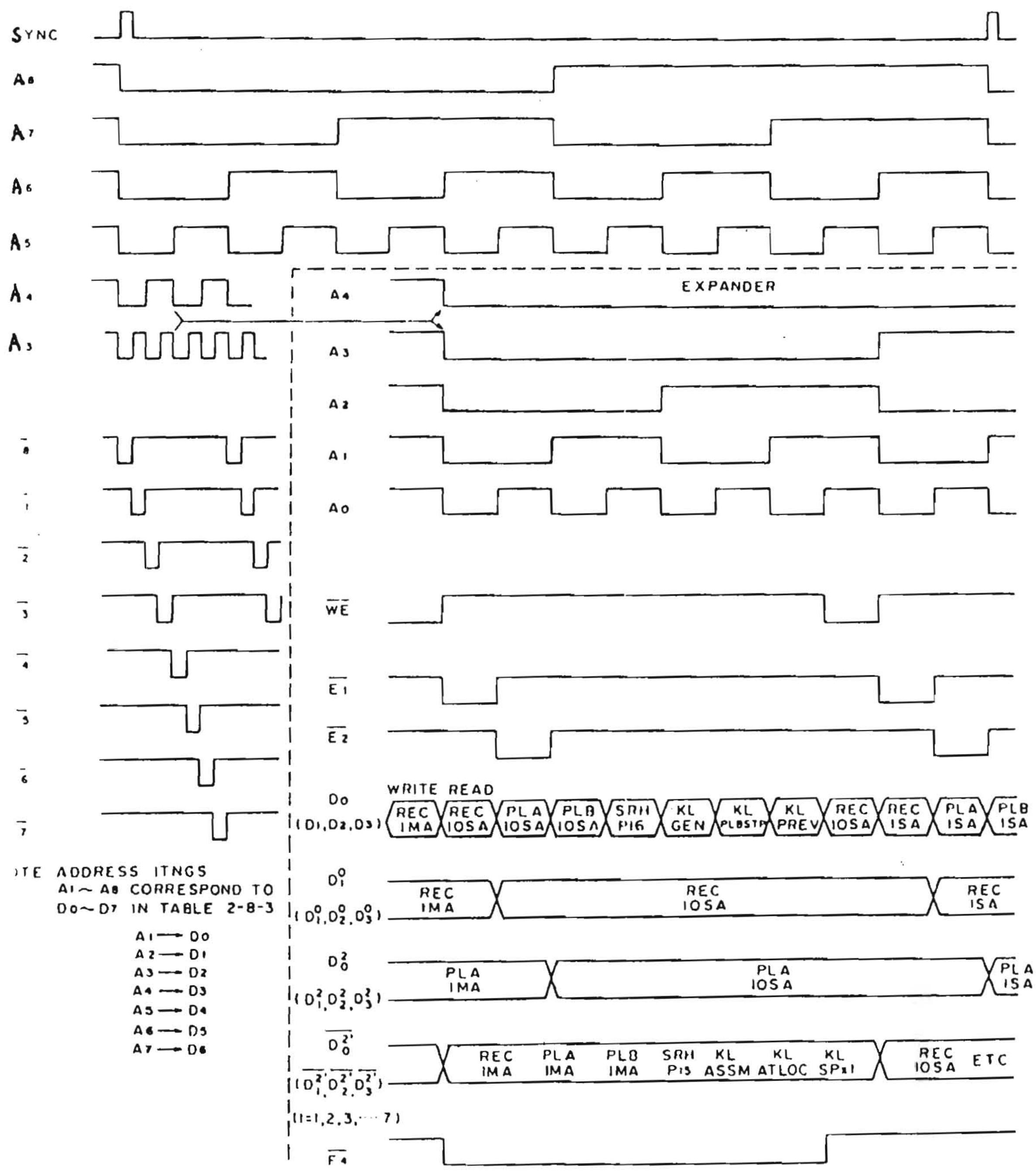


Figure 7-124 LED Display Timing Chart

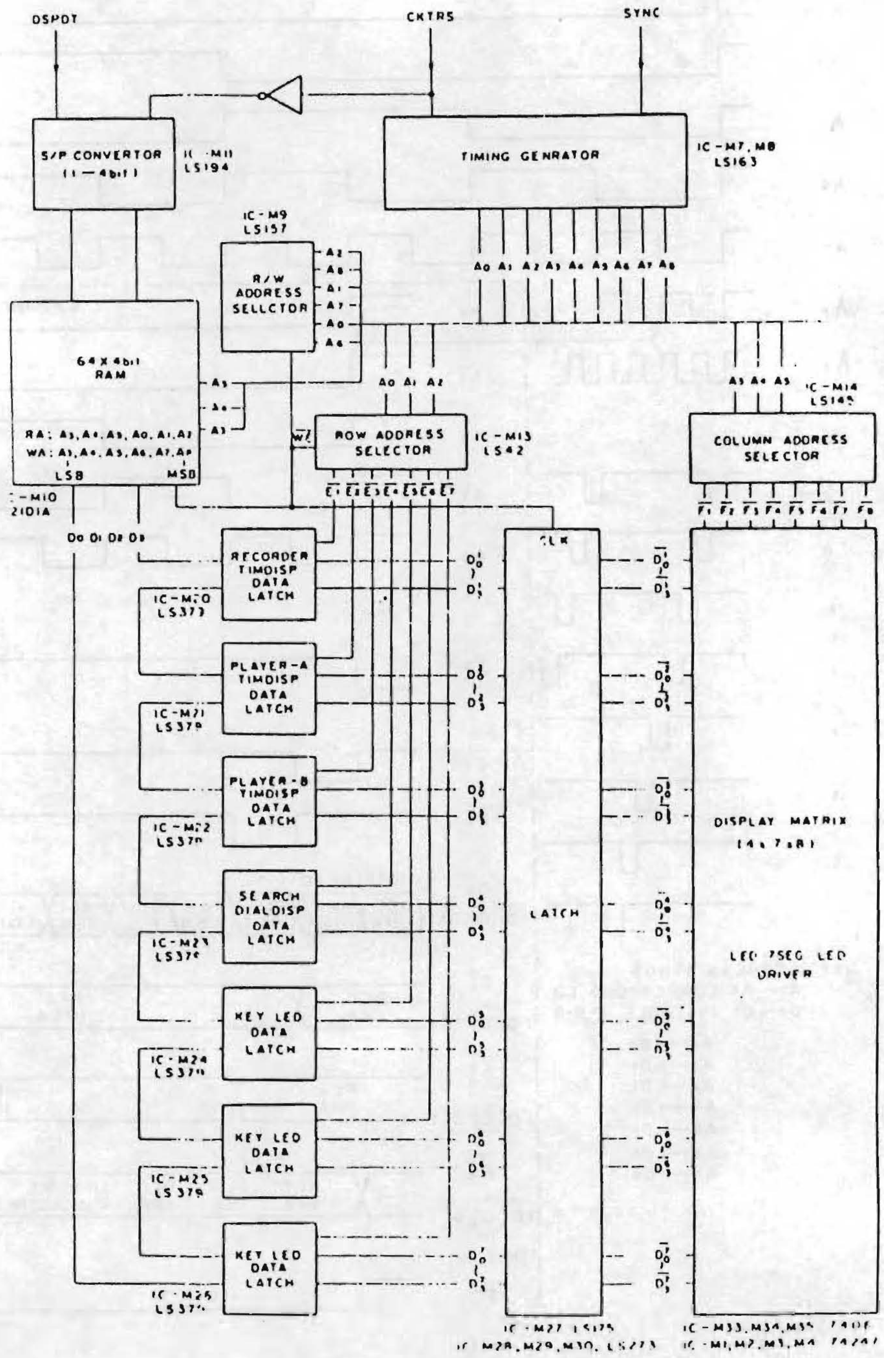


Figure 7-125 LED Display Block Diagram

7.13.4.4 Fader Data Output Circuit

The fader is outlined in Figure 7-126 and has an 8-bit digital output capacity. The oouput code is Gray code. If the fader position is changed by contact and non-contact segments. The circuit is not influenced by chatter, etc. for a bit change. The lowest level of the output code is 00000000 (short circuit to ground = 0) and the highest level is 10000000. Theoretical values of the fader output code are shown in Table 7-13-5.

Since the resistance of the 8-bit output of the fader at ON is high, the output is buffered by CMOS IC (IC-M36, M37) with a high "0" threshold level. The buffer output is loaded in the 8-bit shift register every 16 clock bits and the serial data is output from the LSB. The transmission timing is shown in Figure 7-120.

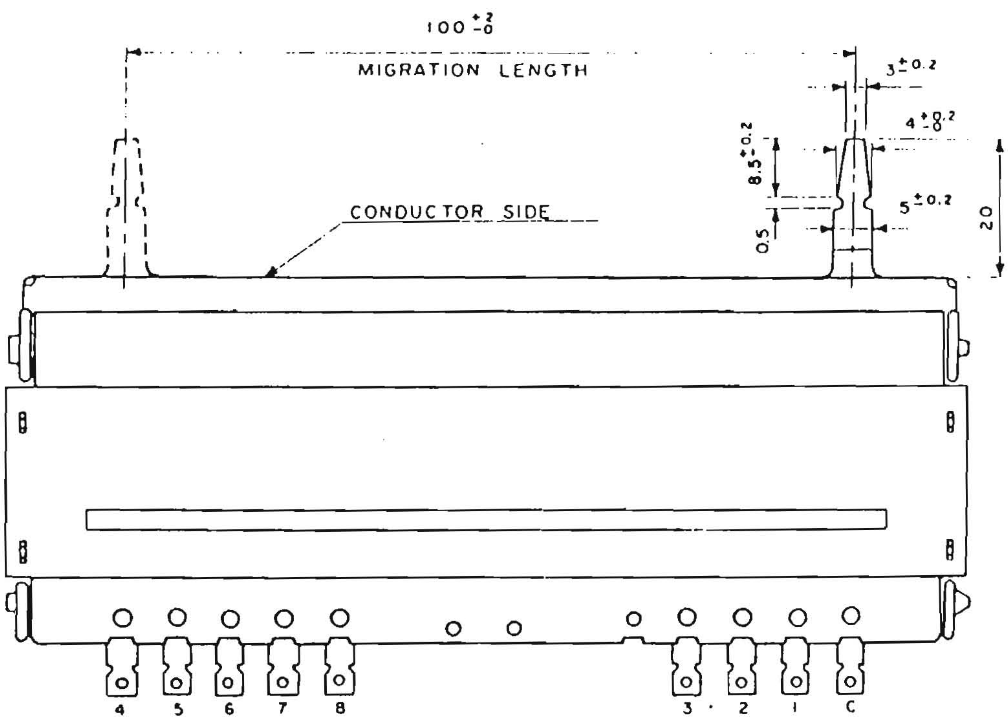


Figure 7-126 Multi Contact Switch

0:SHORT 1:OPEN

OUTPUT \ PIN	1	2	3	4	5	6	7	8
70	1	0	1	0	0	1	1	0
71	0	0	1	0	0	1	1	0
72	0	0	1	1	0	1	1	0
73	1	0	1	1	0	1	1	0
74	1	1	1	1	0	1	1	0
75	0	1	1	1	0	1	1	0
76	0	1	0	1	0	1	1	0
77	1	1	0	1	0	1	1	0
78	1	0	0	1	0	1	1	0
79	0	0	0	1	0	1	1	0
80	0	0	0	1	1	1	1	0
81	1	0	0	1	1	1	1	0
82	1	1	0	1	1	1	1	0
83	0	1	0	1	1	1	1	0
84	0	1	1	1	1	1	1	0
85	1	1	1	1	1	1	1	0
86	1	0	1	1	1	1	1	0
87	0	0	1	1	1	1	1	0
88	0	0	1	0	1	1	1	0
89	1	0	1	0	1	1	1	0
90	1	1	1	0	1	1	1	0
91	0	1	1	0	1	1	1	0
92	0	1	0	0	1	1	1	0
93	1	1	0	0	1	1	1	0
94	1	0	0	0	1	1	1	0
95	0	0	0	0	1	1	1	0
96	0	0	0	0	1	0	1	0
97	1	0	0	0	1	0	1	0
98	1	1	0	0	1	0	1	0
99	0	1	0	0	1	0	1	0
100	0	1	1	0	1	0	1	0
101	1	1	1	0	1	0	1	0
102	1	0	1	0	1	0	1	0
103	0	0	1	0	1	0	1	0
104	0	0	1	1	1	0	1	0

OUTPUT \ PIN	1	2	3	4	5	6	7	8
105	1	0	1	1	1	0	1	0
106	1	1	1	1	1	0	1	0
107	0	1	1	1	1	0	1	0
108	0	1	0	1	1	0	1	0
109	1	1	0	1	1	0	1	0
110	1	0	0	1	1	0	1	0
111	0	0	0	1	1	0	1	0
112	0	0	0	1	0	0	1	0
113	1	0	0	1	0	0	1	0
114	1	1	0	1	0	0	1	0
115	0	1	0	1	0	0	1	0
116	0	1	1	1	0	0	1	0
117	1	1	1	1	0	0	1	0
118	1	0	1	1	0	0	1	0
119	0	0	1	1	0	0	1	0
120	0	0	1	0	0	0	1	0
121	1	0	1	0	0	0	1	0
122	1	1	1	0	0	0	1	0
123	0	1	1	0	0	0	1	0
124	0	1	0	0	0	0	1	0
125	1	1	0	0	0	0	1	0
126	1	0	0	0	0	0	1	0
127	0	0	0	0	0	0	1	0
128	0	0	0	0	0	0	1	1
129	1	0	0	0	0	0	1	1
130	1	1	0	0	0	0	1	1
131	0	1	0	0	0	0	1	1
132	0	1	1	0	0	0	1	1
133	1	1	1	0	0	0	1	1
134	1	0	1	0	0	0	1	1
135	0	0	1	0	0	0	1	1
136	0	0	1	1	0	0	1	1
137	0	0	1	1	0	0	1	1
138	0	1	1	1	0	0	1	1
139	0	1	1	1	0	0	1	1

Table 7-13-5A Theoretical Values of Output Codes

0:SHORT 1:OPEN

OUTPUT \ PIN	1	2	3	4	5	6	7	8
140	0	1	0	1	0	0	1	1
141	1	1	0	1	0	0	1	1
142	1	0	0	1	0	0	1	1
143	0	0	0	1	0	0	1	1
144	0	0	0	1	1	0	1	1
145	1	0	0	1	1	0	1	1
146	1	1	0	1	1	0	1	1
147	0	1	0	1	1	0	1	1
148	0	1	1	1	1	0	1	1
149	1	1	1	1	1	0	1	1
150	1	0	1	1	1	0	1	1
151	0	0	1	1	1	0	1	1
152	0	0	1	0	1	0	1	1
153	1	0	1	0	1	0	1	1
154	1	1	1	0	1	0	1	1
155	0	1	1	0	1	0	1	1
156	0	1	0	0	1	0	1	1
157	1	1	0	0	1	0	1	1
158	1	0	0	0	1	0	1	1
159	0	0	0	0	1	0	1	1
160	0	0	0	0	1	1	1	1
161	1	0	0	0	1	1	1	1
162	1	1	0	0	1	1	1	1
163	0	1	0	0	1	1	1	1
164	0	1	1	0	1	1	1	1
165	1	1	1	0	1	1	1	1
166	1	0	1	0	1	1	1	1
167	0	0	1	0	1	1	1	1
168	0	0	1	1	1	1	1	1
169	1	0	1	1	1	1	1	1
170	1	1	1	1	1	1	1	1
171	0	1	1	1	1	1	1	1
172	0	1	0	1	1	1	1	1
173	1	1	0	1	1	1	1	1
174	1	0	0	1	1	1	1	1

OUTPUT \ PIN	1	2	3	4	5	6	7	8
175	0	0	0	1	1	1	1	1
176	0	0	0	1	0	1	1	1
177	1	0	0	1	0	1	1	1
178	1	1	0	1	0	1	1	1
179	0	1	0	1	0	1	1	1
180	0	1	1	1	0	1	1	1
181	1	1	1	1	0	1	1	1
182	1	0	1	1	0	1	1	1
183	0	0	1	1	0	1	1	1
184	0	0	1	0	0	1	1	1
185	1	0	1	0	0	1	1	1
186	1	1	1	0	0	1	1	1
187	0	1	1	0	0	1	1	1
188	0	1	0	0	0	1	1	1
189	1	1	0	0	0	1	1	1
190	1	0	0	0	0	1	1	1
191	0	0	0	0	0	1	1	1
192	0	0	0	0	0	1	0	1
193	1	0	0	0	0	1	0	1
194	1	1	0	0	0	1	0	1
195	0	1	0	0	0	1	0	1
196	0	1	1	0	0	1	0	1
197	1	1	1	0	0	1	0	1
198	1	0	1	0	0	1	0	1
199	0	0	1	0	0	1	0	1
200	0	0	1	1	0	1	0	1
201	1	0	1	1	0	1	0	1
202	1	1	1	1	0	1	0	1
203	0	1	1	1	0	1	0	1
204	0	1	0	1	0	1	0	1
205	1	1	0	1	0	1	0	1
206	1	0	0	1	0	1	0	1
207	0	0	0	1	0	1	0	1
208	0	0	0	1	1	1	0	1
209	1	0	0	1	1	1	0	1

Table 7-13-5B

0:SHORT 1:OPEN

OUTPUT \ PIN	1	2	3	4	5	6	7	8
210	1	1	0	1	1	1	0	1
211	0	1	0	1	1	1	0	1
212	0	1	1	1	1	1	0	1
213	1	1	1	1	1	1	0	1
214	1	0	1	1	1	1	0	1
215	0	0	1	1	1	1	0	1
216	0	0	1	0	1	1	0	1
217	1	0	1	0	1	1	0	1
218	1	1	1	0	1	1	0	1
219	0	1	1	0	1	1	0	1
220	0	1	0	0	1	1	0	1
221	1	1	0	0	1	1	0	1
222	1	0	0	0	1	1	0	1
223	0	0	0	0	1	1	0	1
224	0	0	0	0	1	0	0	1
225	1	0	0	0	1	0	0	1
226	1	1	0	0	1	0	0	1
227	0	1	0	0	1	0	0	1
228	0	1	1	0	1	0	0	1
229	1	1	1	0	1	0	0	1
230	1	0	1	0	1	0	0	1
231	0	0	1	0	1	0	0	1
232	0	0	1	1	1	0	0	1
233	1	0	1	1	1	0	0	1
234	1	1	1	1	1	0	0	1
235	0	1	1	1	1	0	0	1
236	0	1	0	1	1	0	0	1
237	1	1	0	1	1	0	0	1
238	1	0	0	1	1	0	0	1
239	0	0	0	1	1	0	0	1
240	0	0	0	1	0	0	0	1
241	1	0	0	1	0	0	0	1
242	1	1	0	1	0	0	0	1
243	0	1	0	1	0	0	0	1
244	0	1	1	1	0	0	0	1

OUTPUT \ PIN	1	2	3	4	5	6	7	8
245	1	1	1	1	0	0	0	1
246	1	0	1	1	0	0	0	1
247	0	0	1	1	0	0	0	1
248	0	0	1	0	0	0	0	1
249	1	0	1	0	0	0	0	1
250	1	1	1	0	0	0	0	1
251	0	1	1	0	0	0	0	1
252	0	1	0	0	0	0	0	1
253	1	1	0	0	0	0	0	1
254	1	0	0	0	0	0	0	1
255	0	0	0	0	0	0	0	1

Table 7-13-5C

7.13.4.5 Search Clock Generator

As shown in Figure 127, this section consists of a rotor plate (glass) which rotates directly connected to the dial knob, a stator plate (glass). two LED's (on SD board) and two photocells. This section outputs signals with a frequency proportional to the speed and has a 90° phase difference corresponding to the direction of rotation.

On the rotor, 1,000 slit teeth are engraved and, on the stator, two sets of slit windows are cut out so that the pitch is the same as that of the rotor but the pahse changed by 90°.

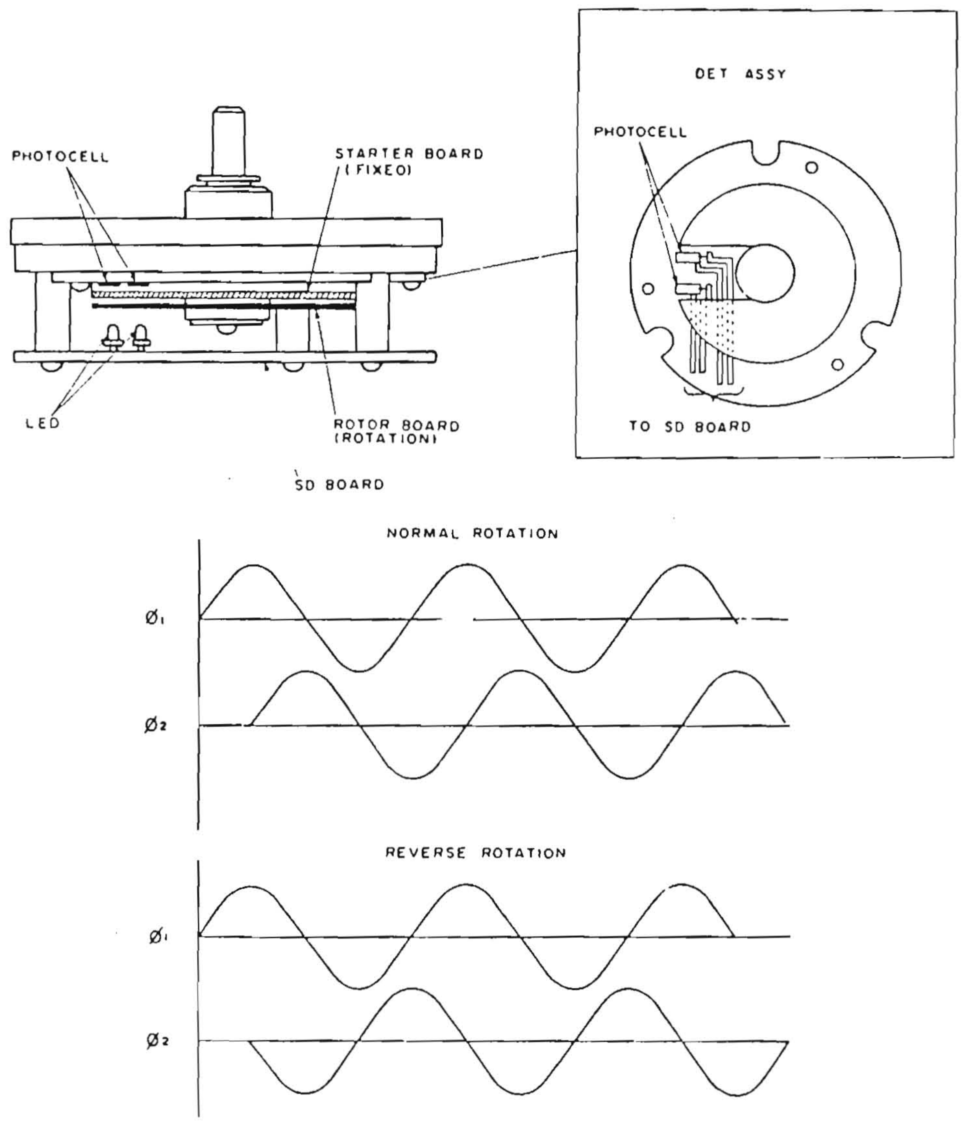


Figure 7-127 Search Dial Lock Generator

Light from the LED's passes through the rotor and stator and is received by the photocell, amplified by the amplifier installed on the SD Board and output. The circuit diagram is shown in Figure 7-128.

The SR-PW board is driven by the first stage differential amplifier IC201 which receives the photocell output and by the second stage amplifier IC202. Gain is adjusted with VR201 and VR251. C201,C251,C202 and C252 are AC coupling capacitor. R206-C203 and R256-C253 make a filter to remove high-frequency noise.

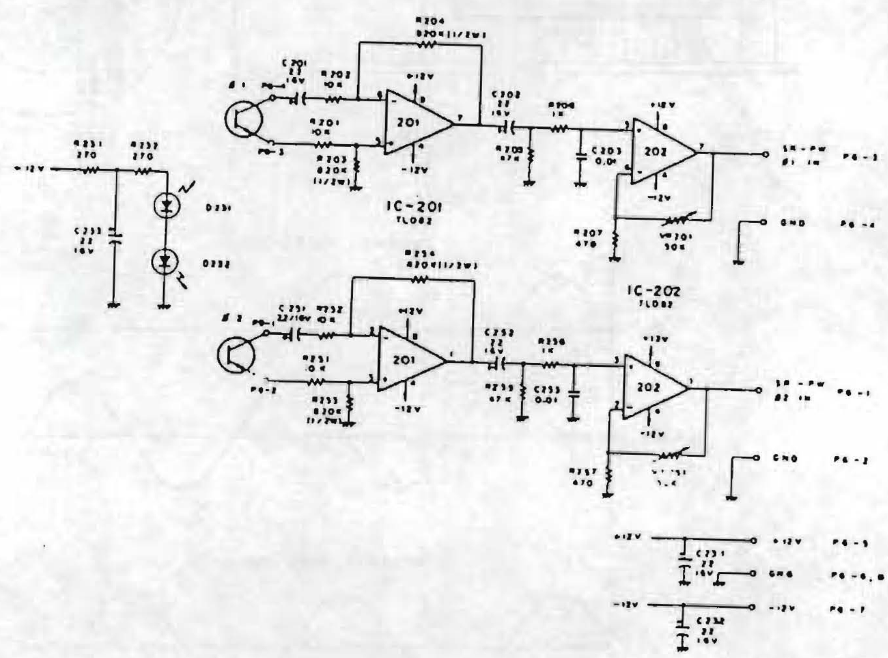


Figure 7-128 Search Clock Generator Circuit (SD Board)

7.13.4.6 Search Clock Waveform Shaping Circuit

This circuit is to shape the two (0_1 and 0_2) search dial outputs, coming from the SD board, into a square wave. The circuit diagram is shown in Figure 2-8-11.

The SD board output contains bias and amplitude variations resulting from center or face deflection of the stator.

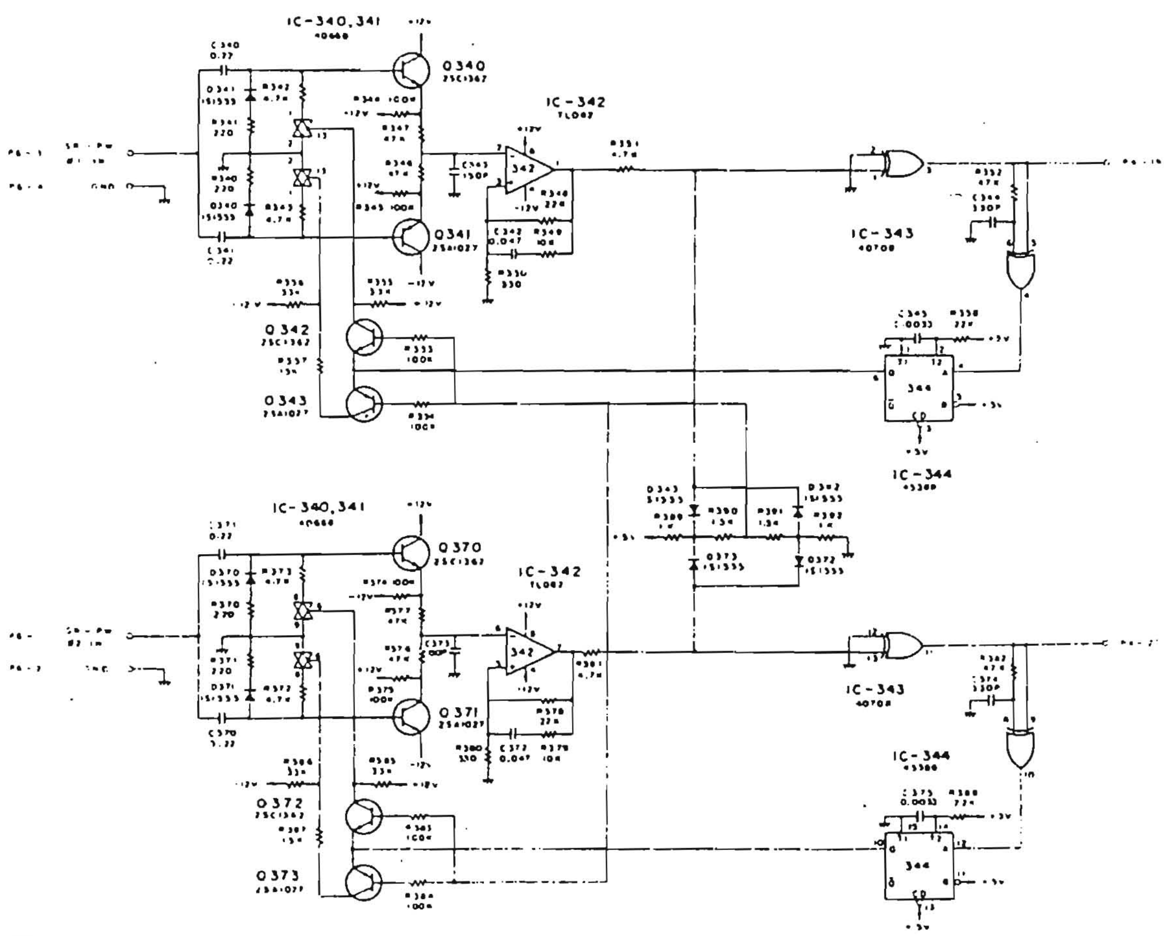


Figure 7-129 Search Clock Waveform Shaping Circuit (SD Board)

If this output is changed to a square wave without correction in the comparator, jitter occurs due to these bias and amplitude variations the search sound will contain a high level of flutter.

When this input signal is passed through the positive peak clamp circuit and negative peak clamp circuit as show in Figure 7-130, the amplitude variations becomes symmetrical. When this signal is delivered to the comparator, a square wave with no jitter can be obtained. The wave form is shown in Figure 7-131.

Positive feedback is applied to the plus input of the comparator via R378, C372, R379 and R380 to prevent the comparator input oscillating close to the point of 0 Volt crossing (dynamic schmitt trigger circuit).

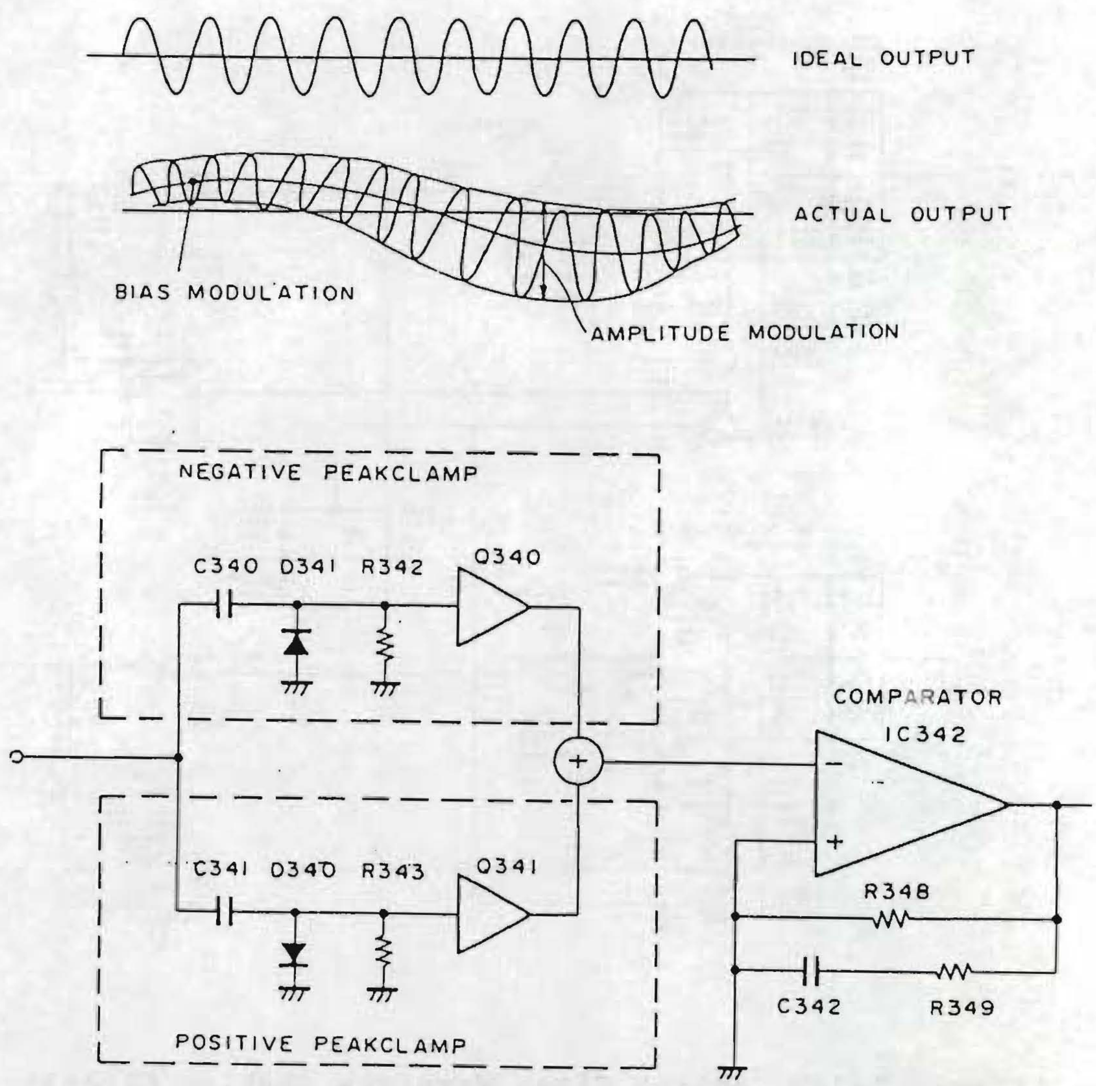


Figure 7-130 Peak Clamp Circuit

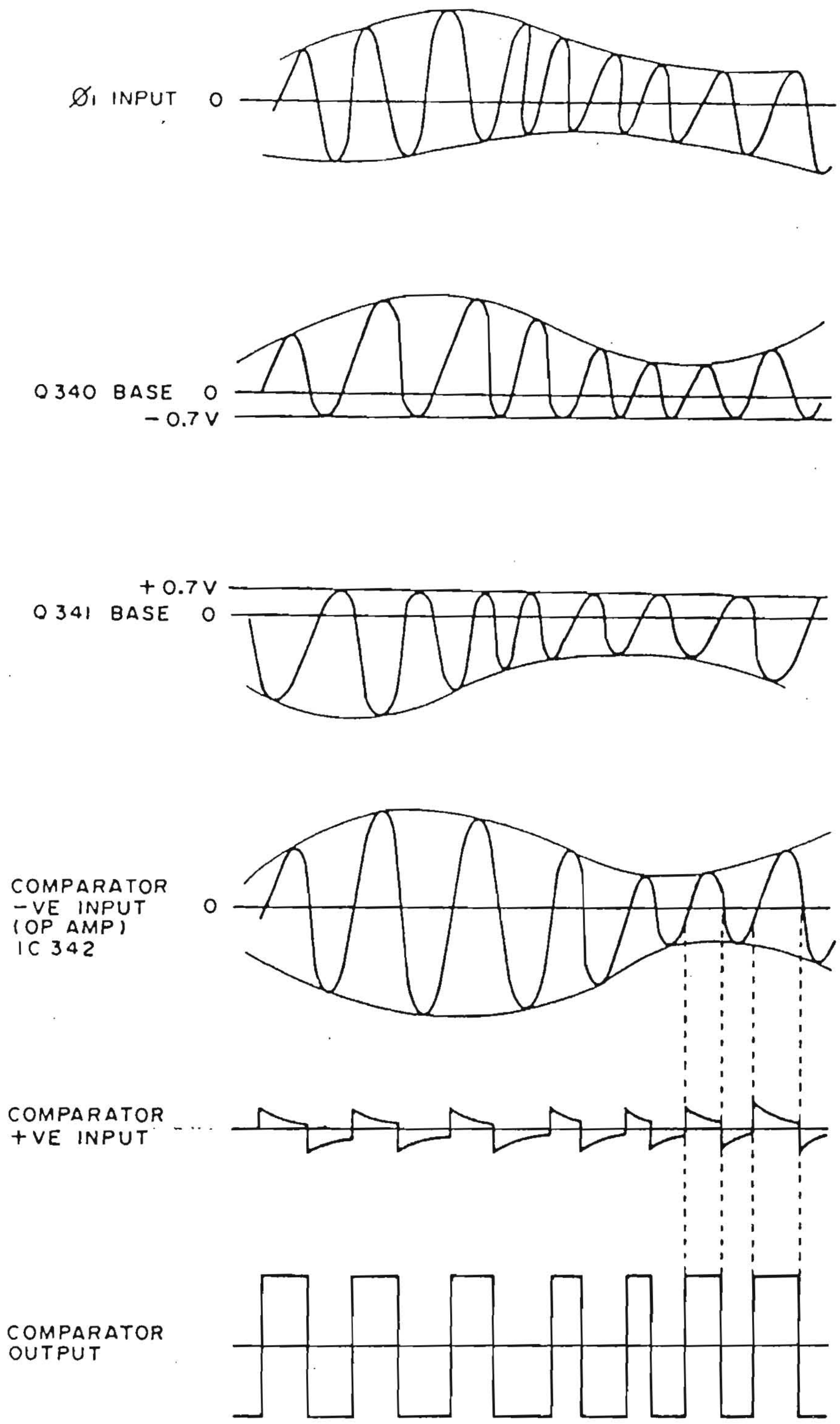


Figure 7-131 Waveform of Peak Clamp and Comparator

7.13.4.6 **Search Clock Waveform Shaping Circuit** (continued)

01 and 02 are not constant frequency, but change in po=roportion to the speed (from 1/500 speed to triple speed; about 6-Hz to 10kHz). Therefore, the positive peak clamp and negative peak clamp must operate correctly. Accordingly, the discharge time constant C_{341} x (R_{342}, IC_{340}) and C_{341} x (R_{343} x C_{341}) must be in inverse proportion to the period.

Therefore, the leading edge of comparator IC342 output goes via R352, C344 and IC343 and triggers monostable multivibrator IC-344, thenopens the analog switches IC340 and IC341 for a certain period of time (C_{345} x R_{358} = 70usec) and is discharged through R_{342} and R_{343}. This results in a discharge time constant circuit which is effectively proportional to the period of 01. The wave form is shown in Figure 7-132.

R351, D343 and D342 form a level shifter for

$$\pm 10V \quad \begin{matrix} +4.7V \\ +7.3V \end{matrix}$$

Since IC340 is operated at

$$\left.\begin{matrix} 0V \\ -12V \end{matrix}\right]$$

the control voltage of IC340 and IC341 is obtained by converting

$$\begin{matrix} +5V \\ \downarrow \\ 0V \end{matrix} \quad \text{To} \quad \begin{matrix} +12V \\ \downarrow \\ 0V \end{matrix} \quad \text{in Q342}$$

and

$$\begin{matrix} +5V \\ \downarrow \\ 0V \end{matrix} \quad \text{To} \quad \begin{matrix} 0V \\ \downarrow \\ -12V \end{matrix} \quad \text{in Q343}$$

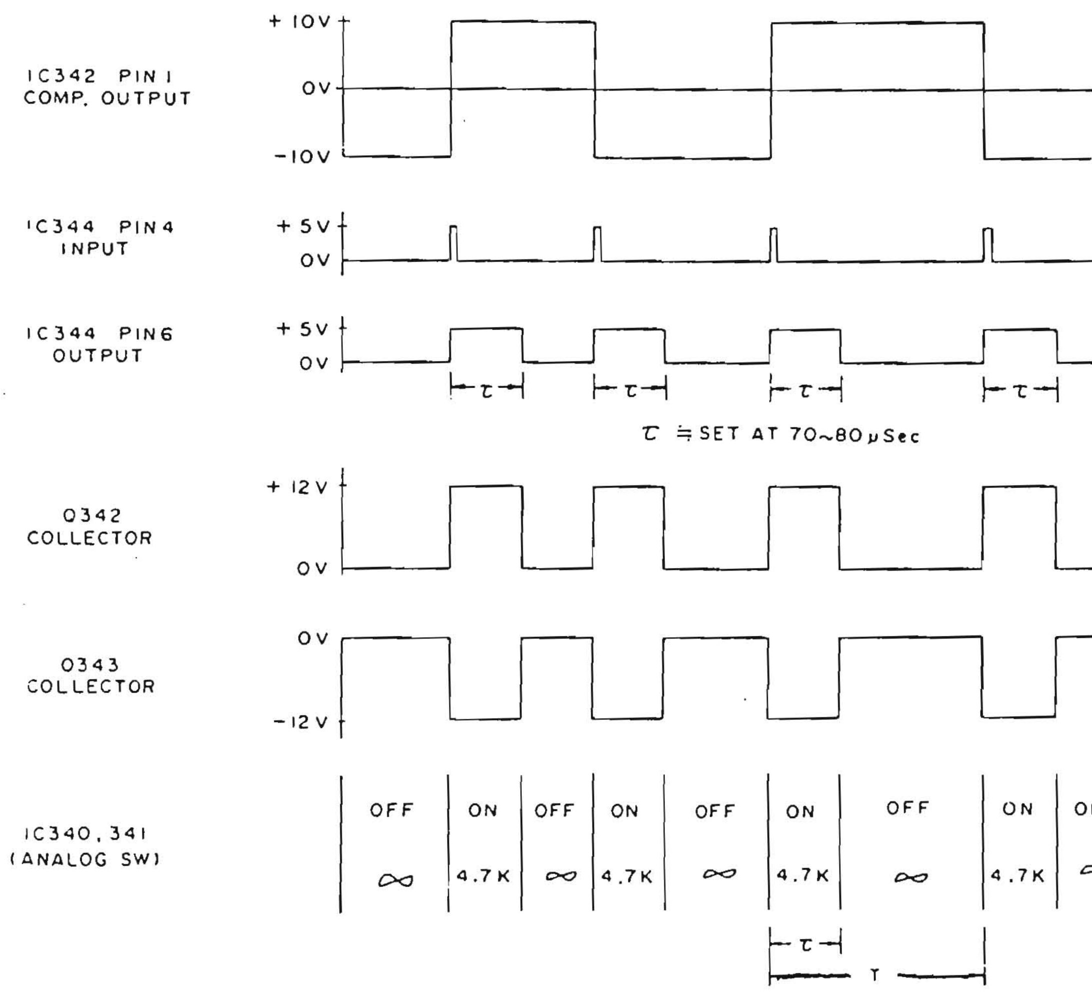


Figure 7-132 Search Clock Waveform Shaping Timing Chart

7.13.4.7 Keyboard Power Supply Circuit

The keyboard is supplied with DC voltage in the range 15_{-1} V +4 from the main unit. From this power, three power supplies - +5V and ±12V - to be used in the keyboard are produced by the switching DC-DC converter. The current capacity of the output is as follows.

Output voltage	Output current capacity
+5 V	3 A
+12 V	40 mA
-12 V	40 mA

7.13.4.7.1 Principle of Switching Regulator Operation

The switching constant voltage power supply hs high conversion efficiency. The principle of the switching regulator operation can be explained by the basic circuit shown in Figure 7-133.

In Figure7-133, Q_1 is a switching transistor and switches ON and OFF at a frequency and duty ratio to keep the output stationary. Therefore, when the circuit is controlled, transistor Q_1 is in the ON condition, and otherwise, in the OFF condition.

Diode D_1 is a catching diode. When Q_1 is in the OFF condition, it forms the currnet path for the inductance L.

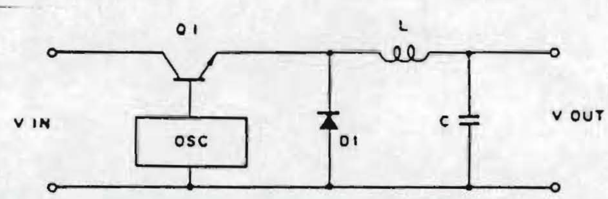


Figure 7-133 Switching Regulator (Basic Circuit)

When Q_1 is in the ON condition, input voltage V_{IN} is supplied to the L - C circuit and current I_1 flows. When Q_1 is in OFF condition, the energy stored in L is supplied to the load through D_1. L and C smooth the input. The output voltage is determined by the following formula

$$V_{OUT} = V_{IN} \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_{IN} \frac{T_{ON}}{T}$$

7.13.4.7.2 +5V Power Supply Circuit

The composition of the +5V DC-DC converter is basically the same as that described in (7-1). TL494 is used as a switching regulator IC. The block diagram of TL494 is shown in Figure 7-134. As shown in this figure, the following circuits are integrated in L494.

(i) 5 V reference power:
For a 7 to 40 V input, a 5 V refernce having a stability of less than 25 mV is supplied.

(ii) Oscillator:
In the oscillator, saw-tooth waves are produced by external resistance R_T and capacitor C_T. Oscillation frequency is fosc = $1/GR_T$.

(iii) Dead time and PWM comparators:
The IC composition of both comparators is same. The dead time comparator can set the switch OFF time of the output trdansistor. The PWM comparator compares the control voltage from the error amplifier output (pin 3) with the lamp voltage of the oscillator, then modulates the output pulse width.

(iv) Error amplifier:
This is a high gain amplifier which controlls the ON/OFF intervals of the ouput transistor.

(v) Output control circuit:
This cirucit can control the operation of two transistors either in parallelor push-pull. The maximum output current for the transistor is 200 mA.

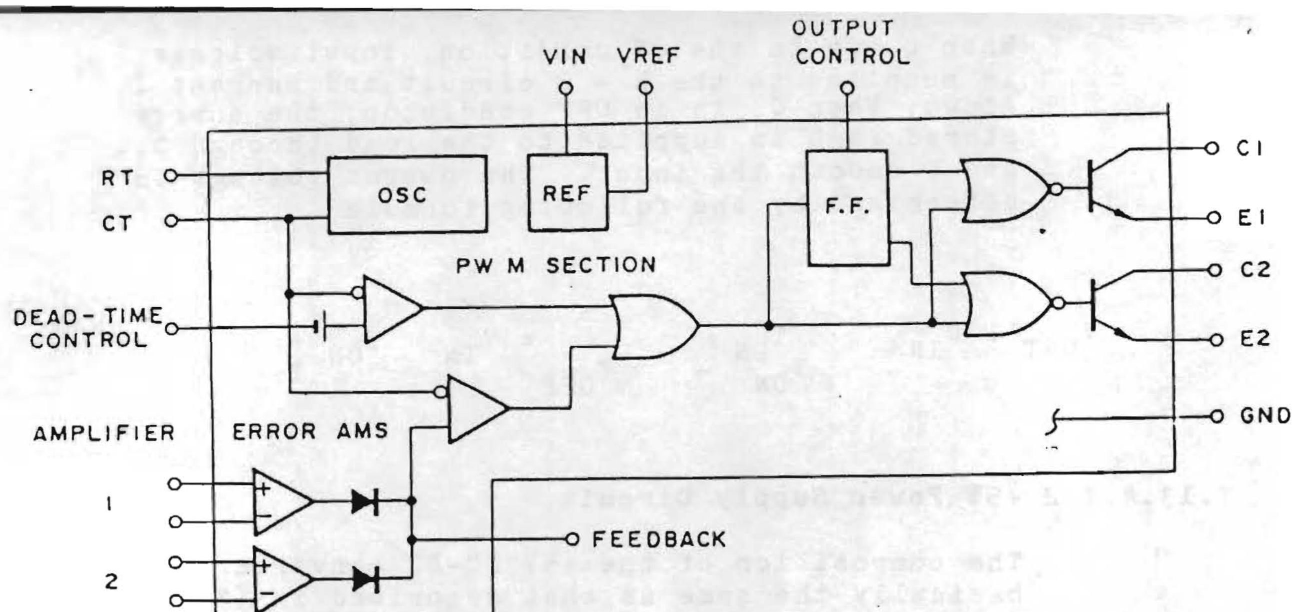


Figure 7-134 TL494 Block Diagram

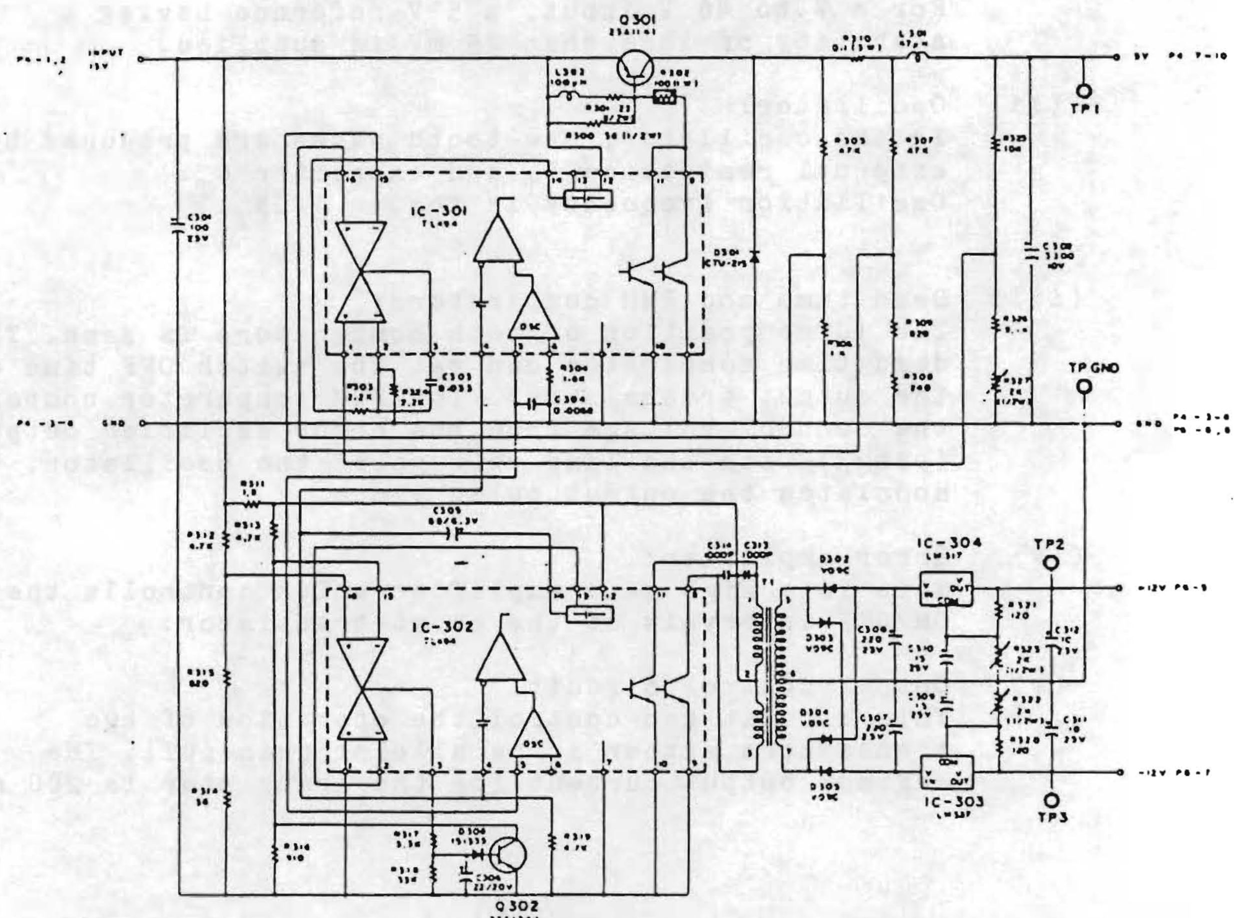


Figure 7-135 Keyboard Power Supply Circuit

7.13.4.7.2 +5V Power Supply Circuit continued

Since TL494 has functions as a switching regulator, it can fully control switching transistor Q301. Through the 5V line, the feedback for overcurrent protection and voltage regulation is input to error amplifier TL494. In the overcurrent protection circuit, the input to the error amplifier is changed by the voltager drop at R310 to change the switching duty cycle. Overcurrent protection operates when the current exceeds 3 A likewise, by comparing with 5V reference, voltage regulation is accomplished by changing the duty cycle. The oscillating frequency of the switching section is a follows:

$$fosc = \frac{1}{CTRT} = \frac{1}{0.0068uF X\ 1.6k\Omega} = 92kHz$$

Since the switching is single end operation, the output freqeuncy is 92 kHz. The output voltage is smoothed by L301 and C302 to obtain a stable 5 V output. The circuit is shown in Figure 7-135.

7.13.4.7.2 ±12V Power Supply Circuit

The ±12V power supply circuit, TL494 is used for switching control. Synchronized operation is made in the oscillator circuit using the oscillation output of the +5V powr supply. The output transistors in push-pull drive the convertor transformer. The current capacity of the ±12V power supply is ±40mA. Therefore, the output transistor TL494 i used to drive the converter transofrmer. Because of push-pull operation, the output frequency is 46kHz.

The converter transformer secondary output is stepped up in the ratio of 3 : 4 and rectified into plus andminus voltages. The rectified voltage is not fed back to the switching section. There, the voltage is not stablized. Accordingly, a stablized ±12V power supply is obtained using a 3-terminal regulator (IC-304: LM-317, IC-303: LM337). Output voltage regulation is attained by changing the electric potential of the common terminal of the 3-terminal regulator.

A 0.8A (typical) current limiting circuit is incorporated in the ±12V 3-terminal regulator in the overcurrent

protection circuit. However, since the TL494's output transistor cannot drive the output, overcurrent protection is made on the primary side with the voltage difference across R311. In the protection circuit, the voltages across R311 (1.8 Ohm) are input to the error amplifier, and the output is inoput to the base of Q302. When an overcurrent flows, the - input (terminal 15) level at the error amplifier decreases and the output (terminal 3) level increases. When the level determined by R_{317} and R_{318} exceeds V_F for the D_{306} and V_{BE} for Q_{302}, Q302 turns ON and increases the error amplifier output taking the - input to the error amplifier as GND level, and a flip-flop is formed. Once the overcurrent protection circuit operates, test is not possible unless the power supply switch is opened. In the overcurrent protection circuit C306 absorbs the undefined output level of the error amplifier ar power supply ON condition via the time constant R_{3127} and C_{306} to prevent malfunctioning of the overcurrent protection circuit. The circuit diagram is shown in Figure 7-135.

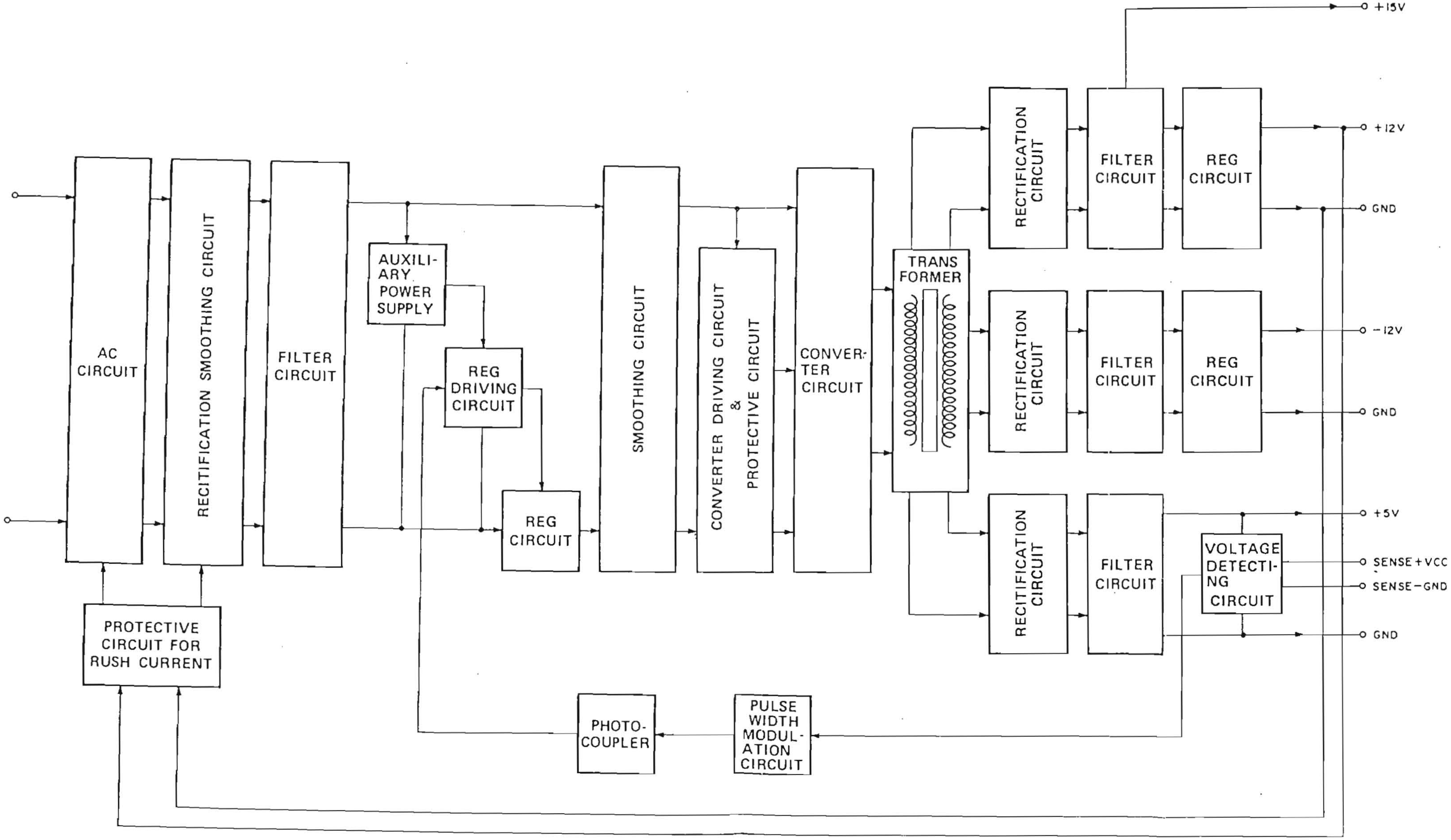


Figure 7-136 Block Diagram of Power Supply Circuit

FULL SUPPLY CIRCUIT (PLPS BOARD BLOCK DIAGRAM

7.14 PCPS BOARD

7.14.1 AC CIRCUIT

The power supply operates normally for the input ranges from AC 90V to 132V and from AC 198V to 264V due to changing the connections of the terminal board.

In the case of each input is applied to the terminalboard Nos. 3 and 7 for the input from AC 90V to 132V, and to the terminalbaord NBos. 4 and 7 for the input from AC 198V to 264V, 95V AC power is obtained to the output of an auto-transformer T_1, and the power supply circuit works with the actuation of a switching relay RY_1.

On the other hand, the power supply circuit is designed to supply the same voltage by means of the voltage doubler due to the short circuit of the terminal board Nos. 7 and 8 for the input from AC 90V to 132V, and the full-wave retification due to the open circuit of the terminal board Nos. 7 and 8 for the input from AC198V to 264V.

7.14.2 PROTECTIVE CIRCUIT FOR RUSH CURRENT

As the cement resistors R_1 and R_2 are connected in AC line to the series, the rush current is regulated to less than 25A even if the switch is turned on in case of the input 264V.

The power supply circuit operates and when the output comes to 12V, the cement resistors R_1 and R_2 generate the heat, but a temperature fuse F_1 adhered to the resistors is melted and cut by the heat, and the circuit is protected.

7.14.3 RECTIFICATION SMOOTHING CIRCUIT

AC is rectified by a diode D_1 being smoothed by the electrolytic condensers C_2 and C_3, and then it is converted into DC.

In case of the input from AC 90V to 132V, the voltage doubler is effected, and in case of the input AC 198V to 264V, the full-wave rectification is performed.

7.14.4 FILTER CIRCUIT

The chokes and condensers compose the low-pass filter, which reduces the common and normal modes noise.

7.14.5 AUXILIARY POWER SUPPLY

The auxiliary power supply circuit is the circuit which produces the power supply to drive REG Tr Q_4 and Q_5, and its output is stabilized at 5V.

This circuit is composed of the constant-voltage circuit with R_{29}, R_{30}, Q_7, Q_8, D_7, ZD_1, and the stable output of 15V is taken out to the emitter of Q_7. Furthermore, the constant-voltage circuit is formed by R_{33}, R_{34}, R_{35}, ZD_2, Q_{10}, Q_{11}, and the stable output 5V produced to the emitter of Q_{11} comes to the power supply which drives REG Tr Q_4 and Q_5.

REG Tr Q_4 and Q_5 turn on by this auxiliary power supply, and when the converter oscillates, approximately 20V of DC voltage full-wave-rectified by D_8 and C_{18} through the auxiliary winding of the converter transformer is supplied to the emitter of Q_7, which turns off so that Q_7 can be reversed biased.

In other words, when the protective circuit operates, the input of the auxiliary power supply becomes supplied from the converter.

When the protective circuit works, the oscillation of the converter stops, and Q_7 turns on again so that the voltage from the auxiliary winding can not be supplied. Consequently, the input of the auxiliary power supply is supplied from the DC power line, and Q_7 generates the heat.

In order to prevent the generation of this heat, before the input voltage becomes normal, Q_9 short-circuits ZD_1, and therefore Q_7 turns off.

7.14.6 REG DRIVING CIRCUIT

The signal pulse-modulated through a photo-coupler is supplied to the base Q_2, being amplified and waveform-arranged by Q_2 and Q_3, and then the signal of the perfect square-wave is impressed at the base of REG Tr Q_4 and Q_5, consequently the switching is performed.

7.14.7 REG CIRCUIT (I)

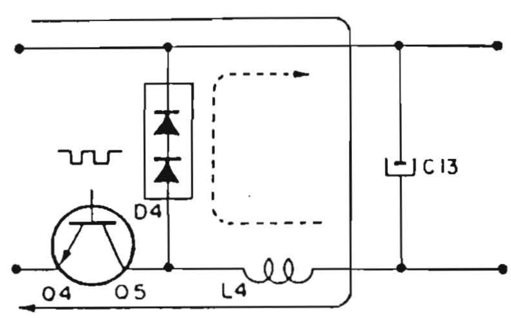
This circuit switches Q_4 and Q_5 due to receiving the signal of the square waveform from the REG driving circuit.

The best driving condition is always given according to flowing the over-driving current by D_3 because the drive the constant-voltage is achieved, and when the transistors Q_4 and Q_5 turn off, the storage time shortens due to flowing out the base current by L_3.

7.14.8 SMOOTHING CIRCUIT

When REG Tr Q_4 and Q_5 turn on, the current flows to C_{13} and L_4 as shown in a solid line and the magnetic energy is accumulated to L_4.

Whereas, when the turning off, the magnetic energy stored to L_4 is dischaged through L_4, D_4 and C_{13} as shown in a dotted line. With repeating the aforementioned state, the switching of Q_4 and Q_5 is smoothed, and the voltage of the both ends of C_{13} is converted into the direct current.



Solid line : ON state of Q4 and Q5
Dotted line : OFF state of Q4 and Q5

7.14.9 CONVERTER DRIVING CIRCUIT

When REG circuit turns on, the voltage is supplied to the converter driving circuit. This voltage is divided by R_{50}, R_{52} and R_{53}, and when the voltage impressed to the both ends of R_{53} reaches Zener voltage of the V_{BE} + ZD_5 of Q_{20} and Q_{19} and Q_{20} connected to a thyristor turn urgently on.

C_{37} is charged by the voltage of the both ends of R_{52} + R_{53}, but, when Q_{19} and Q_{20} turn on, the discharge occurs in sequence of C_{37}, Q_{19} emitter, Q_{19} base, Q_{20} collector, Q_{20} emitter, T_2 winding T_{10}, and C_{37}. The magnetic flux density increases with this discharge, the magnetomotive force is produced, and thus, the base current flows from T_2 to Q_{13}, which turns on, consequently the current flows from and auxiliary winding 1T of the converter transformer T_3 to the 10T of T_2, and the magnetomotive force increases.

When the magnetic flux density reaches a saturation value, the magnetic flux density decreases up to the residual magnetic flux density because of the disappearance of the magnetomotive force. By this slight reduction, Q_{13} is cut off, and the small voltage of reverse polarity is induced by each winding of T_2, consequently Q_{13} is perfectly cut off, and Q_{12} turns on.

For the on-state of Q_{12}, the current of reverse polarity flows from the auxiliary winding 1T of the converter transformer T_3 to the 10T of T_2, the magnetomotive force increases, and then Q_{12} is perfectly cut off.

Moreover, when the magnetic flux density reaches a negative saturation value, the magnetomotive force vanishes, and the magnetic flux density decreases up to the negative saturation flux density, thus Q_{12} is cut off and Q_{13} turns on.

With continuing the repetition of the aforementioned state, the driving current flows to the base of Q_{12} and Q_{13}.

When the converter transformer oscillates with turning Q_{19} and Q_{20} on, the current flows to the closed loop of D_{22}, and because the base potential of Q_{20} becomes minus, Q_{19} and Q_{20} become cut off when the oscillation of Q_{19} and Q_{20} continues.

4.14.12 RECTIFIER CIRCUIT (I) (II) (III)

The square wave fixed to each winding number appeared at the output winding of converter transformer is rectified and converted into the direct curent.

7.14.13 FILTER CIRCUIT (II) (III) (IV)

The low pass filter of type attentuates the high frequency noise of the direct current obtaine by the rectifier circuit.

7.14.14 REG CIRCUIT (II) (III)

The power transistors Q_{14} and Q_{15} are drived by the three terminals regulator and the stable output $\pm$12V is taken out by the boosted voltage.

7.14.15 VOLTAGE DETECTION CIRCUIT

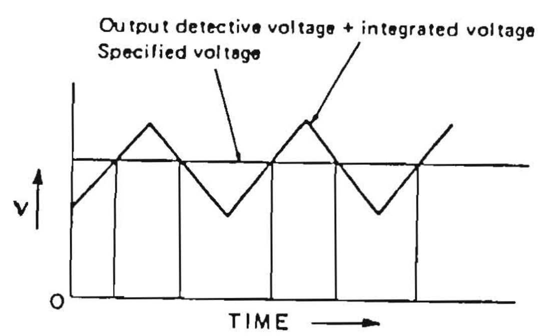
This circuit gives the output to the pulse modulation circuit as per comparing the voltage of +5V system with the specified voltage.

7.14.16 PULSE WIDTH MODULATION CIRCUIT

The output voltage of converter is integrated and is applied to the base of the voltage detecting side of the differential amplification circuit, and then is superimposed to the output detection circuit.

After this voltage is compared with the specified voltage, the pulse width modulation is carried out.

In other words, as the output voltage becomes high, the pulse width appeared to the both end of R_{45} becomes long and as the output voltage becomes low, the pulse width becomes short and, thus, this voltage, which is amplified by Q_{16} is given to the photo-coupler.



7.14.10 PROTECTIVE CIRCUIT

The protective circuit for overcurrent xdetects the secondary overcurrent at the primary side, and the protectvie cirucit for overvoltage detects the voltage applied to the converter.

With the detection of the overcurrent and overvoltage, the oscillations of each converter are stopped and the protection is achieved due to the way that the output voltage of secondary side drops up to zero.

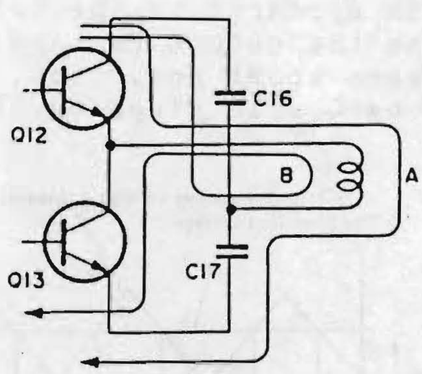
Its operation procedure is as follows. The protective circuit for overcurrent is to integrate and divide the voltage drop and to input to the gate of SCR_2.

Whereas, the protective circuit for overvoltage is to divide the voltage applied to the converter and to input to the gate of SCR_2. When either of the voltages becomes higher than the gate voltage of SCR_2, the SCR_2 turns on and the winding 10T of T_2 is short circuited by the SCR_2, so that the oscillation can stop.

7.14.11 CONVERTER CIRCUIT

The driving current is alternatively given to the base of Q_{12} and Q_{13} from the converter driving circuit, when Q_{12} turns on and Q_{13} turns off, the current flows through a path A.

On the other hand, when Q_{12} turns off and Q_{13} turns on, the current flows through a path B, accordingly, this circuit converts the direct current into the square-wave voltage and the alternating current is generated.



7.14.17 PHOTO-COUPLER

The output obtained from the pulse width modulation circuit is isolated by the photo-coupler =, and is inputted to the REG driving circuit.

Finally the voltage waveforms of the main portion are shown in the following figures.

Refer to the circuit diagram (Figure 7-138) about the points of each waveform (A,B,C,D) in Figure 7-137.

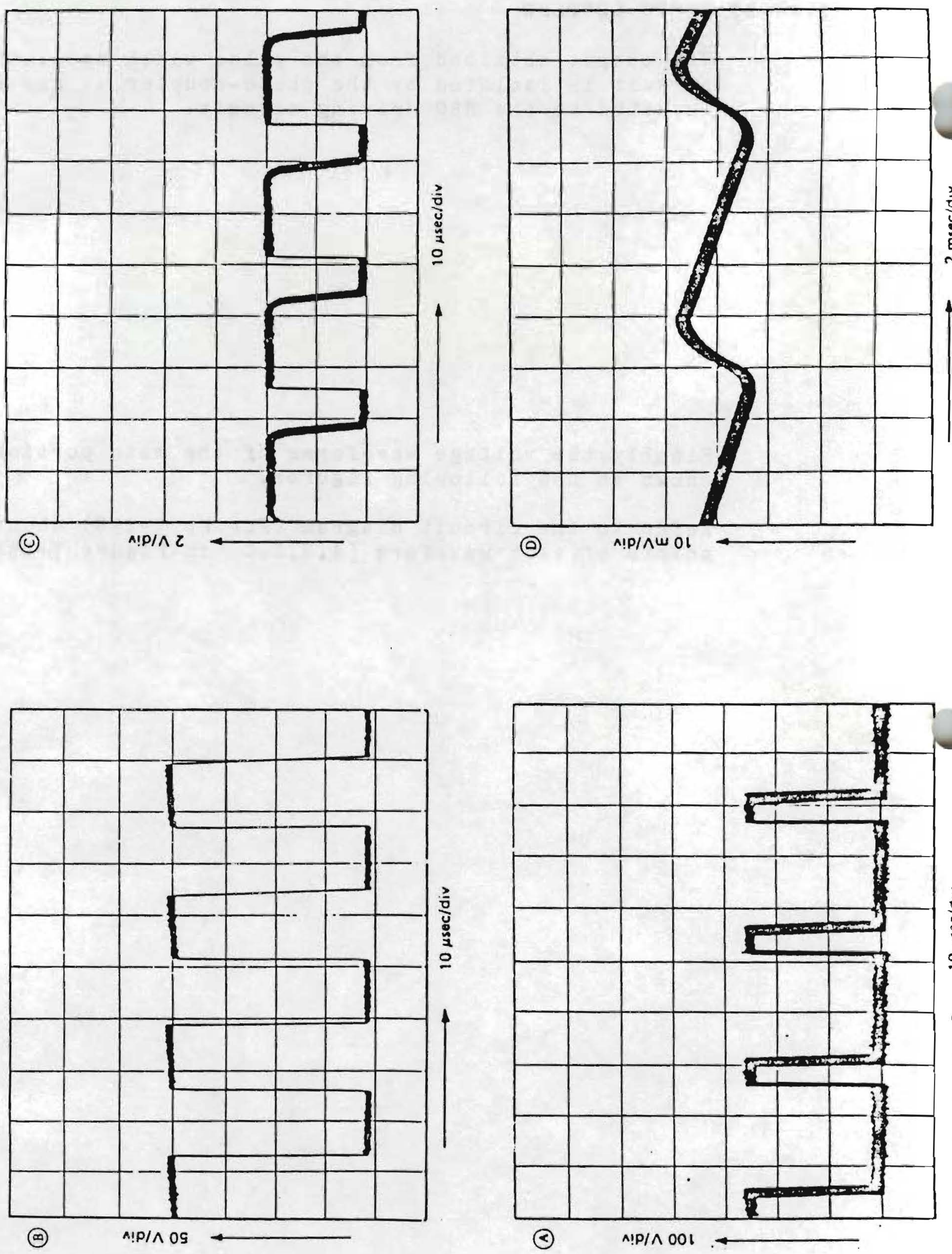
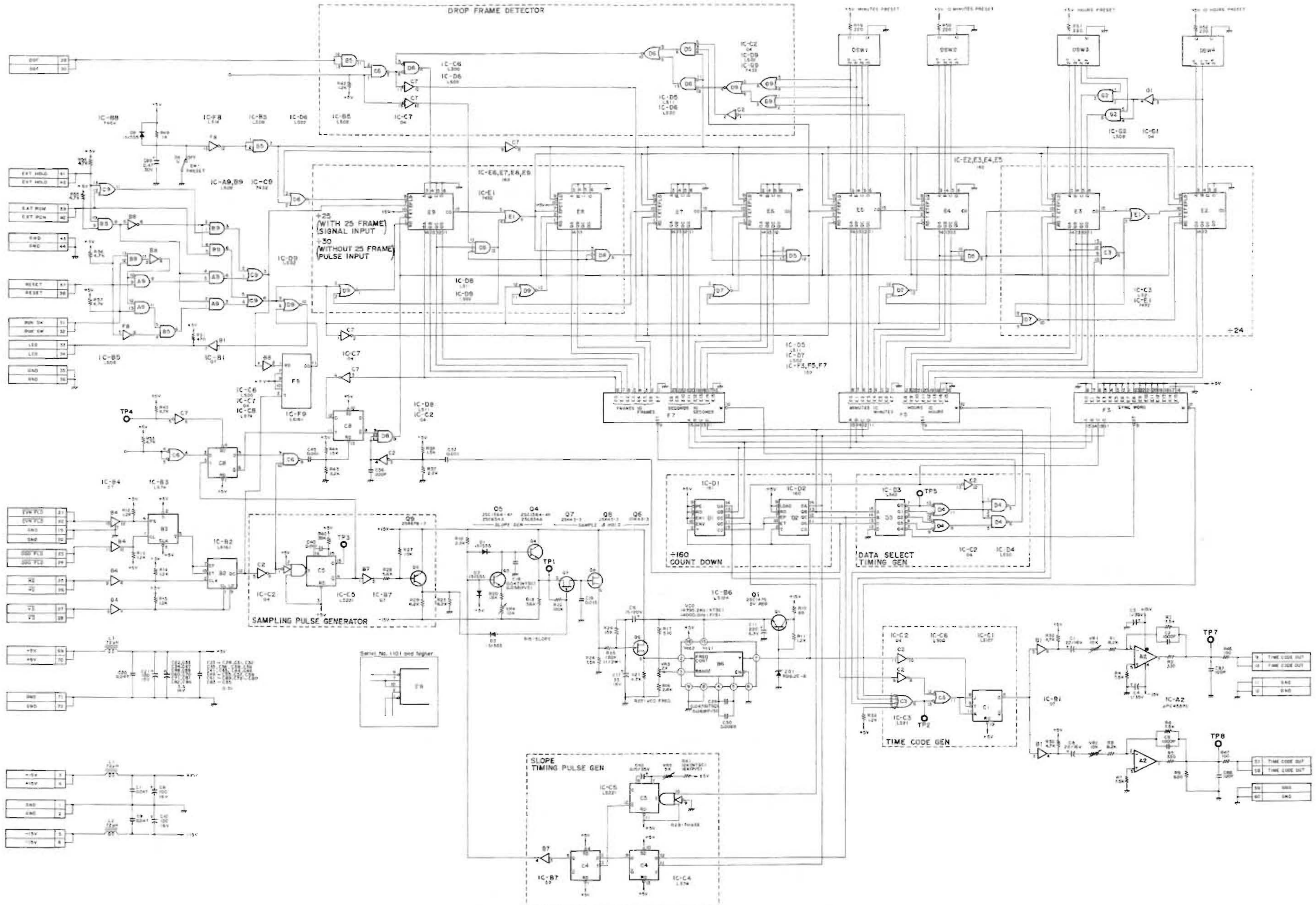
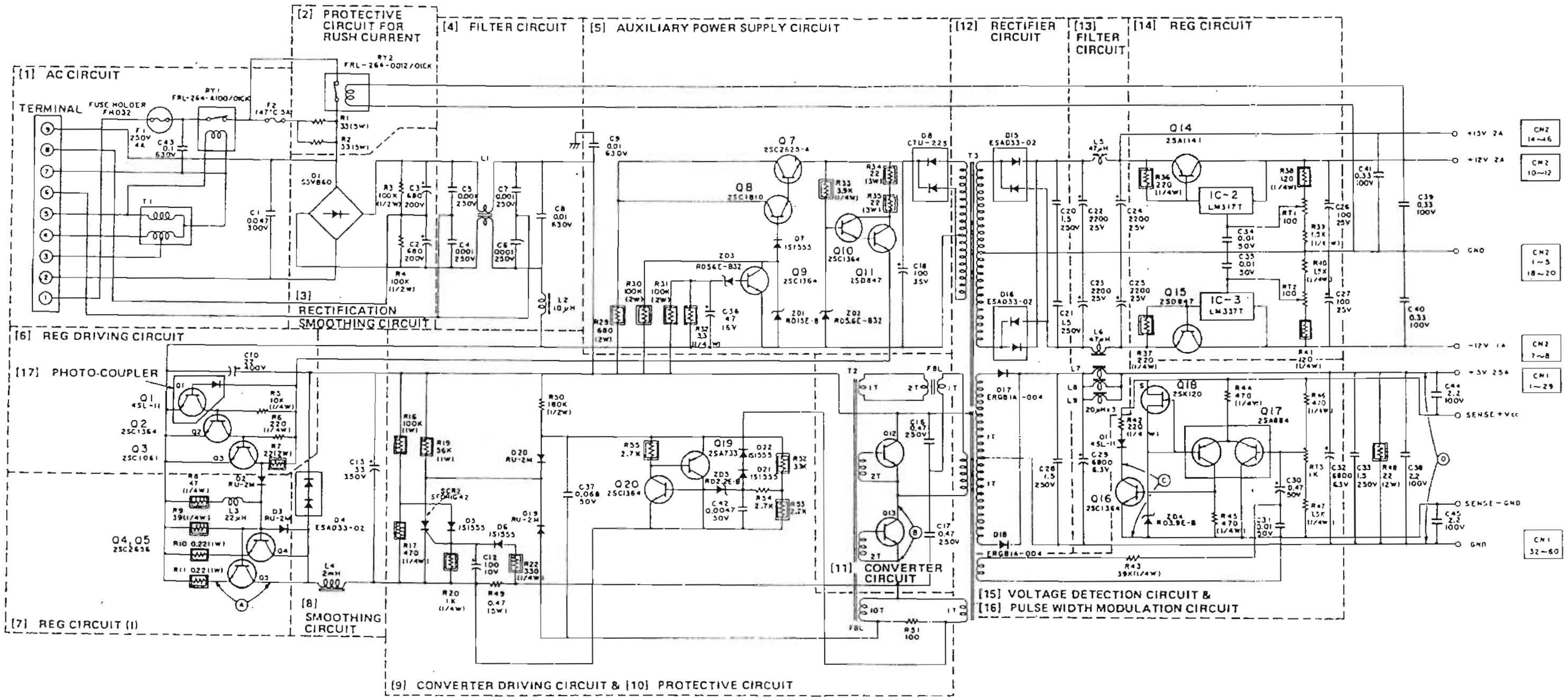

C
2 V/div
10 μsec/div
D
10 mV/div
2 msec/div
B
50 V/div
10 μsec/div
A
100 V/div
10 μsec/div

Figure 7-137

TIME CODE BOARD





POWER SUPPLY SCHEMATIC DIAGRAM

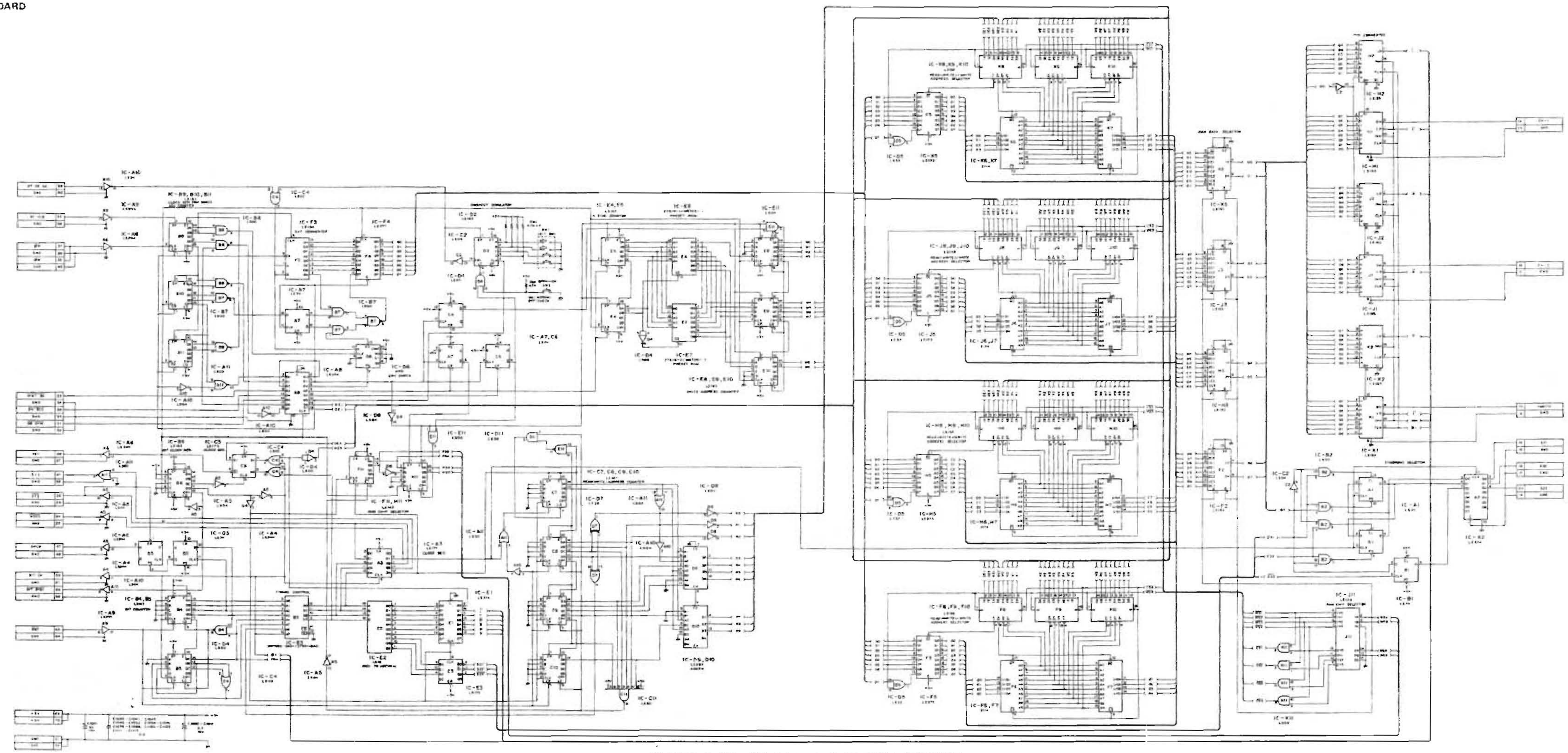
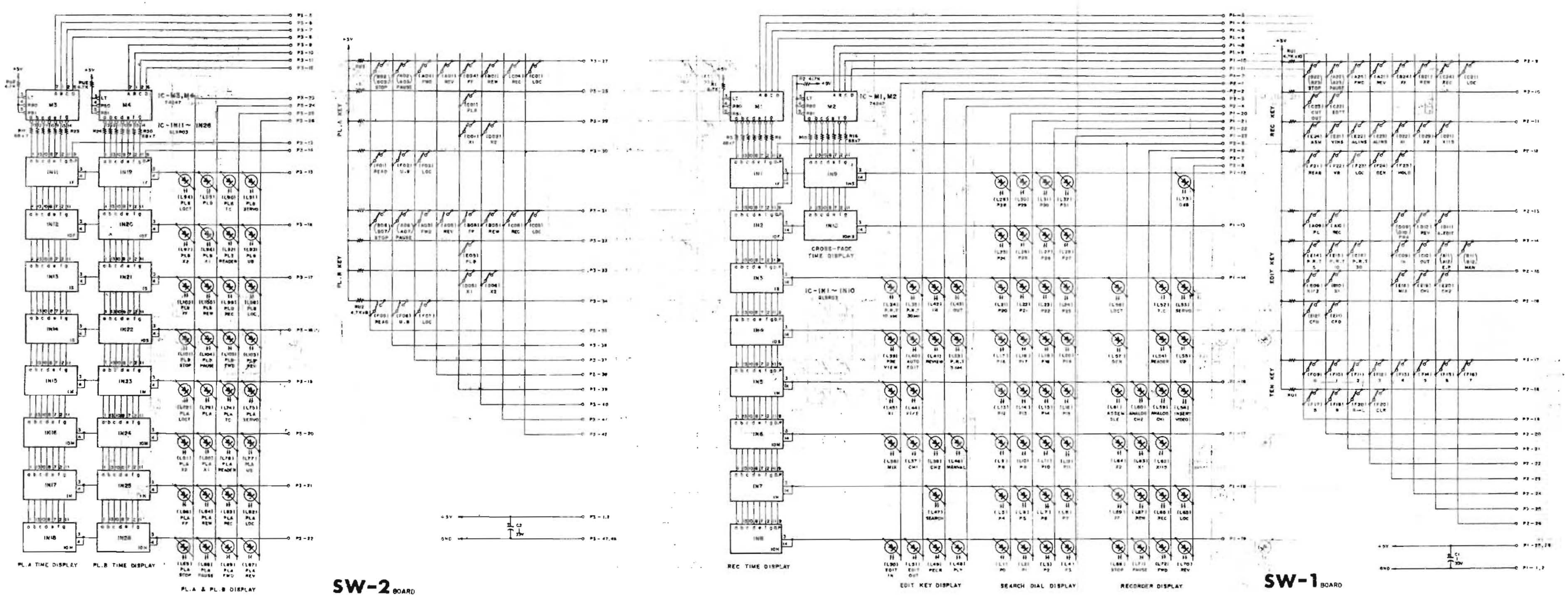


Figure 5-20 Decoder A Schematic Diagram

DECODER A BOARD

KEY BOARD UNIT ASSEMBLY 1 (SW-1 AND SW-2 BOARDS)



Schematic Diagram of the Keyboard